

MOTOROLA Semiconductors



CMOS DATA MANUAL VOLUME 1

STANDARD LOGIC

Selection Guides

quantum electronics

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2018

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Data Sheets

Mechanical Data

Handling Precautions

Reliability and Quality Assurance

Publications and Applications



Or how to find the information you need

CMOS DATA MANUAL

VOLUME 1

STANDARD LOGICUS \ STANDARD SCHOOL STANDARD STAN

- Hip Hops / Latel
 - Shift Registers
 - ale III DOO
- Storagadinos Letonay
- Fairty Generators / Checkers
 - ALD S / Hate Ministible
 - Encoders / Decoders
- Multiplexers / Demultiplexers / Bilateral Switches
 - Multivibrators / Oscillators / Timers

Volume 2 contains date on Special Functions which are defined as the following functions:

- PLL Frequency Synthesizers
 - Display Decoders / Driven
- A/D, D/A Converters / Logic Functions
 - Operational Ampliflers / Comparators
 - Remote Control Functions

- Radio / TV Functions

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Telecommunications functions are listed in the Selection Guide but data is to be found in the Telecommunications Data Manual.

Microprocessors and peripherals are listed in the Selection Guide, but deta is to be found in the Microprocessors Data Manuals (8 and 16-Bit).

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Introduction Or how to find the information you need

MOTOROLA

The European CMOS Data Manuals Volumes 1, 2 and 3 contain all the relevant data required to design and use Motorola CMOS Functions. The first two volumes replace the European CMOS Selection Data Book which was published in 1979.

Volume 1 contains data on Standard Logic which is defined as the following functions:

- NAND / NOR / AND / OR / Complex Gates
- Inverters / Buffers / Level Translators
- Schmitt Triggers
- Flip Flops / Latches
- Shift Registers
- Counters
- Adders / Comparators
- Parity Generators / Checkers
- ALU's / Rate Multipliers
- Encoders / Decoders
- Multiplexers / Demultiplexers / Bilateral Switches
- Multivibrators / Oscillators / Timers

Volume 2 contains data on Special Functions which are defined as the following functions:

- PLL Frequency Synthesizers
- Display Decoders / Drivers
- A/D, D/A Converters / Logic Functions
- Operational Amplifiers / Comparators
- Remote Control Functions
- Radio / TV Functions
- Miscellaneous Functions

Volume 3 contains data on High Speed CMOS. Who a no note much lands the much

Telecommunications functions are listed in the Selection Guide but data is to be found in the Telecommunications Data Manual.

Microprocessors and peripherals are listed in the Selection Guide, but data is to be found in the Microprocessors Data Manuals (8 and 16-Bit).

Memories are also listed in the Selection Guide. Volume 2, Special Functions, contains data on the smaller memories. The data for larger memories is to be found in the Memory Data Manual. See the selector guides for details.

The contents of each section of this book are:

1. SELECTION GUIDES

Ordering Information (page 1-2) — defines the numbering system and suffixes and gives details of processing options.

Selection Guide by Part Number (page 1-6) — contains a human alphanumeric listing of all functions with details of suffixes and pins, and where to find detailed technical data. This section can also be used as a cross reference to find equivalents for other suppliers' functions.

Selection Guide by Function (page 1-13) — lists all devices which are capable of performing broadly defined functions, and where to find detailed technical data.

Counter Selector Table (page 1-18) — gives comparative data for key characteristics of counters.

HSCMOS Selector Guide (page 1-19) — gives key family characteristics and ordering information. Lists devices by function and shows equivalent LSTTL and CMOS functions.

Gate Arrays (page 1-26) - a brief outline of the MOS Gate Arrays and the design system.

2. B-SERIES FAMILY DATA

EIA/JEDEC and Motorola formats for CMOS Industry B and UB series specifications.

3. DATA SHEETS

Technical data for all special functions. Where parts are still at the design and development stage, then the data consists of either Product Previews or Advance Information.

4. MECHANICAL DATA

Package dimensions for all devices in this book.

5. HANDLING PRECAUTIONS

The static and latch-up problems associated with MOS are now well understood. This section lists the precautions to be taken during shipment, assembly and test to avoid these problems. It is recommended that this section be read thoroughly.

6. RELIABILITY AND QUALITY ASSURANCE

This section describes the key elements of Motorola's reliability and quality assurance activities, and gives the results of the 1982 tests.

7. PUBLICATIONS / APPLICATIONS

Lists the publications available from Motorola Semiconductors.

On the back cover, there is a list of Motorola Sales Offices and Distributors.

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Selection Guides

STANDARD PRODUCTS

```
MC14001BAL
—denotes — Operating Voltage Range
— Operating Temperature Range
— Package Material
—denotes Function
```

```
SUFFIXES

AL 3 to 18 V, -55 to +125°C, Ceramic Package
CL 3 to 18 V, -40 to +85°C, Ceramic Package
CP 3 to 18 V, -40 to +85°C, Plastic Package
Limited Voltage Range, Limited Temperature Range, Ceramic Package
P Limited Voltage Range, Limited Temperature Range, Plastic Package
EFL 3 to 18 V, -55 to +125°C, Ceramic Package
FL 3 to 18 V, -40 to +85°C, Ceramic Package
EVL 3 to 6 V, -40 to +85°C, Plastic Package
VL 3 to 6 V, -40 to +85°C, Ceramic Package
VL 3 to 6 V, -40 to +85°C, Ceramic Package
VL 3 to 6 V, -40 to +85°C, Ceramic Package
VP 3 to 6 V, -40 to +85°C, Plastic Package
VP 3 to 6 V, -40 to +85°C, Plastic Package
```

OPTIONS

1. Burn-lin

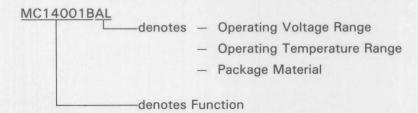
Motorola CMOS integrated circuits are manufactured under strict quality control. Inprocess screens and tight out-going inspection result in a high order of quality and reliability

In addition, Burn-in is an option available on all CMOS packaged products. The sensits of this option are:

- reduced infant mortality (typically 0.2% of the product is screened out);
 - reduced board and system rework;
 - reduced equipment downsime;
 - reduced field failures.

Ordering Information

STANDARD PRODUCTS



SUFFIXES

```
AL 3 to 18 V, -55 to +125°C, Ceramic Package
CL 3 to 18 V, -40 to +85°C, Ceramic Package
CP 3 to 18 V, -40 to +85°C, Plastic Package
L imited Voltage Range, Limited Temperature Range, Ceramic Package
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EFL 3 to 18 V, -55 to +125°C, Ceramic Package
FL 3 to 18 V, -40 to +85°C, Ceramic Package
FP 3 to 18 V, -40 to +85°C, Plastic Package
EVL 3 to 6 V, -55 to +125°C, Ceramic Package
VL 3 to 6 V, -40 to +85°C, Ceramic Package
VL 3 to 6 V, -40 to +85°C, Plastic Package
VL 3 to 6 V, -40 to +85°C, Plastic Package
VL 3 to 6 V, -40 to +85°C, Plastic Package
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VL 3 to 6 V, -40 to +85°C, Plastic Package
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VL 3 to 6 V, -40 to +85°C, Plastic Package
VL 3 to 6 V, -40 to +85°C, Plastic Package
VL 3 to 6 V, -40 to +85°C, Plastic Package
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OPTIONS

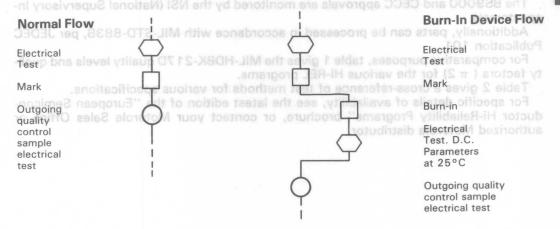
1. Burn-in

Motorola CMOS integrated circuits are manufactured under strict quality control. Inprocess screens and tight out-going inspection result in a high order of quality and reliability.

In addition, Burn-in is an option available on all CMOS packaged products. The benefits of this option are:

- reduced infant mortality (typically 0.2% of the product is screened out);
- reduced board and system rework;
- reduced equipment downtime;
- reduced field failures.

Additional processing of these burnt-in circuits is as follows: 30 .nst2 .teQ edT



Motorola Burn-in is performed under the following conditions:

V_{DD} 15 V

Temperature 125°C ambient Time 168 hours

Bias Dynamic for Memories and Analog Circuits, Static for

all others

- ADE NE MEGALLARIA

Ordering Information:
The Burn-in option is selected by adding the suffix D to the part number, for example:

MC14001BALD

2. Chips and Wafers

Chips and wafers are available for all CMOS types. For further information, consult your Motorola Sales Office or authorized Motorola Distributor.

TABLE 1 - COMPARISON OF HI-REL PROGRAMS

3. HI-REL

The HI-REL Operation in East Kilbride supplies components which have been qualified and/or processed to European standards or military specifications. The factory approvals are: Def. Stan. 05-21, BS9000, CECC.

1

The Def. Stan. 05-21 approval, which is equivalent to N.A.T.O. AQAP 1, is monitored by the British Ministry of Defence.

The BS9000 and CECC approvals are monitored by the NSI (National Supervisory Inspectorate).

Additionally, parts can be processed in accordance with MIL-STD-883B, per JEDEC Publication 101.

For comparative purposes, table 1 gives the MIL-HDBK-217D quality levels and quality factors (π 2) for the various HI-REL programs.

Table 2 gives a cross-reference of test methods for various specifications.

For specific details of availability, see the latest edition of the "European Semiconductor Hi-Reliability Programs" brochure, or contact your Motorola Sales Office or authorized Motorola distributor.

Motorola Burn-in is performed under the following conditions:

TABLE 1 — COMPARISON OF HI-REL PROGRAMS

Program	Description	MIL-HDE Level	BK-217D Factor
BS9000/CECC90000 Level B	Full Qualification, Full Processing	В	1.0
BS9000/CECC90000 Level B	Interim Qualification, Full Processing	B-0	2.0
BS9000/CECC90000 Level B	No Qualification, Full Processing	B-2	6.5
MIL-STD-883B Level B	No Qualification, JEDEC 101 Processing	B-2	6.5
BS9000/CECC90000 Level C	Full Qualification Full Processing	tus 10 Citto a	MotcO.8 Sale
BS9000/CECC90000 Level C	No Qualification Full Processing	C1	13.0
MIL-STD-883B Level C	No Qualification Full Processing	C1	13.0
Ceramic Ceramic	168 Hour Burn-in at 15 V, 125° C, with 100° C Electrical Test	Operation in East seed to Europ Def Stan Of	17.5 T PROCES

TABLE 2 — TEST METHOD CROSS-REFERENCE

Test	CECC 90000	IEC68	BS9400	Method BS2011	MIL STD883
Precap Visual				_	2010A or B
Low Temperature Storage	4.6.1.2	2-1	1.2.10A or B	Aa	
High Temperature Storage	4.6.1.1	2-2	As BS2011	Ba	1008 solv
Rapid Change in Temp. (air)	4.6.8.1	2-14-Na	1.2.6.13	Na Na	1010c
Rapid Change in Temp. (liquid)	4.6.8.3	2-14-Nc	As BS2011	Nc Nc	1011a
Humidity (Cycled)	4.6.3.1	2-4	As BS2011	Da	2600H883
Humidity (Cycled)	4.6.3.2	2-30	d CMOS Series		C74HCXX X
Humidity (Cycled)	9.	1.0	d DPSK Modulate		1004
Humidity (Constar	111	1 2-3 1016			26173
Acceleration	4.6.7 Y	PLL F7-2		4-Bit Mic	282201002
Hermeticity (fine)	4.6.9.1	2-17QK	As BS2011	Synthesia	1014A
Hermeticity (gross	Type Contractor	06172	THOUSEN OF		1014C
	4.6.10	2-20			2003
Termination	4.6.12.2	2-21	As BS2011		2004
Robustness (DIL)	AL,CL,C		or 1.2.6.16.3	Quad 2-In	014001UB
Mechanical Shock	0.J0.JA	2.27	As BS2011	Dual 4-Ing	014002B
Vibration (Swept	and the particular and a second second	2.21	nic Shift Register		C140068
	4.6.5	2-6 vnl au			200700410
Salt Mist	4.6.14	2-11	AdderA	Ka	_14008B_
Salt Mist	_ 201				1009
Operating Life Tes	t 4.8	Pin Equivalen	1.2.7.2	_	1005
Electrical Burn-In	D.S.	· · · · · · · · · · · · · · · · · · ·	1.2.9.2	Quad 2-In	1015
14 3-5	AL,CL,C	***********	out NAND Gate		C14012B
	AL,CL,C		out NAND Gate	Dual 4-in	C14012UB
			p-Flop		
	AL, CL, C		ic Shift Register.		2140148
	AL,CL,C		t Static Shift Regis slog Switch/Multis		0140158
	ALCLC		ilog switch/fautili ounter/Divider		C14016B
			le Divide-By-N Co		C14018B
			4519B - Normall	See MC1	
16 3-65			it nary Counter	Equivalen	C14020B
			ic Shift Register.		C14021B
	0.J5.JA				

X See the S-Bit Microprocessors Data Manual.
 See Data Sheet.
 See the CMOS Data Manual, Volume 3, High Speed CMOS.
 See the Telecommunications Data Manual.

Selection Guide by Part Number

MIL. STD883	Mathod BS2011	889400		CECC			
2010A or B							
		1.2.10A or 8	2-1				Low Te
Device 8001		Function	on c.c	24.6.1.1	uffix	Pins	Page
MC54HCXXX							Raid C
10106	nigii spe	ed CMOS Series.	2-14-Na	4.6.8.1			
MC68HC04P2	8-Bit Sing	gle Chip Microcoi OS Microcomput	mputer	L	P,Z	28	×
MC68HC04P3 MC68HC05C4		gle Chip Microco			P,Z P,Z	40	in X emp
MC68HC09E		roprocessor					Hixnidit
MC74HCXXX		ed CMOS Series.			. ,—		Hemidit
MC6172		ud DPSK Modula				24	l tramidit
MC6172		ud DPSK Demod			P (mater	-	
MC6220		crocomputer with			-/- (2110201		neleco.A
					P	28	8
MC6860	Low Spec	zer (NMOS Deviced Modem	2-170K	4.6.9.1	_,P	24	Hermeti
MC6862	Part Num	ber changed to N	/IC6172	4.6.9.2	pross)		
MC14000UB	Dual 3-In	put NOR Gate Plu	us Inverter		CL,CP	14	3-200
MC14001B	Quad 2-li	nput NOR Gate		AL,	CL,CP	14	3-5
MC14001UB		nput NOR Gate			CL,CP	14	3-14
MC14002B		put NOR Gate			CL,CP	14	
MC14002UB		put NOR Gate					3-14
MC14006B MC14007UB		atic Shift Registe					3-20
MC140070B		nplimentary Pair F Adder					3-24
4009		4049UB - Pin fo			CL,CI		
4010		4050B - Pin for		nt			
MC14011B		nput NAND Gate			CL,CP	14	3-5
MC14011UB		nput NAND Gate			CL,CP		3-14
MC14012B		put NAND Gate .			CL,CP	14	3-5
MC14012UB	Dual 4-In	put NAND Gate .			CL,CP	14	3-14
MC14013B	Dual D Fli	ip-Flop		AL,	CL,CP	14	3-36
MC14014B		tic Shift Register			CL,CP	16	3-40
MC14015B		t Static Shift Reg			CL,CP	16	3-44
MC14016B		alog Switch/Mult			CL,CP	14	3-50
MC14017B		Counter/Divider			CL,CP	16	3-56
MC14018B		ole Divide-By-N C			CL,CP	16	3-61
4019B	See MC1 Equivaler	4519B - Norma	lly Pin for Pir	1			
MC14020B		nary Counter		ΔΙ	CL,CP	16	3-65
MC14021B		tic Shift Register			CL,CP	16	3-40
	Octal Cou			· · · · · · · · · · · · · · · · · · ·		10	0 10

[×] See the 8-Bit Microprocessors Data Manual.
§ See Data Sheet.
☐ See the CMOS Data Manual, Volume 3, High Speed CMOS.
● See the Telecommunications Data Manual.

Device	Function Suffix	Suffix	Pins	Page
MC14023B	Triple 3-Input NAND Gate	AL, CL, CP	14	3-5
MC14023UB	Triple 3-Input NAND Gate		14	2 25 1 2 20 1 2 1
MC14024B	7-Stage Ripple Counter		1.4	3-76
MC14025B	Triple 3-Input NOR Gate	AL,CL,CP	14	3-5
MC14025UB	Triple 3-Input NOR Gate		14	3-14
MC14027B	Dual J-K Flip-Flop	AL,CL,CP	16	3-82
MC14028B	BCD-to-Decimal/Binary-to-Octal Decoder		16	3-86
MC14029B	Binary/Decade Up/Down Counter	AL,CL,CP		3-91
4030B	See MC14070B - Pin for Pin Equivalent			MC1416
4030B 4031B	See MC14070B - Pin for Pin Equivalent See MC14557B - Functionally Equivalent			
MC14032B	Triple Serial Adder (Positive Logic)	AL,CL,CP	16	3-97
MC14034B	8-Bit Universal Bus Register	AL,CL,CP	24	3-102
MC14035B	4-Bit Shift Register	AL,CL,CP	16	3-109
MC14038B	Triple Serial Adder (Negative Logic)		16	
MC14040B	12-Bit Binary Counter	AL,CL,CP	16	3-114
MC14042B	Quad Transparent Latch	AL,CL,CP	16	3-118
MC14043B	Quad NOR R-S Latch	AL,CL,CP	16	3-122
MC14044B	Quad NAND R-S Latch	AL,CL,CP	16	3-122
MC14046B	Phase-Locked Loop	AL,CL,CP	16	3-126
4047B	See MC14528B - Functionally Equivalent	DURBIN WOS	7	
MC14049UB	Hex Inverter/Bufferfiuo1	AL,CL,CP	16	3-131
MC14050B	Hex Buffer	AL,CL,CP	16	3-131
MC14051B	8-Channel Analog Multiplexer/Demultiplexer	AL,CL,CP	16	3-135
MC14052B	Dual 4-Channel Analog Multiplexer/			
0 01	Demultiplexer	AL.CL.CP	16	3-135
MC14053B	Triple 2-Channel Analog Multiplexer/			
16 0	Demultiplexer	AL,CL,CP	16	3-135
4055B	See MC14543B - Functionally Equivalent			
4056B	0 110115105 11 11 51 1 51	PCM Sample		
4057B	See MC14581B - Functionally Equivalent			
MC14060B	14-Bit Binary Counter and Oscillator	AL,CL,CP		MC1441
		and the second second	14	3-141
4061	See MCM14537 - Functionally Equivalent			MC1441
4063	See MC14585B - Functionally Equivalent	PCM Time of		
MC14066B	Quad Analog Switch/Multiplexer	AL,CL,CP	14	3-145
MC14067B	16-Channel Analog Multiplexer/Demultiplexer	AL,CL,CP	24	3-150
MC14068B	8-Input NAND Gate	AL,CL,CP	14	3-5
MC14069UB	Hex Inverter	AL,CL,CP	14	3-157
MC14070B	Quad Exclusive OR Gate	AL,CL,CP	14	3-159
MC14071B	Quad 2-Input OR Gate	AL,CL,CP	14	3-5
MC14072B	Dual 4-Input On Gate	AL,CL,CP	14	3-5
MC14073B	Triple 3-input AND Gate	AL,CL,CP	14	3-5
MC14075B	Triple 3-Input OR Gate	AL,CL,CP	14	3-5
MC14076B	Quad D-Type Register	AL,CL,CP	16	3-165
MC14077B	Quad Exclusive NOR Gate	AL,CL,CP	14	3-159
MC14078B	8-Input NOR Gate	AL,CL,CP	14	3-5
MC14081B	Quad 2-Input AND Gate	AL,CL,CP	14	3-5
MC14082B	Dual 4-Input AND Gate	AL,CL,CP	14	3-5
4085B	See MC14506B - Functionally Equivalent			Note A: Ac Note B: Ac

Device 2019	Function notions	Suffix	Pins	Page
MC14093B	Quad 2-Input NAND Schmitt Trigger	AL.CL.CP	14	3-173
MC14094B	8-Bit Bus Compatible Shift/Store Latch	AL.CL.CP	16	THE RESERVE
MC14097B	Dual 8-Channel Analog Multiplexer/	7-Stage Rip	:48	MC1402
14 3-5	Demultiplexer	AL,CL,CP	24	3-150
4098B	See MC14528B - Normally Pin for Pin	Triple 3-Inp	808	MC1402
16 3-82	Equivalent			
MC14099B	8-Bit Addressable Latch	AL,CL,CP	16	3-182
MC14106B	Hex Schmitt Trigger	AL,CL,CP		3-189
MC14160B	Synchronous Programmable Decade Counter		16	
MC14161B	· and a supplemental and a suppl	See MC14	12.71	EOA 403
WICTTIOID	Counter	AL,CL,CP	16	3-189
MC14162B	Synchronous Programmable Decade Counter	AL,CL,CP	16	3-189
MC14163B	Synchronous Programmable 4-Bit Binary	AL,CL,CI	AB	3-103
WIC 14 103B	gn In IA	AL,CL,CP	16	3-189
MC14174B	Counter	prince of colores	0.0	
MC14174B	Hex D Flip-Flop	AL,CL,CP	16	3-197
MC14175B	Quad D Flip-Flop	AL,CL,CP	16	3-201
MC14194B	4-Bit Universal Shift Register	AL,CL,CP	16	3-205
MC14400	PCM Monocircuit	Quad NANI	16	METAGA
MC14401	PCM Monocircuit	Phasp-Lock	18	MCIAOA
MC14402	PCM Monocircuit	_	22	
	528B - Functionally Equivalent		28	VO9-
MC14403	PCM Monocircuit	Hex hyverte	16	MC 404
MC14405	PCM Monocircuit	rattue xeH	16	MC 405
MC14408	Binary-to-Phone Pulse Converter		16	MC 405
MC14409	Binary-to-Phone Pulse Converter	ario L.Psud	16	MC 405
MC14410	2-of-8 Tone Encoder	celait L.Pred	16	•
MC14411	Bit-Rate Frequency Generator		24	Mereos
MC14412	Universal Low Speed Modem	FL,FP,VL,VP	16	•
MC14413	PCM Sampled Data Filter, See Note A	L,P	16	2010
	24.20 - Functionally Equivalent	Z	18	
MC14414	PCM Sampled Data Filter, See Note A	L,P	16	
		7	18	
MC14415	Quad Precision Timer/Driver	EFL,FL,FP	16	3-209
14 3-141	ry Counter and Oscillator AL, CL, CP			
MC14416	PCM Time Slot Assigner Circuit	See PLACE	16	●408
MC14417	PCM Time Slot Assigner Circuit	ANDL,Pess	18	●406
MC14418	PCM Time Slot Assigner Circuit	L,P	22	
MC14419	2-of-8 Keypad-to-Binary Encoder	L,P	16	3-214
MC14426	8 × 14-Bit Static Tuning Memory	ennanp)-ot	16	0
MC14429	Tuning Memory Control, See Note B	8-logat NAI	18	MCOAOO
MC14430	Input Address Encoder	Hex gverte	16	3-218
MC14433	Input Address Encoder	L,P	24	MCCADY
MC14442	Microprocessor Compatible A/D Converter	L.P	28	MCTAU
MC14443	6-Channel A/D Converter Subsystem	I P	16	MCT407
MC14444	Microprocessor Compatible A/D Converter	L,P	40	MC 407
MC14447	6-Channel A/D Converter Subsystem	L,P	16	MCO407
3-165	90,10,1A	Quad D-Typ	. 99	MCT407

See the CMOS Data Manual, Volume 2, Special Functions.
 See the Telecommunications Data Manual.

Note A: Add Suffix 1 or 2. Example MC14413L2. Note B: Add Suffix B. Example MC14429PB.

Device	Function Suffix	Suffix	Pins	Page
84449UB	See MC14049UB, Pin for Pin Equivalent			
MC14457	Remote Control Transmitter	Programm	16	MG 45
MC14458	Remote Control Receiver	BCIq to-7-		MO 45
MC14466	Low Cost Smoke Detector	BCIq-10-7-		MG 45
MC14467	Low Cost Smoke Detector	with Ripple	16	0
MC14468	Interconnect Smoke Detector	Higg Curre		MG 45
MC14469	Addressable Asynchronous Receiver/Transmitter		40	0
MC14490	Hex Contact Bounce Eliminator	Dug Mono		MG 45
MC14493	Binary-to-7-Segment Latch Decoder/Driver	(Reguladera	16	0
MC14494	Binary-to-7-Segment Latch Decoder/Driver			MG 45
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O See the CMOS Data Manual, Volume 2, Special Functions.

Note C: There are two versions of this device, with different electrical and switching characteristics. To order, one has suffix L or P and the other L1 or P1. See data sheets for details.

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MC14547B	High Currer	nt BCD-to-7-Segment			MC144
40 0		iver		16	AA OM
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	(Retriggeral	ble/Resettable)	C-ot-L,Pii8	16	3-358
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	Equivalent	on Monostable Multivibrator			
40101B		531B - Functionally Equivalent			
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O See the CMOS Data Manual, Volume 2, Special Functions. O stock and the control of the control

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40160B			Equivalent Equivalent			MC148
40161B			Equivalent			
40162B			Equivalent			
40163B			Equivalent 3 119 11			
40174B			Equivalent Salds			
40175B			Equivalent			
40181B			Equivalent 113 sta			
40182B			Equivalent sersylal			
40192B			lly Equivalent			
40193B			lly Equivalent			
40193B			Pin for Pin			
401346	Equivalent		niversal Digital-Loop			
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402000	Equivalent		niversal Digital-Loop			MC145
110110166						- T 1 40191
MC142100	4 × 4 Cross Po	oint Switch	ave)	AL,CL,CP	16	WC145
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MC144115	16-Segment I	CD Driver	Tone Signalling Fifter	siri op os	27	
MC144117	4-Digit Duple:	k Mode LCD Dec	coder/Driver	eiusapiu i		0
MC144122	Remote Contr	ol Receiver	d Modern Filter	eeds byon	10	
MC144124	High Performa	ance Remote Co	ntrol Receiver	sedebion	24	0
MC144130	TV Stereo De	coder	PSK Modem	1200 8	20	()
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MC145104	PLL Frequence	y Synthesizer	4.00.000.000.000	× aaR		11/10
MC145106			MAAA.siras2.sig			MOV
MC145107	PLL Frequence	y Synthesizer	A.Bic StoricaRAM	984 ×	16	0
MC145109	PLL Frequence	y Synthesizer	······································	× 8aPc	16	ANO ME
MC145112	PLL Frequence	y Synthesizer		P	18	O
MC145143	PLL Frequence	y Synthesizer		P	16	an Ou
MC145144		s Input PLL Fre				MCMS
	Synthesizer			L,P	16	0
MC145145	4-Bit Data Bu	s Input PLL Fre	quency	× 81		INCINI
	Synthesizer			L,P	18	0
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MC145157	The state of the s		nthesizer			040
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MC145414			led Data Filters			010
MC145415			ow Pass		1758	
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IVIC 145420			o Transceiver			
140445400	•	T. S.	5.10BFunctional			04.
MC145422			Transceiver 3 7 3		1938	
			1.84BNormally.1		22	0 40
MC145423		rsal Digital-Loo		Equivalent		
			5808Novoally.i		20	04 •
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MC145429	Telset Audio In	terface		OAL,PAH		MOIAA
MC145431	Tuneable Lowp	pass/Bandpass	Filter	L,P		MO144
MC145432	2600 Hz Tone	Signalling Filter	r	L,P	18	MOLAA
MC145433	Tuneable Notc	h/Bandpass Filt	er	L,P		Melda
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MCM5101	256 × 4-Bit S	tatic RAM	Converter	C,P		MC145
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MCM14524			te D		16	0
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MCM65116	2048 × 8-B	it Static RAM		eupe C p. 9	24	MC148
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MCM65256	32768 × 8-B	it ROM		ander b	20	The state of the s
MCM65516	2048 × 8-B	it Multipleyed B	us ROM	L,P-A	18	MC145
MCM144102		Bit Static RAM	Bos triput PLC Pre-	etad Pa-4	8	84 O M

 [×] See the 8-Bit Microprocessors Data Manual.
 + See the Memory Data Manual.
 ■ See the Telecommunications Data Manual.
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Note D: Available only by special order.

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MC14069UB MC14502B MC14503B MC14504B MC14584B See also MC140 Schmitt Triggers MC14093B MC14583B MC14106B MC14584B Flip-Flops/Latches MC14013B MC14027B MC14042B MC14042B MC14043B MC14044B MC14076B MC14076B MC14175B MC14508B MC14174B	Hex Inverter Strobed Hex Inverter/Buffer Hex 3-State Buffer Hex TTL or CMOS to CMOS Level Shifter Hex Schmitt Trigger Hex Schmitt Trigger Dual Schmitt Trigger Hex Schmitt Trigger Dual D Flip-Flop Quad Latch Quad NOR R-S Latch Quad NAND R-S Latch Quad D-Type Register Quad D-Type Register Quad D-Flip-Flop Dual 4-Bit Latch Hex D Flip-Flop Dual 4-Bit Latch Hex D Flip-Flop	3-226 3-230 3-234 3-445 3-173 3-439 3-188 3-445 3-36 3-82 3-118 3-122 3-122 3-165 3-201 3-242 3-197
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MC14069UB MC14502B MC14503B MC14504B MC14584B See also MC140 Schmitt Triggers MC14093B MC14583B MC14584B Flip-Flops/Latches MC14013B MC14027B MC14042B MC14042B MC14043B MC14044B MC14044B MC14076B MC14175B MC14508B MC14174B MC14099B	Hex Inverter Strobed Hex Inverter/Buffer Hex 3-State Buffer Hex TTL or CMOS to CMOS Level Shifter Hex Schmitt Trigger Hex Schmitt Trigger Dual Schmitt Trigger Hex Schmitt Trigger Dual D Flip-Flop Quad Latch Quad NOR R-S Latch Quad NAND R-S Latch Quad D-Type Register Quad D-Type Register Quad D-Flip-Flop Dual 4-Bit Latch Hex D Flip-Flop Dual 4-Bit Latch Hex D Flip-Flop	3-226 3-230 3-234 3-445 3-173 3-439 3-188 3-445 3-36 3-82 3-118 3-122 3-122 3-165 3-201 3-242 3-197

Device	noitenuil Function	Page
Shift Registers	narator/Checker	Perity Ge
MC14035B	4-Bit Shift Register	3-109
MC14194B	4-Bit Universal Shift register	3-205
MC14015B	Dual 4-Bit Static Shift Register	3-44
MC14580B	4 × 4 Multiport Register	3-425
MC14014B	8-Bit Static Shift Register	
MC14021B	8-Bit Static Shift Register	
MC14034B	8-Bit Universal Bus Register	
MC14094B	8-Bit Bus Compatible Shift/Store Latch	3-177
MC14006B	18-Bit Static Shift Register	3-20
MC14557B	1-to-64 Bit Variable Length Shift Register	
MC14517B	Dual 64-Bit Static Shift Register	3-269
MC14562B	128-Bit Static Shift Register	3-3984 604
3-214	119 2-of-8 Keypad-to-Binary encoder	MC14
	30 Input Address Encoder	
	14B 4-Bit Latch/4-to-16 Line Decoder (High)	MC14!
MC14024B	7-Stage Ripple Counter	3-76
MC14024B	Octal Counter/Divider	3-70
MC14017B	Decade Counter/Divider	3-56
MC14017B	Presettable Divide-By-N Counter	3-61
MC14160B	Synchronous Programmable Decade Counter	3-189
MC14162B	Synchronous Programmable Decade Counter	3-189
MC14102B	Real Time 5-Decade Counter	3-327
MC14029B	Binary/Decade Up/Down Counter	3-91
MC14029B		3-65
MC14020B	14-Bit Binary Counter	3-114
MC14060B	14-Bit Binary Counter and Oscillator	3-114
MC14161B	Synchronous Programmable 4-Bit Binary Counter	3-189
MC14163B	Synchronous Programmable 4-Bit Binary Counter	3-189
MC14516B	Binary Up/Down Counter	3-263
MC14510B	Dual Binary Up Counter	3-273
MC14521B	24-Stage Frequency Divider	3-283
MC14526B	Programmable Binary Divide-By-N Counter	3-289
MC14568B	Phase Comparator and Programmable Counters	3-408
MC14569B	Dual Programmable BCD/Binary Counter	3-418
MC14510B	BCD Up/Down Counter	3-247
MC14510B	Programmable BCD Divide-By-N Counter	3-289
MC14522B	Dual BCD Up Counter	3-273
MC14510B		3-371
	558 Dual Binary to 1-of-4 Decoder	MC148
	SSB Dual Binary to 1-of-4 Decoder (Inverting)	
Adders/Compara		
MC14008B	4-Bit Full Adder	3-28
MC14032B	Triple Serial Adder (Positive Logic)	
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MC14560B	NBCD Adder	3-388
MC14561B	9's Complementer	3-392
MC14582B	Look Ahead Carry Block	3-435
MC14585B	4-Bit Magnitude Comparator	3-448

Device	Function Function	Page
Parity Generator/	Checker	
MC14531B	12-Bit Parity Tree	3-31
	4-Bit Universal Shift register	MC141948
ALU's/Rate Multi	4 x 4 Multiport Register	
MC14527B	BCD Rate Multiplier	3-29
MC14554B	2 × 2-Bit Parallel Binary Multiplier	
MC14581B	4-Bit Arithmetic Logic Unit	84604 3-43
3-177	8-Bit Bus Compatible Shift/Store Latch	MC14094B
ncoders/Decode	1-to-64 Bit Variable Length Shift Registerra	
		MC145178
MC14028B	BCD-to-Decimal/Binary-to-Octal Decoder	
MC14419	2-of-8 Keypad-to-Binary encoder	
MC14430 MC14514B	Input Address Encoder	
	4-Bit Latch/4-to-16 Line Decoder (High)	
MC14515B	4-Bit Latch/4-to-16 Line Decoder (Low)	
MC14532B MC14555B	8-Bit Priority Encoder	3-32
MC14556B	Dual Binary to 1-of-4 Decoder Dual Binary to 1-of-4 Decoder (Inverting)	3-36
MC14508	Pameta Central Encoder	
MC145026	Remote Control Encoder	MC140188
MC145027 MC145028	Remote Control Decoder	1901 41 6UB
MC145028	Remote Control Decoder	00141628
	Remote Control Decoder	
	Binary/Decade Up/Down Counter	
Multiplexers/Dem	nultiplexers/Bilateral Switches	
MC14016B	Quad Analog Switch/Multiplexer	
MC14066B	Quad Analog Switch/Multiplexer	
MC14053B	Triple 2-Channel Analog Multiplexer	
MC14551B	Quad 2-Channel Analog Multiplexer	
MC14052B	Dual 4-Channel Analog Multiplexer	
MC14529B	Dual 4-Channel Analog Data Selector	
MC14539B	Dual 4-Channel Data Selector/Multiplexer	
MC14051B	8-Channel Analog Multiplexer	3-13
MC14512B	8-Channel Data Selector	3-25
MC14097B	Differential 8-Channel Analog Multiplexer	
MC14067B	16-Channel Analog Multiplexer	
MC14519B	4-Bit And/Or Selector	
MC14007UB	Dual Complementary Pair Plus Inverter	
MC14555B	Dual Binary to 1-of-4 Decoder	
MC14556B	Dual Binary to 1-of-4 Decoder (Inverting)	3-38
Multivibrators/Os		
MC14060B	14-Bit Binary Counter and Oscillator	
MC14415		
	24-Stage Frequency Divider	
	B's Complementer	MC145618
	Manuel, Volume 2, Special Functions.	

De	vice		ROT		NATIVITER	nction			Page
MC MC	C14528B C14536B C14538B C14541B C14548B C14566B		Programma Dual Mono	able Osci stable M	ultivibrator erostable Mul llator-Timer ultivibrator e Generator	tivibra	itor	 	 3-340
	Yes	_	1						
PLL F	requency	Syn	thesizer						
M	C14046B		Phase-Lock	ked Loop				 	 3-126
	Yes				04-016				
					01-04				
									MC141626
									MC145188
					*60-00				
			4, 16, 64 or 100						
			1-10 or 1-16						

Selectable Multiplayed Durant

TABLE 3 — COUNTER SELECTOR

3-301 3-331 3-34(Binary (Bits)	Octal	Decade	BCD	UP/ Down	Outputs	Carry Out/In	÷ Ratio	Preset/ Program	Reset/ Clear	On-chip Osc.
MC14017B			1		J. U.	Q0-Q9	Out lds	mmengon ⁱ	- 8	Yes	IVI_
MC14018B	5		CFX	-0-09	U	Q1-Q5	stable M	2-10	Yes	100	NA
MC14020B	14				U	Q1, Q4-Q14	ne_Basi	laiweubn	_ 80	Yes	IVI_
MC14022B	_	1	-	_	U	Q0-Q7	Out	_	_	Yes	_
MC14024B	7	_	-	_	U	Q1-Q7		-	-	Yes	-
MC14029B	4#	_	-	1#	U/D	Q0-Q3	Out/In	1-16 or	Yes	senber	1 119
								1-10	88	14046	11/4
MC14040B	12	-	-	_	U	Q1-Q12		-	_	Yes	-
MC14060B	14	-	-	-	U	Q4-Q10 Q12-Q14		-	-	Yes	Yes
MC14160B	- 1	-	-	1	U	Q1-Q4	Out	1-10	Yes	Yes	-
MC14161B	4	-	_	_	U	Q1-Q4	Out	1-16	Yes	Yes	-
MC14162B	-	-	-	.1	U	Q1-Q4	Out	1-10	Yes	Yes	-
MC14163B	4	-	-	-	U	Q1-Q4	Out	1-16	Yes	Yes	-
MC14510B	-	-	_	1	U/D	Q1-Q4	Out/In	1-10	Yes	Yes	-
MC14516B	4	_	-	-	U/D	Q0-Q3	Out/In	1-16	Yes	Yes	-
MC145188	-	-	-	2×1	U	Q0-Q3		- 1	T	Yes	-
MC14520B	2×4	-	-	-	U	Q0-Q3	-	-	-	Yes	-
MC14521B	24	-	-	-	U	Q18-Q24	-	-	-	Yes	Yes
MC14522B	-	-	-	1	D	Q0-Q3	Out/In	1-10	Yes	Yes	-
MC14526B	4	-	-	-	D	Q0-Q3	Out/In	1-16	Yes	Yes	-
MC14534B	-	_	5	_	U	Q0-Q3*	Out	-	_	Yes	-
MC14553B	-	-	-	3	U	Q0-Q3*	Out			Yes	Yes
MC14568B	7	-	-	-	U	Q1		4, 16, 64 or 100			-
	4	-	-	-	U	-	Out	1-16	Yes	-	-
MC14569B	1#	-	-	1#	U	-	In	1-10 or 1-16	Yes	-	-
	1#	-	-	1#	U	Q	In	1-10 or 1-16	Yes		-

Selectable.
* Multiplexed Output.

Introducing a new dimension in CMOS¹

Motorola's new family of standard-logic High-Speed CMOS integrated circuits provides the designer with a complete series of functions which approaches the ideal in performance.

All of the present CMOS logic family features, including low power dissipation and high noise immunity, combine with LSTTL speeds, pinouts and drives to offer the marketplace a new dimension in CMOS standard logic.

- Guaranteed Propagation Delay 15 ns for 74HC00
- Wide Operating Range 2-6 V Recommended
- High Noise Immunity Typically 45% of Supply Voltage
- Low Quiescent Power Dissipation
- Diode Protection All Inputs
- High Fanout 10 LSTTL Loads (4 mA Drive)
- Direct Pin Compatibility with LSTTL Parts (HCXXX or HCTXXX) and CMOS Parts (HC4XXX)
- Input Logic Compatible with CMOS Parts (HCXXX or HC4XXX) and/or LSTTL Parts (HCTXXX)
- Proven Reliability and Process BASIC NUMBERING PARAMETERS and heather large Example: L8244 Octal Buffer/Line Drive Motorola Circuit Identifier Temperature Range - 74 for Commercial Range (- 40°C to 85°C) 54 for Extended Range (-55°C to 125°C) -Package Type High-Speed CMOS Specification - N for Plastic (74 Series Only) Identifier J for Ceramic HC for Buffered High-Speed CMOS HCU for Unbuffered High-Speed CMOS * -Basic Device Type HCT for TTL Input Compatible CMOS * A SEL Not Available On All Devices

1 For full information, see the CMOS Data Manual, Volume 3, High Speed CMOS

1

HIGH SPEED CMOS FUNCTION SELECTOR GUIDE

- Parts shown are functional equivalent except when preceded by an asterisk (*), indicating a suggested alternative
- Device numbers preceded by a "★" are new proprietary designs

High-Speed Device Number MC74/MC54	Function	Functional Equivalent LSTTL Device 74/54	Functional Equivalent CMOS Device MC1XXXX or CDXXXX	Direct Pin Compatibility	Number of Pins
GATES	(DOBSO n) n	niomann	ile savore	a maio	allo escribed
HC00 HC02 HC03	Quad 2-Input NAND Gate Quad 2-Input NOR Gate Quad 2-Input NAND with Open Drain Outputs		4011 4001 *4011	LS LS LS	14 14 81014
HC08 HC10	Quad 2-Input AND Gate Triple 3-Input NAND Gate	LS08 LS10	4081 4023	LS LS	14 14
HC11 HC20 HC27 HC30 HC32	Triple 3-Input AND Gate Dual 4-Input NAND Gate Triple 3-Input NOR Gate 8-Input NAND Gate Quad 2-Input OR Gate	LS11 LS20 LS27 LS30 LS32	4073 4012 4025 4068 4071	LS LS LS LS LS	14 14 14 14 14
HC51	2-Wide, 2-Input/2-Wide,	LS51	*4506	LS	14
★HC58	3-Input AND-OR-INVERT Gates 2-Wide, 2-Input/2-Wide, 3-Input AND-OR Gates	*LS51	*4506	perating H oise Immur	M d14
HC86 HC132	Quad 2-Input Exclusive OR Gate Quad 2-Input Schmitt-Trigger NAND Gate	LS86 LS132	4070 4093	LS CLION	0 14J
HC133	13-Input NAND Gate	LS133	LITTRIC	LS	16
HC266	Quad 2-Input Exclusive NOR Gate (Non Open Drain)	LS266	4077	LS/CMOS	Diffect
HC4002 HC4075 HC4078	Dual 4-Input NOR Gate Triple 3-Input OR Gate 8-Input NOR Gate	*LS25	4002 4075 4078	CMOS CMOS CMOS	14 14 14
BUFFERS / IN	IVERTERS	(2)	AA IJH) e	her Jilo.	-ana-or
HC04 HC104 HC14 HC240/ HC7240 HC241/ HC7241	Hex Inverter Hex Unbuffered Inverter Hex Schmitt-Trigger Inverter Octal Buffer/Line Driver/Line Receiver, 3-State, Inverting Output Octal Buffer/Line Driver/Line Receiver, 3-State	LS04 LS04 LS14 LS240	*4069 4069 4584	LS/CMOS LS/CMOS LS/CMOS LS	14 14 14 20 20
HC244/	Octal Buffer/Line Driver/Line Receiver,	LS244		LS	20
HCT244 HC365	3-State Hex 3-State Bus Driver with Common 2-Input NOR Enable	LS365A		cuit I SJ tille	0 s16oto
HC366	Hex 3-State Bus Driver with Common 2-Input NOR Enable,	LS366A	nge (- 40°C	Ran(2J ommercial Ra	PA for C
HC367	Inverting Output Hex 3-State Bus Driver with Separate 2-Bit	LS367A	4503	LS/CMOS	16
HC368	and 4-Bit Sections Hex 3-State Bus Driver with Separate 2-Bit and 4-Bit Sections, Inverting Output	LS368A	ication ipeed CMOS gh-Speed Ct	LS right pereth	16
HC540	Octal Buffer/Line Driver/Line Receiver,	LS540	npatible CMC	-	20
HC541	3-State Inverting Outputs Octal Buffer/Line Driver/Line Receiver, 3-State	LS541		LS	20
HC4049 HC4050	Hex Inverting Buffer Hex Buffer		4049 4050	CMOS CMOS	16

High-Speed Device Number MC74/MC54	Functional Course Functional Equivalent Equiv	Functional Equivalent LSTTL Device 74/54	Functional Equivalent CMOS Device MC1XXXX or CDXXXX	Direct Pin Compatibility	Number Pins
SCHMITT TE	RIGGERS		Dentanitore	A SERVER INC	DICK 121 DIL 1
HC14 HC132	Hex Schmitt-Trigger Inverter Quad 2-Input Schmitt-Trigger NAND Gate	LS14 LS132	4584 4093	LS/CMOS LS	14 14
BUS TRANS	CEIVERS		na Output	inverti	000011
HC242	Quad Bus Transceiver, 3-State, Inverting Output	LS242	Type Flip-Fld ng Output	-d lates	10014
HC243 HC245/	Quad Bus Transceiver, 3-State Octal Bus Transceiver, 3-State	LS243 LS245	insperent La Type Flip-Flo	TistLS	20
HCT245 HC640 HC643	Octal Bus Transceiver, 3-State Octal Bus Transceiver, 3-State	LS640 LS643	ial Input/Par	LS LS	20
HC646	Octal Bus Transceiver and Register,	LS646	legister del or Paralla	S H LS	24
HC648	3-State Octal Bus Transceiver and Register, 3-State, Inverting Output	LS648	t Shift Regist Type Registe frectional Ur	-O tigLS	24 1010H
ARITHMETIC	CIRCUITS		legister	Shift R	
HC85 HC181 HC182 HC280	4-Bit Magnitude Comparator 4-Bit Arithmetic Logic Unit Carry Lookahead Generator 9-Bit Odd/Even Parity Generator/Checker	LS85 LS181 LS182 LS280	*4585 4581 4582 *4531	LS LS/CMOS LS/CMOS LS	16 24 16 14
HC283	4-Bit Binary Full Adder with Fast Carry	LS283	4008	e2 rigLs	ea016
HC888 HC4560	NBCD Adder SOA#	ii Shift Regis	4560	CMOS	20 16
MISCELLANE	EOUS			P.	SETMAN
HC292	Programmable Frequency Divider/ Digital Timer	LS292	mable Decar	mergus LS	081016
HC294	Programmable Frequency Divider/ Digital Timer	LS294	mable 4-Bit	Meyno	B1016
HC4046	Phase-Locked Loop	*LS297	4046	CMOS	16
FLIP-FLOPS /	LATCHES		ronous Clear	Synch	
HC73 HC74	Dual J-K Flip-Flop with Reset Dual D-Type Flip-Flop with Set and Reset, Positive-Edge Triggered	LS73A LS74A	*4027 4013	LS LS	14
HC75	4-Bit D-Type Latch	LS75	*4042	muoQLS	16
HC76 HC107	Dual J-K Flip-Flop with Set and Reset Dual J-K Flip-Flop with Reset	LS76A LS107A	*4027 4027	S.Lsette S.LSount	14
HC109	Dual J-K Flip-Flop with Set and Reset, Positive-Edge Triggered	LS109A	*4027	SJal Del	16
HC112	Dual J-K Flip-Flop with Set and Reset, Negative-Edge Triggered	LS112A	*4027	ZJesde	16
HC113	Dual J-K Flip-Flop with Set, Negative-Edge Triggered	LS113) e	10*4027ri8 10# 4027ri8	2 12-Stag	AL 402
HC174	Hex D-Type Flip-Flop with Common Clock and Reset	LS174 sk	19174 9 1926 1926	LS/CMOS	80416
HC175	Quad D-Type Flip-Flop	LS175	4175	LS/CMOS	16
HC259 HC273	8-Bit Addressable Latch Octal D-Type Flip-Flop with Common Clock/Reset	LS259 LS273	*4099 *4175	LS LS	16 20
HC373/ HCT373	Octal D-Type Transparent Latch, 3-State	LS373	nostable Mu	oM IsLS	20
HC374/ HCT374	Octal D-Type Flip-Flop, 3-State	LS374	nostable Mu	M leLS	\$4.20
HC533	Octal D-Type Transparent Latch, 3-State Inverting Output	LS533	cision Retrig	S Dual Pre	20

High-Speed Device Number MC74/MC54	Equivalent Course Punction Placet Punction Punction Punction VXXX or Function VXXX or Funct	Functional Equivalent LSTTL Device 74/54	Functional Equivalent CMOS Device MC1XXXX or CDXXXX	Direct Pin Compatibility	Number of Pins
FLIP-FLOPS/L	ATCHES (continued)			TRIGGERS	TTIMHOR
HC534	Octal D-Type Flip-Flop, 3-State, Inverting Output	LS534	mitt-ringger input Schmit	LS	20
HC563	Octal Transparent Latch, 3-State, Inverting Output	LS576	6150	SCEIVERS	20
HC564	Octal D-Type Flip-Flop, 3-State, Inverting Output	LS580	s Transceive	ua baLS	20
HC573 HC574	Octal Transparent Latch, 3-State Octal D-Type Flip-Flop, 3-State	LS573 LS574	s Transceive a Transceive	LS LS	20 20
SHIFT REGIS	TERS		The many said	1 8	HCT24
HC164	8-Bit Serial Input/Parallel Output Shift Register	LS164	*4034	LS	14
HC165	8-Bit Serial or Parallel Input/Serial Output Shift Register	LS165	*4021	Satist But S	40016
HC173 HC194	4-Bit D-Type Register, 3-State 4-Bit Bidirectional Universal Shift Register	LS173 LS194A	4076 4194	LS/CMOS LS/CMOS	16 16
HC195	4-Bit Universal Shift Register	LS195A	*4035	LS	16
HC299	8-Bit Universal Shift/Store Register, 3-State	LS299	*4094	LS	20
★HC589	8-Bit Parallel-to-Serial Shift Register with Input Latches, 3-State	*LS597	*4014 or*4021		16
HC595	8-Bit Serial-to-Parallel Shift Register, 3-State	LS595	*4034	LS	16
HC597	8-Bit Parallel-to-Serial Shift Register with Input Latches	LS597	*4014 or *4021	A GOSM	16
COUNTERS					
HC160	Programmable Decade Counter, Asynchronous Clear	LS160A	4160	LS/CMOS	16
HC161	Programmable 4-Bit Binary Counter, Asynchronous Clear	LS161A	4161	LS/CMOS	16
HC162	Programmable Decade Counter, Synchronous Clear	LS162A	4162	LS/CMOS	16
HC163	Programmable 4-Bit Binary Counter, Synchronous Clear	LS163A	4163	LS/CMOS LS	16
HC192	Presettable BCD Decade Up/Down Counter	LS192	4510	-C till-A	16
HC193	Presettable 4-Bit Binary Up/Down Counter	LS193	4516	H-LisLS H-LisuC	16 1010H
HC390 HC393 HC4017	Dual Decade Counter Dual 4-Bit Binary Counter Decade Counter/Divider	LS390 LS393	*4518 *4520 4017	LS LS CMOS	16 14 16 16
HC4020	14-Stage Binary Ripple Counter	heren	4020	CMOS	
HC4024 HC4040 HC4060	7-Stage Binary Ripple Counter 12-Stage Binary Ripple Counter 14-Stage Binary Ripple Counter with Oscillator	h Set, gered k and Reset	4024 4040 4060	CMOS CMOS CMOS	16 16
MONOSTARI	E MULTIVIBRATORS	9	Type Flip-Flo	-O bauO a	HC 17E
HC123	Dual Retriggerable Monostable Multivibrator	LS123	*4538 or *4528	SJIII Ad	16
HC221	Dual Monostable Multivibrator	LS221	*4538 or *4528	LS	16
HC423	Dual Monostable Multivibrator	LS423	*4528 or *4528	-G leaLS	16
HC4538	Dual Precision Retriggerable/Resettable Monostable Multivibrator	*LS221	4538	CMOS	16

High-Speed Device Number MC74/MC54	Function	Functional Equivalent LSTTL Device 74/54	Functional Equivalent CMOS Device MC1XXXX or CDXXXX	Direct Pin Compatibility	Number of Pins
DECODERS/	ENCODERS/DISPLAY DRIVERS			PATIBLE DEV	NOO-SUB
HC42 HC137	BCD to 1-of-10 Decoder 1-of-8 Decoder/Demultiplexer with Latched Inputs, Inverting Output	LS42 LS137	*4028 *4028	LS	16 16
HC138/ HCT138	1-of-8 Decoder/Demultiplexer	LS138	*4028	SLS-Sta	16
HC139	Dual 1-of-4 Decoder (Active-Low Outputs)	LS139	4555	LS/CMOS	16
HC147	10-to-4 Priority Encoder	LS147	*4532	nevnLS	16
HC154 HC237	4-to-16 Decoder 1-of-8 Decoder/Demultiplexer	LS154 *LS137	*4514 *4028	TievniLS	24 16
HC4511	with Latched Inputs BCD-to-7-Segment Latch/Decoder/Driver	*(LS46-	4511	LS/CMOS	780H 780H
HC4514 HC4543	Latch/Decoder/Driver 4-Bit Latch/4-to-16 Line Decoder BCD-to-7 Segment Latch/Decoder/Driver for Liquid-Crystal Displays	*(LS46- LA49)	4514 4543	CMOS CMOS	24 16
DIE COMPA	TIBLE DEVICES	0.01010 C - 1			HC643
		10470		L C/CMOC	1
HC173 HC240/ HCT240	4-Bit D-Type Register, 3-State Octal Buffer/Line Driver/Line Receiver, 3-State, Inverting Output	LS173 LS240	4076	LS/CMOS LS	16 20
HC241/ HCT241	Octal Buffer/Line Driver/Line Receiver, 3-State	LS241	e DEVICES	LS LS	20
HC242	Quad 3-State Bus Transceiver, Inverting Output	LS242	egoder/Dem	18-16LS	14
HC243	Quad 3-State Bus Transceiver	LS243	poinsynt a	LS	14
HC244/ HCT244	Octal Buffer/Line Driver/Line Receiver, 3-State	LS244	ffeetLine Dri	SJ tar LS	20
HC245/ HCT245 HC251	Octal Bus Transceiver, 3-State 8-Input Multiplexer, 3-State	LS245	*4512	18 le LS 18 le LS	16
HC253 HC257	Dual 4-Input Multiplexer, 3-State Quad 2-Input Data Selector/Multiplexer, 3-State	LS253 LS257	*4539 *4519	LS/CMOS LS	16 16
HC299	8-Bit Universal Shift/Store Register, 3-State	LS299	*4094	LS LS	20
HC354 HC356 HC365	8-Input Multiplexer, 3-State 8-Input Multiplexer, 3-State Hex 3-State Bus Driver with Common 2-Input NOR Enable	LS354 LS356 LS365A	*4512 *4512	LS	20 20 16
HC366	Hex 3-State Bus Driver with Common 2-Input NOR Enable, Inverting Output	LS366A	ng Output Vultiplexer,	to May 10	16 HC25
HC367	Hex 3-State Bus Driver with Separate 2-Bit and 4-Bit Sections	LS367A	4503	LS/CMOS	16
HC368	Hex 3-State Bus Driver with Separate 2-Bit and 4-Bit Sections, Inverting Output	LS368A	Input Multipl Multiplexer, Multiplexer,	zuenl-8	16
HC373/ HCT373	Octal Transparent Latch, 3-State	LS373	alog Switch	AbaLS	20
HC374/ HCT374	Octal D-Type Flip-Flop, 3-State	LS374	lexer/Demul	S-Cham	20
HC533	Octal D-Type Transparent Latch, 3-State, Inverting Output	LS533	lexer/Demul		20 2040H
	4066 CMOS	rexelqi	lexer/Demul		HC408

High-Speed Device Number MC74/MC54	Misser Company of Function of Variation of State	Functional Equivalent LSTTL Device 74/54	Functional Equivalent CMOS Device MC1XXXX or CDXXXX	Direct Pin Compatibility	Number Pins
BUS-COMPA	TIBLE DEVICES (continued)				
HC534	Octal D-Type Flip-Flop, 3-State, Inverting Output	LS534	1-of-10 Dec lecoder/Dem	of CLS	20
HC540	Octal Buffer/Line Driver/Line Receiver, 3-State Inverting Outputs	LS540	atched Inpu	i risiwLS	20
HC541	Octal Buffer/Line Driver/Line Receiver, 3-State	LS541	lecoder/Dem		20
HC563	Octal Transparent Latch, 3-State, Inverting Output	LS576	e-Low Outp	10-01-0	20
HC564	Octal D-Type Flip-Flop, 3-State, Inverting Output	LS580	Decoder Den	ar-olLS 18-to-1	20
HC573	Octal Transparent Latch, 3-State	LS573	atched inpu	HaiwLS	20
HC574	Octal D-Type Flip-Flop, 3-State	LS574	7-Segment	-of-CLS	20
★HC589	8-Bit Parallel-to-Serial Shift Register	*LS597	*4014 or	Latch	16
HC595	with Input Latches, 3-State 8-Bit Serial-to-Parallel Shift Register,	LS595	*4021 *4034	The second secon	16
HC640	3-State Octal Bus Transceiver, 3-State	LS640	Decoder/Dri		20
HC643	Octal Bus Transceiver, 3-State	LS643	2000	AG LS TAN	20
HC646	Octal Bus Transceiver, 3-State Octal Bus Transceiver and Register, 3-State	LS646	Type Registe	-O 118LS	24
HC648	Octal Bus Transceiver and Register, 3-State	LS648	Her/Line Dri te, inverting	LS	24
TTL INPUT C	OMPATIBLE DEVICES	DEM BUILDINGS	ST SELL VISIT	9-540	ACTOH-
HCT138	1-of-8 Decoder/Demultiplexer	LS138	*4028	DOLS	16
HCT240	Octal Buffer/Line Driver/Line Receiver, 3-State, Inverting Output	LS240	T eug eiser	Tievn LS	20
HCT241	Octal Buffer/Line Driver/Line Receiver, 3-State	S LS241	ffer/Line Dri	A Star	20
HCT244	Octal Buffer/Line Driver/Line Receiver, 3-State	LS244	s Transceive	The second secon	20
HCT245	Octal Bus Transceiver, 3-State	LS245	Multiplexer,	tugnES	20
НСТЗ73	Octal D-Type Transparent Latch, 3-State	LS373	nput wurtiph Input Data S	S LS	20
НСТЗ74	Octal D-Type Flip-Flop, 3-State	LS374	9.	LS	20
MULTIPLEXE	RS (ANALOG AND DIGITAL)				
HC151	8-Channel Digital Multiplexer	LS151	*4512	LS	16
HC153	Dual 4-Channel Digital Multiplexer	LS153	4539	LS/CMOS	16
HC157	Quad 2-Input Data Selector/Multiplexer	LS157	*4519	S.E. LS	16
HC158	Quad 2-Input Data Selector/Multiplexer, Inverting Output	LS158	iommon 2-Ir tete Bus Driv	RAMINA C	16
HC251	8-Input Multiplexer, 3-State	LS251	*4512	LS	16
HC253	Dual 4-Input Multiplexer, 3-State	LS253	*4539	LS/CMOS	16
HC257	Quad 2-Input Data Selector/Multiplexer, 3-State	LS257	*4519	S-E xLS	as:16
HC298	Quad 2-Input Multiplexer with Storage	LS298	rete Bus Drh	B-E KLS	188016
HC354	8-Input Multiplexer, 3-State	LS354	*4512	18-SLS	20
HC356	8-Input Multiplexer, 3-State	LS356	*4512	nevnLS	20
HC4016 HC4051	Quad Analog Switch 8-Channel Analog	tch, 3-State	4016 4051	CMOS	14 16
HC4052	Multiplexer/Demultiplexer 8-Channel Analog Multiplexer/Demultiplexer	ip, 3-State	4052	CMOS	16
HC4053	8-Channel Analog Multiplexer/Demultiplexer	Dutput	4053	CMOS	16
HC4066	Quad Analog Switch		4066	CMOS	14

High-Speed Device Number MC74/MC54	Function	Functional Equivalent LSTTL Device 74/54	Functional Equivalent CMOS Device MC1XXXX or CDXXXX	Direct Pin Compatibility	Number of Pins
MULTIPLEXE	RS (ANALOG AND DIGITAL) (continued)				
★HC4316	Quad Analog Switch with Level Translator	us to at	*4016	ouhortol ai	16
★HC4351	Quad Analog Multiplexer/Demultiplexer with Latched Select Inputs	es. 4 par	*4051	m 600 to	18
★HC4352	Dual 4-Channel Analog Multiplexer/Demultiplexer with Latched Select Inputs		*4052	es of the r	18 ⁵
★HC4353	Triple 2-Channel Analog Multiplexer/Demultiplexer with Latched Select Inputs	JT.	*4053	speed sim wer consulot CMOS	Low po

Output drive capability of 10 LSTTL loads

e Simple design procedure

Design of the gate arrays is a very simple procedure, using the Motorola CAD system. This system has all of the design aids necessary for the designer to simulate his design, automatically place and route the circuit, complete an accurate timing analysis and present a test program for testing the finished product.

The CAD system is an improved version of the system which has been successfully used for several years for the design of Motorola ECL and TTL Macrocell Arrays. The same design system can be used for all three technologies. The designer needs no knowledge of I.C. design or computer programming to design a Motorola Gate Array.

The designer works in his own office using a simple printing terminal with Modem or acoustic coupler, and connects to the Motorola computer by dialling the nearest Motorola Sales Office. From here, connection to the Motorola computer in Phoenix, Arizona, is over the Motorola worldwide communications network.

Using a comprehensive library of SSI and MSI functions, the designer describes his circuit as a list of functions and interconnections which then becomes the input to the CAD system.

Future plans include the addition of analog and memory functions, and using a 2µ HCMOS process which will increase speed.

For further information on the Motorola range of CMOS, TTL and ECL Arrays, contact your nearest Motorola Sales Office.

MOS GATE ARRAYS

Motorola is introducing a range of 3μ High-Density CMOS Gate Arrays, with gate counts from 600 to 6000 gates. 4 parts will be introduced in 1983 and 2 more in 1984.

Key features of the range are:

- System speed similar to LSTTL
- Low power consumption
- Option of CMOS or LSTTL compatible inputs
- Output drive capability of 10 LSTTL loads
- Simple design procedure

Design of the gate arrays is a very simple procedure, using the Motorola CAD system. This system has all of the design aids necessary for the designer to simulate his design, automatically place and route the circuit, complete an accurate timing analysis and prepare a test program for testing the finished product.

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Future plans include the addition of analog and memory functions, and using a 2μ HCMOS process which will increase speed.

For further information on the Motorola range of CMOS, TTL and ECL Arrays, contact your nearest Motorola Sales Office.

B AND UB SERIES CMOS FAMILY DATA

The CMOS Devices in this volume which have a B or UB suffix meet the minimum values for the industry-standardised" family specification. These standardised values are shown in the Maximum Ratings and Electrical Characteristics Tables, in addition to a standard minimum specification for characteristics the B/UB devices feature:

- e 3-18 vott operational limits
- Capable of driving two low-power TTL leads, one low-power Schottley TTL lead, or two HTL leads over the reted temperature range

B-Series Family Data

Paremeters specified at 5.0, 10, and 15 volt suppl

2.0 V min 9 0.0 V supply 2.5 V min 9 15 V supply

The Industry-standardized maximum ratings and recommended operating range are shown at the bottom of this page. Limits for the static characteristics are shown in two formats: Table 1 is in the industry format and Table two format. The Motorola format is used throughout this data book. Additional specification values are shown on the individual data

Switching characteristics for the B and UB saries devices are specified under the following conditions:

Losd Capacitance, CL, of 50 pF

Load Resistance, R., of 200 K C

input pulse voltage equal to + VDD supply voltage input ouise rise and fall times of 20 ps

Propagation Delay times measured from 50% point of input voltage to 50% point of output voltage.

V 81 bas 07 8 sensitor vious tensitib soulT

Exceptions to the B and UB Series Family Specification.
There are a number of devices which have a B or UB suffix whose input and/or outputs very somewhat from the family specification because of functional requirements. Some catterprise of notable exceptions are:

Devices with specialized outputs on the oblg, such as NPN emitter-follower drivers or transmission gates do not meet cutter reasilizations.

Devices with specialized inputs, such as oscillator

femur Voltoge

The input voltage specification is interpreted as the wonst-case input voltage to produce an output level of "1" of "0". The "1" or "0" output level is defined as a deviation from the supply (Vpp) and ground (Vsp) levels. For a 5.0 V supply, this deviation is 0.5 V; for a 10 V supply, 1.0 V; and for 15 V, 1.5 V. As an exemple, in a device operating at a 5.0 V supply, the device with the input starting at ground is guaranteed to switch on an before 3.5 V and not to switch up to witch on a before 3.5 V and not the switching are defined as witchin 0.5 V of the ideal output level for the example with a 5.0 V supply. The actual switching level reterred to the input it between 1.5 V and 3.5 V.

Noise Margin

The values for input voltage and the given defined coupout deviation lead to minimum noise margins of 1.0 V, 2.0 V; and 2.5 V for a 5.0 V, 10 V, and 15 V supply, respectively.

Dutout Briss Current

Devices in the 8 Series are capable of sinking a minimum of 0.36 mA over the temperature range with a 5.0 V supply. This value guarantees that these CMOS devices will drive one Schottky low-power TTL Input.

8 Series vs UB CMDS

The primary difference between B series and UB series devices is that UB series genes and inverters are constructed with a single inverting stage between input and output. The ducreased gain caused by using a single stage results in less noise immunity and a transfer characteristic that is toss ideal.

The decreased gain is quite useful when CMOS Gates and inverters are used in a "Linear" mode to form oscillators, monostables or amplifiers. The decreased gain factors increased stability and a "cleaner" output weedlamn, in addition to linear operation, the UB gates and inverters offer an increase in speed since only a single state is involved.

The B series U3 CMOS, and devices with no suffix can be used interchangeably in digital circuits that interface to other CMOS devices.

MAXIMUM BATHIGS (Voltages referenced to Vee)

-65 to +150	

ECOMMENDED DPERATING BANGE

Specifications coordinated by ETA/JEDEC Bolid State Products Council.

2

The CMOS Devices in this volume which have a B or UB suffix meet the minimum values for the industry-standardized* family specification. These standardized values are shown in the Maximum Ratings and Electrical Characteristics Tables. In addition to a standard minimum specification for characteristics the B/UB devices feature:

- 3-18 volt operational limits
- Capable of driving two low-power TTL loads, one low-power Schottky TTL load, or two HTL loads over the rated temperature range
- Maximum input current of ±1 µA at 15 volt power supply over the temperature range
- Parameters specified at 5.0, 10, and 15 volt supply
- Noise margins of 1.0 V min @ 5.0 V supply

2.0 V min @ 10 V supply 2.5 V min @ 15 V supply

The industry-standardized maximum ratings and recommended operating range are shown at the bottom of this page. Limits for the static characteristics are shown in two formats: Table 1 is in the industry format and Table 2 is in the equivalent Motorola format. The Motorola format is used throughout this data book. Additional specification values are shown on the individual data sheets.

Switching characteristics for the B and UB series devices are specified under the following conditions:

Load Capacitance, C_L , of 50 pF Load Resistance, R_L , of 200 K Ω

Input pulse voltage equal to +V_{DD} supply voltage Input pulse rise and fall times of 20 ns

Propagation Delay times measured from 50% point of input voltage to 50% point of output voltage

Three different supply voltages: 5, 10, and 15 V

Exceptions to the B and UB Series Family Specification

There are a number of devices which have a B or UB suffix whose input and/or outputs vary somewhat from the family specification because of functional requirements. Some categories of notable exceptions are:

Devices with specialized outputs on the chip, such as NPN emitter-follower drivers or transmission gates, do not meet output specifications.

Devices with specialized inputs, such as oscillator inputs, have unique input specifications.

Input Voltage

The input voltage specification is interpreted as the worst-case input voltage to produce an output level of "1" or "0". The "1" or "0" output level is defined as a deviation from the supply (VDD) and ground (VSS) levels. For a 5.0 V supply, this deviation is 0.5 V; for a 10 V supply, 1.0 V; and for 15 V, 1.5 V. As an example, in a device operating at a 5.0 V supply, the device with the input starting at ground is guaranteed to switch on or before 3.5 V and not to switch up to 1.5 V. Switching and not switching are defined as within 0.5 V of the ideal output level for the example with a 5.0 V supply. The actual switching level referred to the input is between 1.5 V and 3.5 V.

Noise Margin

The values for input voltage and the given defined output deviation lead to minimum noise margins of 1.0 V, 2.0 V, and 2.5 V for a 5.0 V, 10 V, and 15 V supply, respectively.

Output Drive Current

Devices in the B Series are capable of sinking a minimum of 0.36 mA over the temperature range with a 5.0 V supply. This value guarantees that these CMOS devices will drive one Schottky low-power TTL input.

B Series vs UB CMOS

The primary difference between B series and UB series devices is that UB series gates and inverters are constructed with a single inverting stage between input and output. The decreased gain caused by using a single stage results in less noise immunity and a transfer characteristic that is less ideal.

The decreased gain is quite useful when CMOS Gates and inverters are used in a "Linear" mode to form oscillators, monostables or amplifiers. The decreased gain results in increased stability and a "cleaner" output waveform. In addition to linear operation, the UB gates and inverters offer an increase in speed since only a single stage is involved.

The B series, UB CMOS, and devices with no suffix can be used interchangeably in digital circuits that interface to other CMOS devices.

MAXIMUM RATINGS (Voltages referenced to VSS)

Rating	Symbol	Value	Unit
DC Supply Voltage	VDD	-0.5 to +18	Vdc
Input Voltage, All Inputs	Vin	-0.5 to V _{DD} + 0.5	Vdc
DC Current Drain per Pin	1	10	mAdo
Operating Temperature Range AL Device CL/CP Device	TA	-55 to +125 -40 to +85	°C
Storage Temperature Range	T _{stg}	-65 to +150	°C

RECOMMENDED OPERATING RANGE

DC Supply Voltage	VDD	+3.0 to +15	Vdc

^{*}Specifications coordinated by EIA/JEDEC Solid-State Products Council.

TABLE 1 - EIA/JEDEC FORMAT FOR CMOS INDUSTRY B AND UB SERIES SPECIFICATIONS AT

ELECTRICAL CHARACTERISTICS

PARAMETER		TEMP VDD		Town Y SECOND	LIMITS						
		RANGE (Vdc)	CONDITIONS	TLO	OW°	+ 2	5°C	THIGH		UNITS	
		MAINGE	(Age)	KIDST BYTE	Min	Max	Min	Max	Min	Max	
IDD	Quiescent Device Current GATES	Mil	5 10 15	Vin = VSS or VDD	$^{4.6V}_{1N} = 0$ $^{4.6V}_{1N} = 0$ $^{4.6V}_{1N} = 0$	0.25 0.5 1.0	31	0.25 0.5 1.0	10931	7.5 15 30	μAdc
	\$1.0-	Comm	5 10 15	All valid input combinations	V1N = 0	1.0 2.0 4.0	er e	1.0 2.0 4.0		7.5 15 30	μAdo
35A	0.1-	Mil	5 10 15	VIN = VSS or VDD	0 = m/V /3.51 -	1.0 2.0 4.0	27	1.0 2.0 4.0		30 60 120	μAdo
Ade	BUFFERS, FLIP-FLOPS	Comm	5 10 15	All valid input combinations	10.0 =	4 8 16	er er n	4.0 8.0 16.0	tni	30 60 120	μAdo
Ads	112.	Mil	5 10 15	VIN = VSS or VDD	no 0 m	5 10 20	as n	5 10 20	many	150 300 600	μAdo
	MSI	Comm	5 10 15	All valid input combinations	-40°C	20 40 80	net ren rature r	20 40 80	esatiliki viliki sa	150 300 600	μAdo
VOL	Low-Level Output Voltage	All	5 10 15	VIN = VSS or VDD		0.05 0.05 0.05	, engryp	0.05 0.05 0.05	region siens	0.05 0.05 0.05	Vdc
Vон	High-Level Output Voltage	All	5 10 15	VIN = VSS or VDD	4.95 9.95 14.95	R TAI	4.95 9.95 14.95	ROLA	4.95 9.95 14.95	2-1	Vdc
VIL	Input Low Voltage # B Types	Allas	5 10 15	V _O = 0.5V or 4.5V V _O = 1.0V or 9.0V V _O = 1.5V or 13.5V II _O < 1µA	myš	1.5 3.0 4.0	801	1.5 3.0 4.0	ARÁC	1.5 3.0 4.0	Vdc
VIL	Input Low Voltage # UB Types	All	5 10 15	V _O = 0.5V or 4.5V V _O = 1.0V or 9.0V V _O = 1.5V or 13.5V II _O I < 1µA	5∀	1.0 2.0 2.5	0.,	1.0 2.0 2.5		1.0 2.0 2.5	Vdc
VIH	Input High Voltage# B Types	All 8	5 10 15	V _O = 0.5V or 4.5V V _O = 1.0V or 9.0V V _O = 1.5V or 13.5V II _O < 1µA	3.5 7.0 11.0	level.	3.5 7.0 11.0		3.5 7.0 11.0	20V 101	Vdc
VIH	Input High Voltage# UB Types	O All	5 10 15	V _O = 0.5V or 4.5V V _O = 1.0V or 9.0V V _O = 1.5V or 13.5V II _O < 1µA	4.0 8.0 12.5	Type I	4.0 8.0 12.5	*	4.0 8.0 12.5	0 to 0.8 1 to 0.8 13.5 or	Vdc
lor	Output Low (Sink) Current	- 0	5	V _O = 0.4V, V _{IN} = 0 or 5V V _O = 0.5V,	0.64		0.51		0.36	0.5 or 4.0 0 or 9.0 1.5 or 1	(Vo 1.
2012	- 1,0 - 2,0 - 2,5	Mil 0.1 0.3	10	V _{IN} = 0 or 10V V _O = 1.5V, V _{IN} = 0 or 15V V _O = 0.4V,	4.2	Lawel	3.4		0.9	1.5 or 0.6 1.5 or 0.6 1.6 or 1.	mAde
3bV	4.0 - 8.0 - 12.6 -	Com	5 10	V _{IN} = 0 or 5V V _O = 0.5V, V _{IN} = 0 or 10V V _O = 1.5V,	0.52	Isvad 1	1.1		0.36	A 10.8.0	mAde
6631	T Taxi		15	V _{IN} = 0 or 15V	3.6		3.0		2.4	if to d.1	

		TENED	.,				LIN	IITS			
8739	PARAMETER	RANGE	V _{DD} (Vdc)	CONDITIONS	TLO	ow*	+ 25°C		THIGH*		UNITS
	note miss	HANGE	(vac)	23 T sale	Min	Max	Min	Max	Min	Max	
IOH зыла	Output High (Source) Current	85.0 8.0 0. Mil	5	V _O = 4.6V, V _{IN} = 0 or 5V V _O = 9.5V, V _{IN} = 0 or 10V V _O = 13.5V,	-0.25 -0.62	nlV	-0.2	LING	-0.14 -0.35	intopoli O solvei	mAdo
	7.6	1.0	15	V _{IN} = 0 or 15V	-1.8	um I	-1.5	10	-1.1		
abAs	18 20 30	2.0	5	V _O = 4.6V, V _{IN} = 0 or 5V	-0.2	non	-0.16	meQ.	-0.12		
nbA:	30 80 120	Com	10 15	V _O = 9.5V, V _{IN} = 0 or 10V V _O = 13.5V V _{IN} = 0 or 15V	-0.5 -1.4	No.	-0.4 -1.2	ISM!	-0.3 -1.0		mAdd
IIN	Input Current	Mil Comm	15 15	V _{IN} = 0 or 15V V _{IN} = 0 or 15V	neltecid	±0.1 ±0.3	01 10	±0.1 ±0.3	1011-41	±1.0 ±1.0	μAdo μAdo
loz	3-State Output Leakage Current	Mil	15 15	V _{IN} = 0 or 15V V _{IN} = 0 or 15V		±0.4 ±1.6	8	±0.4 ±1.6		±12 ±12	μAdo
CIN	Input Capacitance per unit load	All		Any Input	000		ar L	7.5			pF

 $^{^{}m eT}_{LOW}$ = $-55^{
m oC}$ for Military temperature range device, $-40^{
m oC}$ for Commercial temperature range device. THIGH = $+125^{
m oC}$ for Military temperature range device, $+85^{
m oC}$ for Commercial temperature range device.

#Applies for Worst Case input combinations.

TABLE 2 - MOTOROLA FORMAT FOR CMOS INDUSTRY B AND UB SERIES SPECIFICATIONS

DDV . U.I	3.0 1	3.12
	Characteristic	1 -

0.5	4.0			Tio	w*	25	°C	Thi	gh*	
istic	0.4	Symbol	Vdc	Min	Max	Min	Max	Min	Max	Unit
	"0" Level	VOL	5.0 10 15	V(E) = V(E) = A(E) =	0.05 0.05 0.05		0.05 0.05 0.05	-kag	0.05 0.05 0.05	Vdc
	"1" Level	VOH	5.0 10 15	4.95 9.95 14.95	0V- 0V-	4.95 9.95 14.95	IIA-	4.95 9.95 14.95	-250 olo∀ ng omou T	Vdc
	"0" Level	VIL		Aut >	nu L					Vdc
	4.0 8.0 12.5	4.0 8.0 12.5	10	V9H =		-	1.5 3.0 4.0	- -0 (s)	1.5 3.0 4.0	H 1417
	"1" Level	VIH		Aut >	oli J					Vdc
	18.0	0.64	5.0 10 15	3.5 7.0 11.0	ov-	3.5 7.0 11.0	-	3.5 7.0 11.0		
	"0" Level	O. VIL	5.0	V&U -	1.0		1.0	-	1.0	Vdc
	-		15	V3-0 -	2.5	-	2.5	-	2.5	
	"1" Level	V _{IH}	5.0 10	4.0 8.0	0V-	4.0 8.0	-Con	4.0 8.0	-	Vdc
	O.S. S.S.	"0" Level "0" Level "1" Level	"1" Level VIL "1" Level VIL "1" Level VIL "1" Level VIL	"1" Level VIL 5.0 "10" Level VIH 5.0 "10" Level VIL 5.0	Symbol VDD Vdc Min	Symbol VDD Vdc Min Max	Symbol VDD Vdc Min Max Min M	Symbol VDD Vdc Min Max Min M	Vode	Note

Charact	eristic			Symbol	VDD	Tlo	w	25	piggin	Thi	jh	Unit
Min lites	Hadd.	oiNi	Mak	nin i	Vdc	Min	Max	Min	Max	Min	Max	0
Output Drive Current (AL)	B Gates	-	0.1	- ГОН	a T	ogt		100	ens Cus	or Outest	Tu6 bas	mAd
(VOH = 2.5 Vdc)	Source			- 1	5.0	-1.2	-	-1.0	G .HA)	-0.7	(e g ula)	
(VOH = 4.6 Vdc)				- 1	5.0	-0.25	-	-0.2	-	-0.14	-	
(V _{OH} = 9.5 Vdc)	4.0			-	10	-0.62	- 1	-0.5	07.70)	-0.35	-	
(V _{OH} = 13.5 Vdc)				- 1	15	-1.8	,-	-1.5	, -	-1.1	-	
(VOL = 0.4 Vdc)	Sink			- IOL	5.0	0.64		0.51	-	0.36	-	mAd
(VOL = 0.5 Vdc)					10	1.6	-	1.3	O JAI	0.9	Conff Con	St Clube
(VOL = 1.5 Vdc)				- 1	15	4.2	-	3.4	-	2.4	(episto)	
Output Drive Current (CL/	CP) B Gat	es	28	ІОН	1							mAd
(VOH = 2.5 Vdc)	Source				5.0	-1.0	-	-0.8	(CL)(C	-0.6	-	
(VOH = 4.6 Vdc)					5.0	-0.2	-	-0.16	-	-0.12	-	
(VOH = 9.5 Vdc)				-	10	-0.5	-	-0.4	-	-0.3	-	
(VOH = 13.5 Vdc)				-	15	-1.4	-	-1.2	-	-1.0	T	ALION II
(VOL = 0.4 Vdc)	Sink			IOL	5.0	0.52		0.44	0	0.36	10 TO 2	mAd
(VOL = 0.5 Vdc)				1	10	1.3	O CO	1.1	09- ,0	0.9	128FC 16	MIC
(VOL = 1.5 Vdc)					15	3.6	SIG YOU	3.0	100, 100	2.4	128°C 16	
Output Drive Current (AL)	LIR Gates			ГОН		.075217-iss	100 000 F		MANUAL T	DEVISOR OF THE PERSON NAMED IN		mAc
(VOH = 2.5 Vdc)	Source			HO	5.0	-1.2	m obv. G	-1.0		-0.7	d to nig	mAc
(V _{OH} = 4.6 Vdc)	Source				5.0	-0.25	W STAN II	-0.2	_	-0.14		
					10	-0.62	n appr d	-0.5	_	-0.35		
(V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc)					15	-1.8		-1.5		-1.1	_	
(VOL = 0.4 Vdc)	0:-1-			1		0.64		0.51		0.36		mAd
	Sink			IOL	5.0		-		_		-	mAd
(VOL = 0.5 Vdc)					10	1.6		1.3	_	0.9		
(V _{OL} = 1.5 Vdc)				1	15	4.2		3.4		2.4		-
Output Drive Current (CL)		ates		ІОН								mAd
$(V_{OH} = 2.5 \text{ Vdc})$	Source				5.0	-1.0	-	-0.8	- 1	-0.6	-	
$(V_{OH} = 4.6 \text{ Vdc})$					5.0	-0.2	-	-0.16	-	-0.12	-	
$(V_{OH} = 9.5 \text{ Vdc})$					10	-0.5	-	-0.4	-	-0.3	- 7	
(V _{OH} = 13.5 Vdc)					15	-1.4	-	-1.2	-	-1.0	-	
(VOL = 0.4 Vdc)	Sink			IOL	5.0	0.52	-	0.44	-	0.36	-	mAd
(VOL = 0.5 Vdc)					10	1.3	- 1	1.1	-	0.9	-	
(VOL = 1.5 Vdc)					15	3.6	-	3.0	-	2.4	-	
Output Drive Current (AL)	Other De	vices		ТОН								mAd
(VOH = 4.6 Vdc)	Source				5.0	-0.25	-	-0.2	-	-0.14	-	
(VOH = 9.5 Vdc)					10	-0.62	10-	-0.5	-	-0.35	-	
(VOH = 13.5 Vdc)					15	-1.8	-	-1.5	-	-1.1	-	
(VOL = 0.4 Vdc)	Sink			IOL	5.0	0.64	-	0.51	-	0.36	-	mAd
(VOL = 0.5 Vdc)				0.	10	1.6	_	1.3		0.9		
(VOL = 1.5 Vdc)					15	4.2	_	3.4	-	2.4	-	
Output Drive Current (CL/	CP) Other	Device	s	ТОН	1	1	-					mAd
(V _{OH} = 4.6 Vdc)	Source			Un	5.0	-0.2	_	-0.12	-	-0.12	-	
(VOH = 9.5 Vdc)				100	10	-0.5	_	-0.4	-	-0.3	-	
(VOH = 13.5 Vdc)					15	-1.4	-	-1.2	-	-1.0	-	
(V _{OL} = 0.4 Vdc)	Sink			IOL	5.0	0.52	_	0.44	_	0.36	-	mAd
(V _{OL} = 0.5 Vdc)				-OL	10	1.3	_	1.1	_	0.9		.mett
(V _{OL} = 1.5 Vdc)					15	3.6		3.0	_	2.4		
Input Current (AL Device)				lin	15	-	±0.1	-	±0.1	-	±1.0	μΑο
Input Current (CL/CP Dev				-	15	+-	±0.1	_	±0.1		±1.0	μΑο
	100/			lin		1				-		1
nput Capacitance (Vin = 0)				Cin	-	-	-	-	7.5	-	Ī	pF
Gate Quiescent Current	(AL De	vice)		IDD	5.0	+	0.25	-	0.25	_	7.5	μΑσ
(Per Package)				.00	10	-	0.5	_	0.5		15	pa-10
					15	-	1.0	-	1.0		30	
	(CL/CP	Davies		Inn	5.0	-	1.0		1.0		7.5	
	(CL/CP	Device)		IDD	10		2.0		2.0	_	15	μΑο

	* 4	id?	1 25°C 1	1	T	VDD	Tic	w	25	°C	Th	igh "	
SINU	xulià	Characte	eristic	naMi l	Symbol	Vdc	Min	Max	Min	Max	Min	Max	Unit
Flip-Flop	and Buf	fer Quies	cent Current		IDD	5.0	1101 -	1.0	-	1.0	11/4/11	30	μAdc
(Per Pa	ackage)		(AL Device)		5.1-	0.8 10	-	2.0	-	2.0	-	60 ·	HOV)
					0.25	15	-	4.0	-	4.0	-	120	HOV)
			(CL/CP Device)		IDD	5.0	-	4.0	-	4.0	-	30	μAdc
			- 151-		8.1- 1	10	-	8.0	-	8.0	_(a	60	HOV
obAm		0.36	- f8.0	-	0.64	8 15	101-	16	-	16	-	120	(VOL)
MSI Quie	scent Cu	rrent	(AL Device)	-	a I IDD	5.0	-	5.0	-	5.0	-	150	μAdo
(Per Pa	ackage)	8.5	3.4		6.2	10	-	10	-	10	-	300	TOAL
						15	HOI -	20	-08	20	NJOL n	600	O tuquid
			(CL/CP Device)	- 1	IDD	5.0	-	20	-	20	-	150	μAdo
					-0.2	10	-	40	-	40	-	300	HOV)
			- 0.0-		8.0- T	15	-	80	-	80	-	600	HOV)
LSI Quies	cent Cur	rent			IDD			See	Individu	al Data S	Sheets.	DV 8.51	HOAL

* T_{low} = -55°C for AL Device, -40°C for CL/CP Device. T_{high} = +125°C for AL Device, +85°C for CL/CP Device. #Noise immunity specified for worst-case input combination. Noise Margin for both "1" and "0" level = 1.0 Vdc min @ VDD = 5.0 Vdc 2.0 Vdc min @ VDD = 10 Vdc 2.5 Vdc min @ VDD = 15 Vdc Squrca 1VOH = 4.5 Vdc1 1.6 (VOH = 9.5 Vdc)

MC14000UB

DUAL 3-INPUT "NOR" GATE PLUS INVERTER

The MC14000UB dual 3-input MOR gate plus inverter is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These complementary MOS look gates find primary use where low power dissipation and/or high noise immunity is desired.

- Ouisscent Current = 0.5 nA typ/pkg @ 5 Vdc
 - Noise Immunity = 45% of Voo typical
 - Diede Protection on All Inputs
 - w Supply Voltage Range = 3.0 Vdc to 18 Vdc

Data Sheets

- Total and State and State
 - Logic Swing Independent of Fanout
- Pin-for-Pin Replacement for CD4000UB

CMOS SSI

COMPONER COMPLEMENTARY MOST

DUAL 3-INPUT "NOR" GATE PLUS INVERTER



P SUFFIX

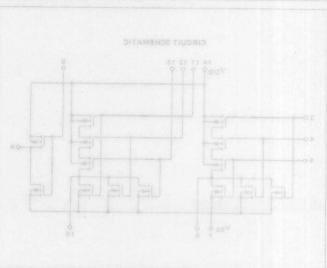
L SUPFIX SEADMIC PACKAGE CASE 632

CASE INFORMATION

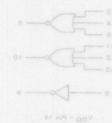
C Lamino Packaga
Plastic Packaga
Extended Operating
"Imperature Plange
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MAXIMUM RATINGS (Voltages referenced to Vigs

AT	











MC14000UB

DUAL 3-INPUT "NOR" GATE PLUS INVERTER

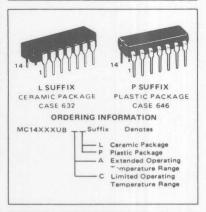
The MC14000UB dual 3-input NOR gate plus inverter is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These complementary MOS logic gates find primary use where low power dissipation and/or high noise immunity is desired.

- Quiescent Current = 0.5 nA typ/pkg @ 5 Vdc
- Noise Immunity = 45% of Vpp typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Single Supply Operation Positive or Negative
- High Fanout > 50
- Input Impedance = 10^{12} ohms typical
- Logic Swing Independent of Fanout
- Pin-for-Pin Replacement for CD4000UB

CMOS SSI

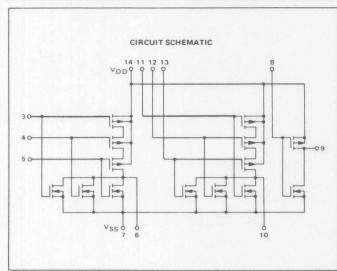
(LOW-POWER COMPLEMENTARY MOS)

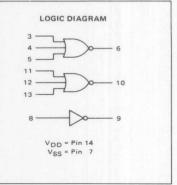
DUAL 3-INPUT "NOR" GATE PLUS INVERTER

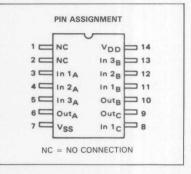


MAXIMUM RATINGS (Voltages referenced to VSS)

Rating	Symbol	Value	Unit
DC Supply Voltage	VDD	-0.5 to +18	Vdc
Input Voltage, All Inputs	Vin	-0.5 to V _{DD} +0.5	Vdc
DC Current Drain per Pin	1	10	mAdc
Operating Temperature Range AL Device CL/CP Device	TA	-55 to +125 -40 to +85	оС
Storage Temperature Range	T _{stq}	-65 to +150	°C







		0154	GGV 3	VDD	Tie	ow*		25°C	Charac	Th	igh *	
Charact			Symbol	Vdc	Min	Max	Min	Тур	Max	Min	Max	Unit
Output Voltage	081"0	Level	VOL	5.0	-	0 05	-	0	0.05	+ 15 (%	0.05	Vdc
Vin VDD or 0			01	10		0.05	4	0	0.05	6 15 (%)	0.05	FILE.
130			01	15	-	0.05	-	0	0.05	519	0.05	ALJT7
		Level	VOH	5.0	4.95		4.95	5.0		4.95	omiT lis	Vdc
Vin O or VDD				10	9.95	-	9 95	10		9.95	en (T.S ne	TURSTUL
002			- 0,8	15	14.95		14.95	15	an 65	14.95	ar 701	HITT.
Input Voltage#	0.,0	" Level	VIL						Q films	JO (Role	a 88.01 =	Vdc
(VO = 4.5 Vdc)			100-	50	-	1.0	-	2.25	1.0	-	1.0	1866001 ⁶
(VO = 9.0 Vdc)				10		2.0		4.50	2.0	200731	2.0	
(VO = 13.5 Vdc)			8,8	15	-	2.5		6.75	2.5	1. Yns/pF	2.5	1783
	08."1	" Level	VIH			1 8 1		1 10	1 C1 + 18	3.50 ne/or	- THAT	1250
$(V_0 = 0.5 \text{ Vdc})$			-	5.0	4.0	-	4.0	2.75		4.0	-	Vdc
$(V_0 = 1.0 \text{ Vdc})$				10	8.0	1 100	8.0	5.50	end to ex	8.0	avig <u>s</u> alum	The for
$(V_0 = 1.5 \text{ Vdc})$				15	12.5		12.5	8.25	-	12.5	-	
Output Drive Current	IAL Dev	ice)	10Н									mAdc
(VOH - 2.5 Vdc)	Sou	irce		5.0	-1.2		-1.0	-1.7		-0.7		
(VOH 4.6 Vdc)				50	-0.25	-	-0.2	-0.36		-0.14	-	
(VOH - 9.5 Vdc)				10	-0.62	- 1	-0.5	-0.9	-	-0.35		
(VOH = 13.5 Vdc)			BRVAWA	15	-1.8	THEY DU	-1.5	-3.5	g -	-1.1	-	
(VOL = 0.4 Vdc)	Sin	k	IOL	5.0	0.64	-	0.51	0.88	-	0.36	-	mAdc
(VOL = 0.5 Vdc)			1	10	1.6		1.3	2.25	-	0.9		
(VOL 1.5 Vdc) -			in 08	15	4.2	-	3.4	8.8	-	2.4	-	
Output Drive Current	ICL/CP	Device)	ІОН									mAdc
(VOH - 25 Vdc)	Soc	irce	2100	5.0	-1.0		-0.8	-1.7	gav	-0.6		
(VOH : 4.6 Vdc)			2000	5.0	-0.2		-0.16	-0.36	17	-0.12	-	1
(VOH = 9.5 Vdc)			2101-	10	-0.5		-0.4	-0.9	at 5	-0.3	.00	
(VOH = 13.5 Vdc)				15	-1.4	-	-1.2	-3.5	- 1	-1.0	nītu 9	
(VOL = 0.4 Vdc)	Sin	k	IOL.	5.0	0.52	70000	0.44	0.88	-	0.36	103029090	mAdc
(VOL = 0.5 Vdc)				10	13	1	1.1	2.25	720	0.9	-	
(VOL = 15 Vdc)			2010	15	3.6		30	8.8	VET	24		
nput Current (AL De	vice)		ad in	15		+01		±0.00001	±01	-	•10	μAdc
nput Current (CL/CP	Device)		1 _{in}	15	700000	+03		±0.00001	±03		:10	μAdc
nput Capacitance			Cin		-			5.0	7.5		1	pF
(V ₁₀ = 0)				Name -						10-28		
Quiescent Current (Al	Device		1pp	50		0.25		0.0005	0.25	-	7.5	μAdc
(Per Package)			100	10		0.50		0.0010	0.50		15 0	
				. 15		1.00		0.0015	1.00		30.0	
Quiescent Current (CI	/CP Dev	ice)	IDD	50		1.0		0.0005	1.0		7.5	µAdc
(Per Package)			00	10		2.0		0.0010	2.0		15.0	proje.
				15		4.0		0.0015	4.0	-	30.0	
Total Supply Current	*1	may 2/3/5	IT	5.0		-	IT =	(0.3 μA/kH) f + lon	/N	6.0353111	uAdc.
(Dynamic plus Qui			12000	10				(0.6 μA/kH				I Andic
Per Gate, C1 = 50				15				(0.8 µA/kH				

 $^{^{\}circ}$ T_{low} = -55 $^{\circ}$ C for AL Device, -40 $^{\circ}$ C for CL/CP Device. T_{high} = +125 $^{\circ}$ C for AL Device, +85 $^{\circ}$ C for CL/CP Device.

#Noise immunity specified for worst case input combination. Noise Margin for both "1" and "0" level = 0.5 Vdc min @ V_{DD} = 5.0 Vdc 1.0 Vdc min @ V_{DD} = 10 Vdc 1.0 Vdc min @ V_{DD} = 15 Vdc

†To calculate total supply current at loads other than 50 pF

IT(CL) = IT(50 PF) + N X 10-3 (CL - 50) VDDf

where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, f in kHz is input frequency and N is number of gates per package

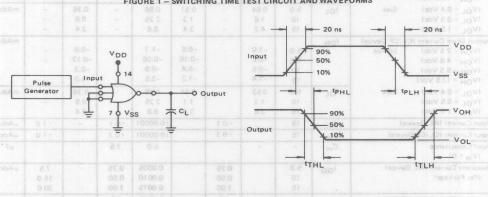
* *The formulas given are for the typical characteristics only at 25°C.

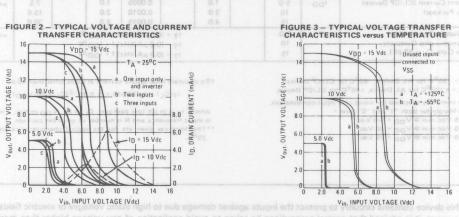
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields: however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in} \text{ or } V_{out}) \le V_{DD}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g. either V_{SS} or V_{DD}).

Character	ristic				Symbol	VDD	Min	Тур	Max	Unit
tind they they had	au T	1 0000	mar 805	Min	1 say	Vdc		bullation!	Charge	
Output Rise Time t _{TLH} = (3.0 ns/pF) C _L + 30 ns t _{TLH} = (1.5 ns/pF) C _L + 15 ns t _{TLH} = (1.1 ns/pF) C _L + 10 ns					tTLH	5.0 10 15	lava J	180 90 65	360 180 130	ns
Output Fall Time t _{THL} = (1.5 ns/pF) C _L + 25 ns t _{THL} = (0.75 ns/pF) C _L + 12.5 ns t _{THL} = (0.55 ns/pF) C _L + 9.5 ns	0 e 01 21	8 9 68 61		4.95 9.95 14.95	tTHL	5.0 10 15	f <u>a</u> vau	100 50 40	200 100 80	ns out
Propagation Delay Time tpLH, tpHL = (1.7 ns/pF) CL + 30 ns tpLH, tpHL = (0.66 ns/pF) CL + 22 ns tpLH, tpHL = (0.50 ns/pF) CL + 15 ns	2.25 4.50 6.75		2.0		tPLH, tPHL	5.0 10 15	tave.)	115 55 40	230 110 80	ns OV

The formulas given are for the typical characteristics only.

FIGURE 1 -SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



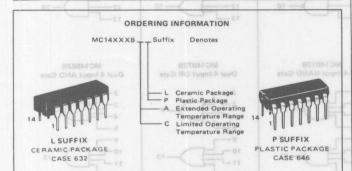




B-SUFFIX SERIES CMOS GATES

The B Series logic gates are constructed with P and N channel enhancement mode devices in a single monolithic structure (Complementary MOS). Their primary use is where low power dissipation and/or high noise immunity is desired.

- Quiescent Current = 0.5 nA typ/pkg @ 5 Vdc
- Noise Immunity = 45% of VDD typ
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range.
- Double Diode Protection on All Inputs
- Pin-for-Pin Replacements for Corresponding CD4000 Series B Suffix Devices



MAXIMUM RATINGS (Voltages referenced to Vss)

Rating	Symbol	Value	Unit
DC Supply Voltage	V _{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	Vin	-0.5 to V _{DD} +0.5	Vdc
DC Current Drain per Pin	1	10	mAdc
Operating Temperature Range – AL Device CL/CP Device	TA	-55 to +125 -40 to +85	°C
Storage Temperature Range	T _{stg}	-65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either $v_{\mbox{\footnotesize{SS}}}$ or $v_{\mbox{\footnotesize{DD}}}.$

MC14001B Quad 2-Input NOR Gate

MOS 8-SERIES GATES

MC14002B Dual 4-Input Nor Gate

MC14011B Quad 2-Input NAND Gate

MC14012B

Dual 4-Input NAND Gate

MC14023B Triple 3-Input NAND Gate

MC14025B Triple 3-Input NOR Gate

> MC14068B 8-Input NAND Gate

MC14071B Quad 2-Input OR Gate

MC14072B Dual 4-Input OR Gate

MC14073B
Triple 3-Input AND Gate

MC14075B
Triple 3-Input OR Gate

MC14078B 8-Input NOR Gate

MC14081B Quad 2-Input AND Gate

MC14082B Dual 4-Input AND Gate

CMOS SSI

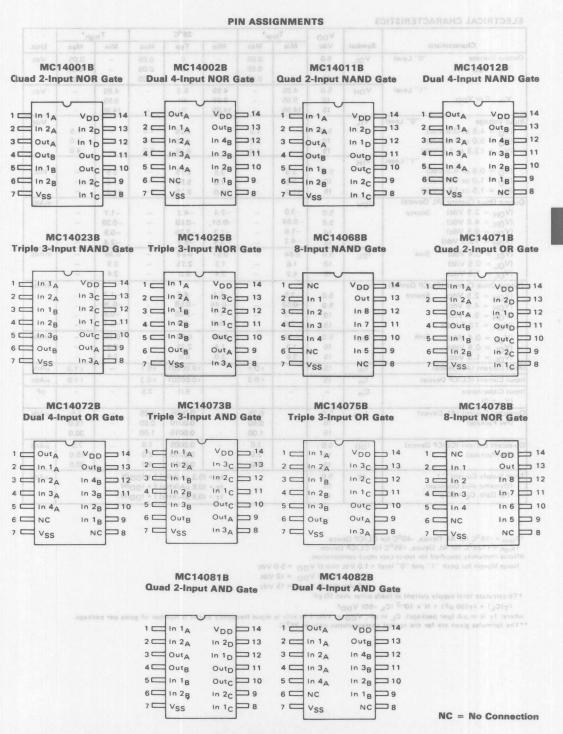
(LOW-POWER COMPLEMENTARY MOS)

B-SERIES GATES



LOGIC DIAGRAMS

NOR	NAND	OR	AND
MC14001B Quad 2-Input NOR Gate	MC14011B Quad 2-Input NAND Gate	MC14071B Quad 2-Input OR Gat	MC14081B Quad 2-Input AND Gate
1 3 2 5 0 4	1 2 5 6 4	6—	2-
N 8 0 10 T 12	8 9 12	8 9	10 8 10
13 0 11	130—11	13 GO	V 10 484 = 13 10/1 0
MC14025B	MC14023B	MC14075B	benefitu8 stugtuO HA e
Triple 3-Input NOR Gate	Triple 3-Input NAND Gate	Triple 3-Input OR Gat	Triple 3-Input AND Gate
3 8 9	2 9 8 9	2 8 9	9 10 2 9 9 3
N 4 6	4 6	4 5	5 4 6
T 11 12 10 10	11 12 10 10	11 12 13 MONTAMED AND S	10 12 10
MC14073B			MC14XXX8
Dual 4-Input NOR Gate	MC14012B Dual 4-Input NAND Gate	MC14072B Dual 4-Input OR Gat	MC14082B Dual 4-Input AND Gate
4 3 0 1 1 N 5 P 9 U 10 U 11 11 11 11 11 11 11 11 11 11 11 11 1	2 3 4 5 10 11 11 12	2 3 4 5	1 2 3 1 1 1 5 1 3 1 3 1 3 1 3 1 3 1 3 1 3 1
MC140828	'2		AXIMUM RATINGS (Voltages relen
MC14078B 8-Input NOR Gate	MC14068B 8-Input NAND Gate	V todmy2	operation vigges and a special research and an annual research and an annual research.
8 2	2 0bAm 01 30 821+4	raa- for	SS = Pin 7 All Devices
1 4	The second control of		
I 4 N 5 P 9 U 10 T 10	5 9 10	1 .00	
N 5 P 9 13	9 10 13 10 11 11 12 ad and the second points and another area of the second points and the second points are a second points and a second points are a second point are a second points are a second point are a second points are a second point are a seco	deb statege studies against de sever, it is advised that not over than maximum	This device contains circultry to con- static votragas or electric Helds; main- tainen to evold application at site wo this high implessme claudt. For prop



		VDD	Tio	w*		25°C		Th	igh *	
Characteristic	Symbol	Vdc	Min	Max	Min	Тур	Max	Min	Max	Unit
Output Voltage "0" Level	VOL	5.0	-	0.05	-	0	0.05	-	0.05	Vdc
V _{ID} V _{DD} or 0	ort	10	- 1	0.05	10.28	0	0.05	-	0.05	DM:
te Dual 4-Input NAND G	D OHAR	15	Cuested 1	0.05	Nen d	0 1	0.05	sleD I	0.05	nt-S b
"1" Level	VOH	5.0	4.95	-	4.95	5.0	-	4.95	-	Vdc
V _{ID} 0 or V _{DD}	0	10	9.95		9.95	10	-	9.95		
		15	14.95	67.00	14.95	15		14.95	-	
Input Voltage "0" Leve	VIL	A 7 1	1		da	ATTEN		1	O.	Vdc
$(V_0 = 4.5 \text{ or } 0.5 \text{ Vdc})$	tin 20 EE	5.0	2 0	1.5	gruO	2.25	1.5	ET 55	1.5	as m
$(V_0 = 9.0 \text{ or } 1.0 \text{ Vdc})$		10	be	3.0	alveri	4.50	3.0	or Ed.	3.0	A540
(V _O = 13.5 or 1.5 Vdc)	10.	15		4.0		6.75	4.0		4.0	
"1" Leve		Bros			-			1		-
$(V_0 = 0.5 \text{ or } 4.5 \text{ Vdc})$	Outo	5.0	3.5	010	3.5	2.75	E 10	3.5	Out	Vdc
(V _O = 1.0 or 9.0 Vdc)		10	7.0	_ R E2	7.0	5.50	TTL8	7.0	C n=	10.26
(V _O = 1.5 or 13.5 Vdc)	113000	15	11:0	70.00	11.0	8.25	377	11.0		
Output Drive Current (AL Device)	ТОН	20	11.0	25 from	311.0	0.20	esterned 1	11.0	II. OL	mAdo
(V _{OH} = 2.5 Vdc) Source	TOH	5.0	-3.0		-2.4	-4.2	_	-1.7		made
(V _{OH} = 4.6 Vdc)		5.0	-0.64		-0.51	-0.88		-0.36		
$(V_{OH} = 9.5 \text{ Vdc})$		10	-1.6		-1.3	-2.25		-0.9		
$(V_{OH} = 13.5 \text{ Vdc})$	2830	15	-4.2		-3.4	-8.8	_	-2.4	214013	199
$(V_{OL} = 0.4 \text{ Vdc})$ Sink	DEP ON	5.0	0.64	\$13.00 E	0.51	0.88	title .	0.36	लेकी उपयो	mAdd
$(V_{OL} = 0.4 \text{ Vdc})$ Sink $(V_{OL} = 0.5 \text{ Vdc})$	OL	10	1.6	_	1.3	2.25	_	0.36		MAGG
		15	4.2		3.4	8.8	-	2.4		
(V _{OL} = 1.5 Vdc)		15	4.2	-	3.4			2.4		
Output Drive Current (CL/CP Device)	ОН	21	0.5	21 0	00	AFO	100			mAdd
(V _{OH} = 2.5 Vdc) Source	700	5.0	-2.5	61 50	-2.1	-4.2	2005	1.7	0 n1-	S ni
$(V_{OH} = 4.6 \text{ Vdc})$	E n1	5.0	-0.52	E 12	-0.44	-0.88 -2.25	3.000	-0.36	2 m 2	T of
$(V_{OH} = 9.5 \text{ Vdc})$		10 2 0	-1.3					-0.9	f nl	10.20
$(V_{OH} = 13.5 \text{ Vdc})$	to 3	15 E a	-3.6	UE	-3.0	-8.8	TTLA -	-2.4		8500
$(V_{OL} = 0.4 \text{ Vdc})$ Sink	IOL	5.0	0.52	OH CO	0.44	0.88	TTD-8	0.36	TuO_	mAdo
$(V_{OL} = 0.5 \text{ Vdc})$	d ani	10	1.3	0.00	1.6	2.25	TT A	0.9	0.000	100
$(V_{OL} = 1.5 \text{ Vdc})$		15	3.6		3.0	8.8	-	2.4	E of	Laure !
Input Current (AL Device)	1 _{in}	15		± 0.1	The same	± 0.00001	±0.1	-	± 1.0	μAdo
Input Current (CL/CP Device)	lin	. 15		± 0.3	-	±0.00001	± 0.3	-	± 1.0	μAdd
Input Capacitance	Cin	-	-			5.0	7.5	1	-	pF
(V _{in} = 0)					-					
Quiescent Current (Al. Device)	loc	5.0	1 10	0.25	- FEET 13	0.0005	0.25	-	7.5	μAdd
(Per Package)	IDD	10	Sqin'i	0.50	UNA	0.0010	0.50	6860	15.0	
		15		1.00	-	0.0015	1.00		30.0	13.5
Quiescent Current (CL/CP Device)	lon	5.0		1.00		0.0005	1.0		7.5	
(Per Package)	1DD	10	the state of	2.0	OQV	0.0005	2.0	N con a	15.0	μAde
ti ei rackagei	7	15		4.0	In-3c	0.0010	4.0	0	30.0	
True railes Et		-			-			(N)	30.0	Lat
Total Supply Current**†	Total	5.0	3 E			(0.3 μA/kH			in d	μAdd
(Dynamic plus Quiescent, Per Gate, C ₁ = 50 pF)	di at m	10	bo			(0.6 μA/kH				1000
rei Gate, CL - 50 pri		15			IT =	(0.9 μA/kH	z) f + 1 DE	D/M		A STATE

*T_{IOW} = -55°C for AL Device, -40°C for CL/CP Device.

Thigh = +125°C for AL Device, +85°C for CL/CP Device. #Noise immunity specified for worst-case input combination.

Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc

2.0 Vdc min @ VDD = 10 Vdc

2.5 Vdc min @ V_{DD} = 15 Vdc

To calculate total supply current at loads other than 50 pF

I_T(C_L) = I_T(50 pF) + N x 10-3 (C_L -50) V_{DD}f

NC = No Connection

where: IT is in µA (per package), CL in pF, VDD in Vdc, f in kHz is input frequency and N is number of gates per package.

*The formulas given are for the typical characteristics only at 25°C.

3-8

MC14081B

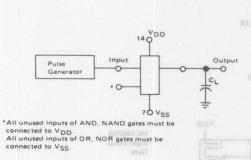
B-SERIES GATE SWITCHING TIMES

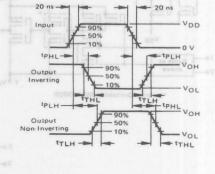
SWITCHING CHARACTERISTICS* (CL = 50 pF, TA = 25°C)

Characteristic	Symbol	V _{DD} Vdc	Min	Тур	Max	Unit
Output Rise Time, All B-Series Gates	tTLH	5.0		0	3V	ns
^t TLH = (1.35 ns/pF) C _L + 33 ns ^t TLH = (0.60 ns/pF) C _L + 20 ns			-	100	200	B.139-9
tTLH = (0.40 ns/pF) C _L + 20 ns		10 15		50 40	100	
Output Fall Time, All B-Series Gates	^t THL	et n		En L	-1	ns
^t THL = (1.35 ns/pF) C _L + 33 ns		5.0		100	200	
^t THL = (0.60 ns/pF) C _L + 20 ns	11,01	10	1	50	100	
tTHL = (0.40 ns/pF) CL + 20 ns		15	and I	40	80	
Propagation Delay Time MC14001B, MC14011B only	tPLH, tPHL]		ns
tpLH, tpHL = (0.90 ns/pF) C ₁ + 80 ns		5.0	_	125	250	
tpLH, tpHL = (0.36 ns/pF) C _L + 32 ns		10		50	100	
tpLH, tpHL = (0.26 ns/pF) CL + 27 ns		15	BIGGRAGON	40	80	
All Other 2, 3, and 4 Input Gates	011,5,1					
tplH, tpHI = (0.90 ns/pF) C ₁ + 115 ns	921.62	5.0	_	160	300	
tpLH, tpHL = (0.36 ns/pF) CL + 47 ns		10	_	65	130	
tpLH, tpHL = (0.26 ns/pF) CL + 37 ns		15	-	50	100	
8-Input Gates (MC14068B, MC14078B)			193			
tpLH, tpHL = (0.90 ns/pF) CL + 155 ns	ou grow	5.0	-	200	350	
tpLH, tpHL = (0.36 ns/pF) CL + 62 ns		10	-	80	150	
tpLH, tpHL = (0.26 ns/pF) CL + 47 ns		15	ESONA	60	110	

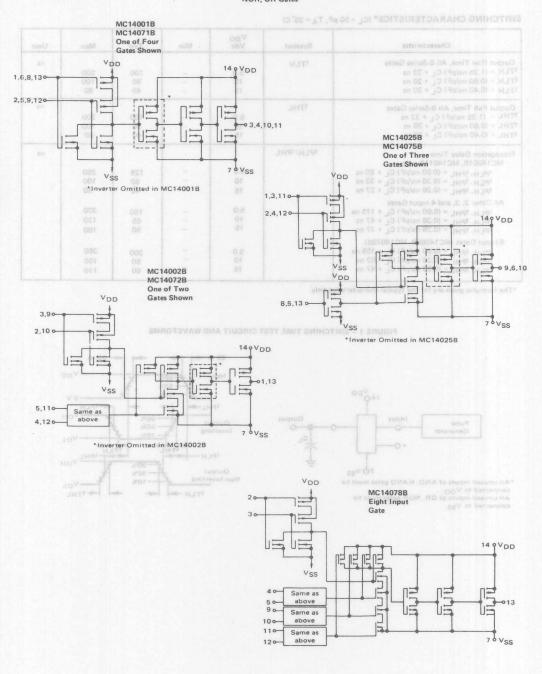
^{*}The formulas given are for the typical characteristics only.

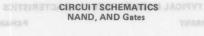
FIGURE 1 - SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

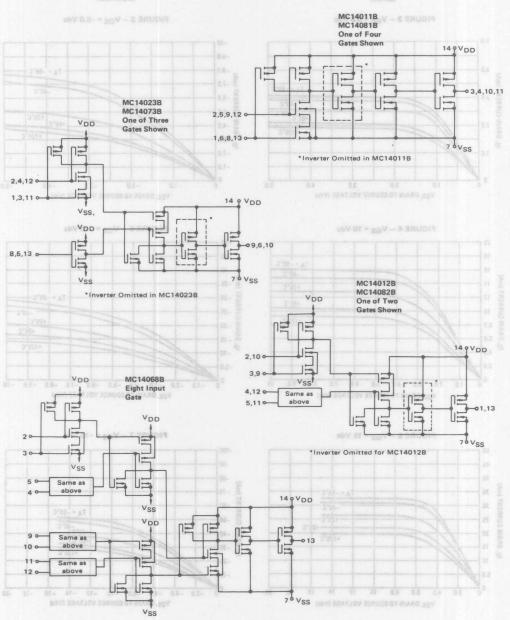




CIRCUIT SCHEMATIC NOR, OR Gates







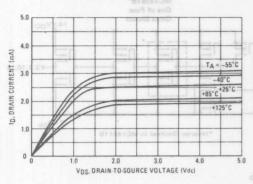
TYPICAL B-SERIES GATE CHARACTERISTICS

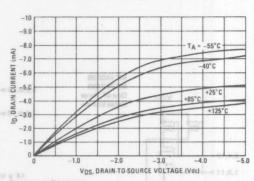
N-CHANNEL DRAIN CURRENT

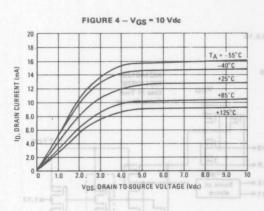
P-CHANNEL DRAIN CURRENT (SOURCE)

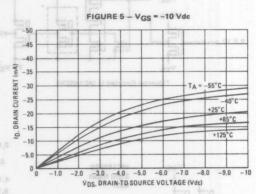
FIGURE 2 - VGS = 5.0 Vdc

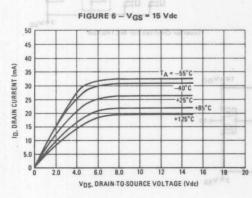
FIGURE 3 - VGS = -5.0 Vdc

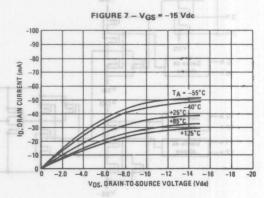












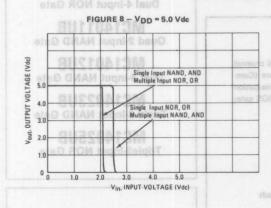
CMOS B-SERIES GATES





GIAD ROM fugni-S bau TYPICAL B-SERIES GATE CHARACTERISTICS (cont'd)

VOLTAGE TRANSFER CHARACTERISTICS



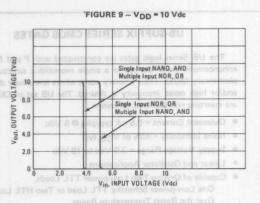
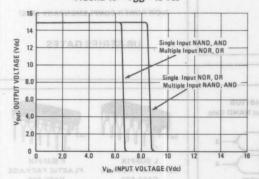


FIGURE 10 - VDD = 15 Vdc

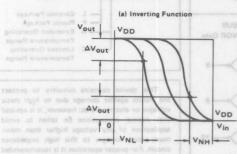


DC NOISE IMMUNITY (VNL AND VNH)

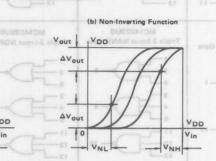
Double Diode Protection on All Inputs

The dc noise immunity is defined as the input voltage range from an Ideal "1" or "0" input level (assuming the previous CMOS driving state is unloaded which does not produce output state (combination) change(s). The typical and limit values of the input ranges V_{NL} and V_{NH} for the output to stay within a range aV_{out} from either V_{DD} or V_{SS} are given in the Electrical Characteristics table. The definitions of V_{NL} V_{NH}, and aV_{out} are illustrated in Figure 11 for inverting and non-inverting functions.

FIGURE 11 - DC NOISE IMMUNITY



appropriate logic voltage level (e.g., either



VSS = 0 volts dc



UB-SUFFIX SERIES CMOS GATES

8-SERIES GATE CHARACTERISTICS (cont'd)

The UB Series logic gates are constructed with P and N channel enhancement mode devices in a single monolithic structure (Complementary MOS). Their primary use is where low power dissipation and/or high noise immunity is desired. The UB set of CMOS gates are inverting non-buffered functions.

- Quiescent Current = 0.5 nA typ/pkg @ 5 Vdc
- Noise Immunity = 45% of VDD typ
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Linear and Oscillator Applications
- Capable of Driving Two Low-power TTL Loads,
 One Low-power Schottky TTL Load or Two HTL Loads
 Over the Rated Temperature Range.
- Double Diode Protection on All Inputs
- Pin-for-Pin Replacements for Corresponding CD4000 Series UB Suffix Devices
- Formerly Listed without UB Suffix

MC14001UB Quad 2-Input NOR Gate

MOS ESERIES GATES

MC14002UB
Dual 4-Input NOR Gate

MC14011UB Quad 2-Input NAND Gate

MC14012UB
Dual 4-Input NAND Gate

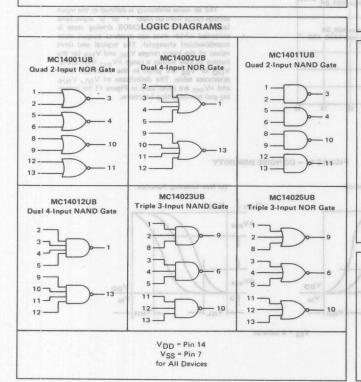
MC14023UB
Triple 3-Input NAND Gate

MC14025UB Triple3-Input NOR Gate

CMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

UB-SERIES GATES

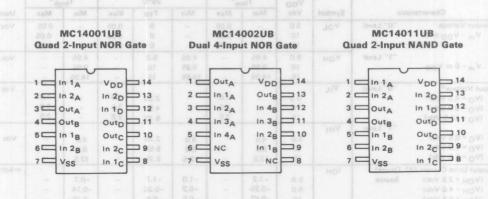


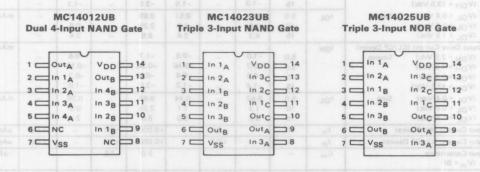


This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that $V_{\rm in}$ and $V_{\rm out}$ be constrained to the range $V_{\rm SS} \le (V_{\rm in} \ {\rm or} \ V_{\rm OD})$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD).







NC = No Connection

MAXIMUM RATINGS (Voltages referenced to VSS)

Rating	Symbol	Value	Unit
DC Supply Voltage	V _{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	Vin	-0.5 to V _{DD} +0.5	Vdc
DC Current Drain per Pin	-00	10	mAdc
Operating Temperature Range - AL Device CL/CP Device	TA	-55 to +125 -40 to +85	оС
Storage Temperature Range	T _{stg}	-65 to +150	OC.

ELECTRICAL CHAR	ACTERISTICS
-----------------	-------------

		Vpp	Tic	ow*		25°C		Th	igh *	
Characteristic	Symbol	Vdc	Min	Max	Min	Тур	Max	Min	Max	Unit
Output Voltage "0" Level	VOL	5.0	-	0.05	-	0	0.05	-	0.05	Vdc
Vin VDD or 0		10	800200	0.05	-	0	0.05	NC1400	0.05	1
d 2-Input NAND Coto	81 O 48	15	RIGHT 1	0.05	SOC-	0 555	0.05	magari-S	0.05	
"1" Level	VOH	5.0	4.95	-	4.95	5.0	-	4.95	-	Vdc
V _{in} = 0 or V _{DD}	0	10	9.95	-	9.95	10		9.95	-	
		15	14.95		14.95	15	-	14.95		1
Input Voltage# "0" Level	VIL		200				700"	28.	1	Vdc
(Vo = 4.5 Vdc)	2 5	5.0	Bing	1.0	30	2.25	1.0	24-	1.0	
(VO = 9.0 Vdc)	36	10	gilt rel	2.0	- 3 C	4.50	2.0	75,214	2.0	
(Vo = 13.5 Vdc)	76	15	10.67	2.5		6.75	2.5	-	2.5	
"1" Level	VIH			-			James	-		
(VO = 0.5 Vdc)	B	5.0	4.0	AB HI	4.0	2.75	F arun	4.0	1 -10	Vdc
(V _O = 1.0 Vdc)	38	10	8.0	-DIA	8.0	5.50	ST OF IN	8.0	1	1000
(V _O = 1.5 Vdc)	310	15	12.5		12.5	8.25	5.0	12.5		
Output Drive Current (AL Device)	ГОН			20.7			Tar ar			mAdo
(VOH = 2.5 Vdc) Source	1011	5.0	-1.2	_	-1.0	-1.7	_	-0.7	-	
(V _{OH} = 4.6 Vdc)		5.0	-0.25	_	-0.2	-0.36	-	-0.14	_	
(VOH = 9.5 Vdc)		10	-0.62		-0.5	-0.9	-	-0.35	-	
(VOH = 13.5 Vdc)		15	-1.8		-1.5	-3.5	_	-1.1	-	
(VOI = 0.4 Vdc) Sink	IOL	5.0	0.64	eram-	0.51	0.88	SUS	0.36	-	mAdo
(V _{OL} = 0.5 Vdc)	,OL	10	1.6		1.3	2.25	The second second	0.9	a tomore	1
(VOL = 1.5 Vdc)	-	15	4.2	S-Empe	3.4	8.8	D CTINAI	2.4	a lmud	
Output Drive Current (CL/CP Device)	ГОН	-	-		-	-		-		mAdo
(VOH = 2.5 Vdc) Source	TOH	5.0	-1.0		-0.8	-1.7	1	-0.6	7	made
(V _{OH} = 4.6 Vdc)	31	5.0	-0.2	& Entit	-0.16	-0.36	Noze II	-0.12	1 120	
(V _{OH} = 9.5 Vdc)	7	E10	-0.5	a tent	-0.4	-0.9	=100	-0.3	2 mm-11	1
(V 12 E V/d-)		15	-1.4		-1.2	-3.5	T STATE	-1.0		
(VOL = 0.4 Vdc) Sink	IOL	5.0	0.52		0.44	0.88	100.01	0.36		mAdc
(VOL = 0.5 Vdc)	OL	10	1.3	82 ml	1.1	2.25	In 3g	0.30	11 Th	MAGC
(V _{OL} = 1.5 Vdc)	3	15	3.6	gt nr	3.0	8.8	in 2g in	2.4	100	
OL .	1	15	1.7UD	±0.1	3.0	±0.00001	±0.1	2.9	110	μAdc
	lin		-	67.7					-	-
Input Current (CL/CP Device)	1 in	15	p.E. ect	± 0.3	70 6	±0.00001	±03	- 88	11.0	μAdc
Input Capacitance	Cin	-	-			5.0	7.5	-	- 1	pF
(V _{in} = 0)										
Quiescent Current (AL Device)	IDD	5.0	-	0.25		0.0005	0.25	-	7.5	μAdc
(Per Package)		10	-	0.50		0.0010	0.50	1	15.0	
		15	Comp.	1.00	-	0.0015	1.00	-	30.0	
Quiescent Current (CL/CP Device)	IDD	5.0	-	1.0	-	0.0005	1.0		7.5	μAdc
(Per Package)		10	-	2.0	-	0.0010	2.0	-	15.0	
		15	-	4.0	-	0.0015	4.0	-	30.0	
Total Supply Current**†	IT	5.0			T =	(0.3 µA/kH2	r) f + ipp	/N		μAdc
(Dynamic plus Quiescent,		10				10.6 µA/kH2				1
Per Gate, C _L = 50 pF)		15				(0.8 µA/kH				1

 $^{^{\}circ}T_{1ow} = -55^{\circ}C$ for AL Device, $-40^{\circ}C$ for CL/CP Device. $T_{high} = +125^{\circ}C$ for AL Device, $+85^{\circ}C$ for CL/CP Device.

†To calculate total supply current at loads other than 50 pF:

 $I_T(C_L) = I_T(50 \text{ pF}) + N \times 10^{-3} (C_L - 50) V_{DD} f$

where: I_{T} is in μA (per package), C_{L} in pF, V_{DD} in Vdc, f in kHz is input frequency and N is number of gates per package.

[#]Noise immunity specified for worst-case input combination. Noise Margin for both "1"and "0" level =

0.5 Vdc min @ V_{DD} = 5.0 Vdc

1.0 Vdc min @ V_{DD} = 10 Vdc

1.0 Vdc min @ V_{DD} = 15 Vdc

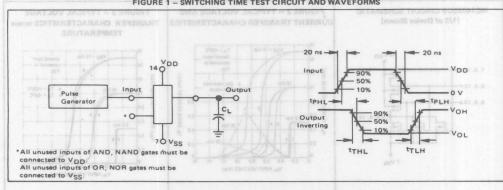
^{**}The formulas given are for the typical characteristics only at 25°C.

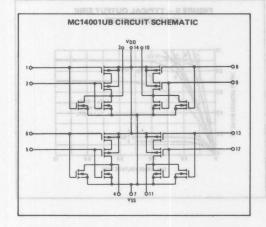
SWITCHING CHARACTERISTICS* (CL = 50 pF, TA = 25°C)

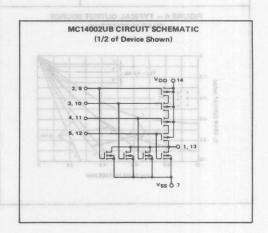
Characteristic		Symbol	V _{DD} Vdc	Min	Тур	Max	Unit
Output Rise Time	007.51	tTLH					ns
tTLH = (3.0 ns/pF) CL + 30 ns			5.0	-	180	360	
tTLH = (1.5 ns/pF) CL + 15 ns			10	-	90	180	100
tTLH = (1.1 ns/pF) CL + 10 ns		n tin tin	15	-	65	130	
Output Fall Time	er co	tTHL			toil	The	ns
tTHL = (1.5 ns/pF) CL + 25 ns			5.0	- 12.00	100	200	
tTHL = (0.75 ns/pF) CL + 12.5 ns			10	-	50	100	
tTHL = (0.55 ns/pF) CL + 9.5 ns			15	-	40	80	1,8,8,12
Propagation Delay Time	12	tPLH, tPHL	or c		14		ns
tpLH, tpHL = (1.7 ns/pF) CL + 30 ns			5.0	-	90	180	25.0.0.0
tpLH, tpHL = (0.66 ns/pF) CL + 22 ns			10	-	50	100	
tpLH, tpHL = (0.50 ns/pF) CL + 15 ns			15	-	40	80	1 186

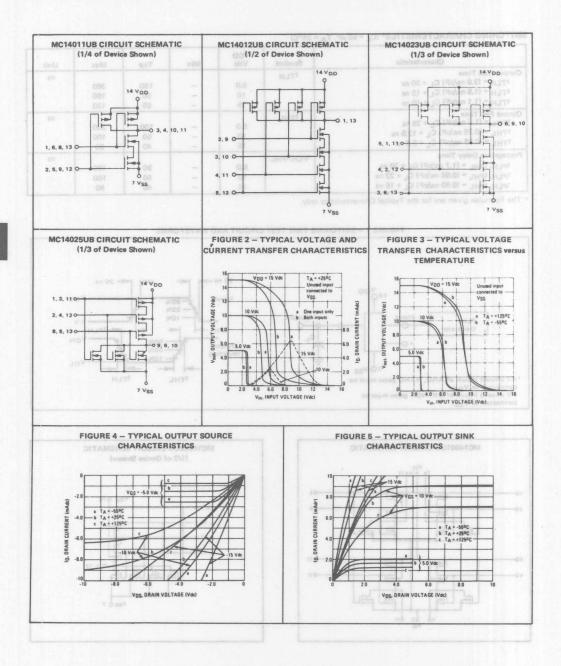
^{*} The Formulae given are for the Typical Characteristics only.

FIGURE 1 - SWITCHING TIME TEST CIRCUIT AND WAVEFORMS











MC14002B MC14002UB

DUAL 4-INPUT "NOR" GATE

The MC14002B and MC14002UB are constructed with P and N channel enhancement mode devices in a single monolithic structure (Complementary MOS). Their primary use is where low power dissipation and/or high noise immunity is desired.

- Quiescent Current = 0.5 nA typ/pkg @ 5 Vdc
- Noise Immunity = 45% of VDD typ
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered (MC14002B only)
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range. (MC14002B only)
- Double Diode Protection on All Inputs
- Pin-for-Pin Replacements for CD4002B and CD4002UB

MAXIMUM RATINGS (Voltages referenced to VSS)

Rating	Symbol	Value	Unit
DC Supply Voltage	V _{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	Vin	-0.5 to VDD +0.5	Vdc
DC Current Drain per Pin	1 1	10 10 of d	mAdc
Operating Temperature Range - AL Device CL/CP Device	TA	-55 to +125 -40 to +85	∃ C°C
Storage Temperature Range	T _{stg}	-65 to +150	°C

See the MC14001B data sheet for complete characteristics of the R. Series device

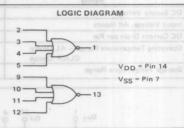
See the MC14001UB data sheet for complete characteristics for the UB device.

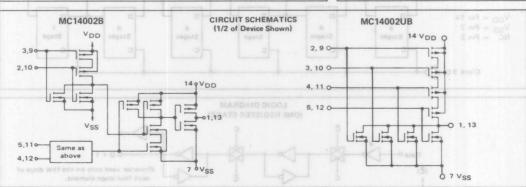
CMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

DUAL 4-INPUT "NOR" GATE







This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper

operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leqslant (V_{in}$ or $V_{out}) \leqslant V_{DD}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

MC14006B



The MC14006B shift register is comprised of four separate shift register sections sharing a common clock: two sections have four stages, and two sections have five stages with an output tap on both the fourth and fifth stages. This makes it possible to obtain a shift register of 4, 5, 8, 9, 10, 12, 13, 14, 16, 17, or 18 bits by appropriate selection of inputs and outputs. This part is particularly useful in serial shift registers and time delay circuits.

18-BIT STATIC SHIFT REGISTER

- Output Transitions Occur on the Falling Edge of the Clock Pulse
- Quiescent Current 5nA/package typical @ 5 Vdc
- Fully Static Operation
- 8-MHz Shift Rate typical
- Can be Cascaded to Provide Longer Shift Register Lengths
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range
- Pin-for-Pin Replacement for CD4006B

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

18-BIT STATIC SHIFT REGISTER





L SUFFIX CERAMIC PACKAGE CASE 632 P SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

MC14XXXB TT Suffix Denotes

L Ceramic Package
 P Plastic Package

A Extended Operating
Temperature Range
C Limited Operating

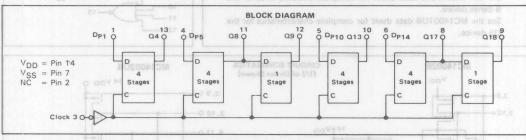
C Limited Operating Temperature Range

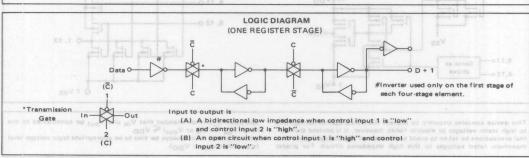
MAXIMUM RATINGS (Voltages referenced to VSS)

Rating	Symbol	Value Value	Unit
DC Supply Voltage REALG DISCL	VDD	-0.5 to +18	Vdc
Input Voltage, All Inputs	Vin	-0.5 to V _{DD} + 0.5	Vdc
DC Current Drain per Pin	1	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	TA	-55 to +125 -40 to +85	°C
Storage Temperature Range	T _{stg}	-65 to +150	°C

TRUTH TABLE (Single Stage)







		gyT	rs(8)8	VDD	DD T _{lo}			25°C		Th	igh *	
	Characteri	stic	Symbol	Vdc	Min	Max	Min	Тур	Max	Min	Max	Unit
Output	Voltage	"0" Level	VOL	5.0	-	0.05		0	0.05	C: +30	0.05	Vdc
Vin	Vnn or 0	50	- 02	10	-	0.05		0	0.05	Cr + 15	0.05	
	08	40		15	-	0.05	- 1	0	0.05	01 + 10	0.05	
		"1" Level	VOH	5.0	4.95		4.95	5.0	-	4.95	some inch	Vdc
	0 or V _{DD}	100	- OH	10	9.95	JHT	9.95	10		9.95	Roter 8.1	* JR7
	100	08		15	14.95	_	14.95	15	-in 8	14.95	Rolan-St. D	
Input Vo	oltage#	"0" Level	VIL			-			201	(0 + 10 (Rg\zn 88.0	Vdc
	= 4.5 or 0.5 Vdd		-11	5.0	-	1:5		2.25	1.5	word?	1.5	ananna5
-	= 9.0 or 1.0 Vda			10		3.0		4.50	3.0	30\m 2.1	3.0	
	= 13.5 or 1.5 Vo			15	-	4:0	_	6.75	4.0	pla=38.6	4.0	0 107
0		0"1" Level	VIH	. 8				85	C1 + 55	3.5 ns/oF	2 3697	1.197
(Vo	= 0.5 or 4.5 Vde	100 (3	200	5.0	3.5	Trust	3.5	2.75	-	3.5	ristateN sets	Vdc
(VO	= 1.0 or 9.0 Vdd		120	10	7.0	13366	7.0	5.50	_	7.0	-	
(VO	= 1.5 or 13.5 Vo		08	15	11.0	-	11.0	8.25	-	11.0	-	- 30
Output [Drive Current (A	I Device)	ГОН	n						NO.	super Freque	mAdc
	= 2.5 Vdc)	Source	.01	5.0	-3.0	lo ¹	-2.4	-4.2	2.11	-1.7	anthat I act	1112100
	= 4.6 Vdc)	12		5.0	-0.64		-0.51	-0.88	_	-0.36	_	1200
	= 9.5 Vdc)			10	-1.6		-1.3	-2.25		-0.9	else Flise ac	A
	= 13.5 Vdc)			15	-4.2	HJTT	-3.4	-8.8	1131	-2.4	DE 98121 9814	Stock P
	= 0.4 Vdc)	Sink	loL	5.0	0.64	-	0.51	0.88	_	0.36	-	mAdc
	= 0.5 Vdc)	08-		10	1.6	_	1.3	2.25	_	0.9	_	
	= 1.5 Vdc)	00-	0	15	4.2	_02	3.4	8.8	-	2.4	am	T quasi
	Orive Current (C		10н							-		mAdc
	4 = 2.5 Vdc)	Source		5.0	-2.5		-2.1	-4.2		-1.7		
	4 = 4.6 Vdc)	7.01	180	5.0	-0.52	10	-0.44	-0.88	_	-0.36	9/1	er brok
	= 9.5 Vdc)	25.	08	10	-1.3	-	-1.1	-2.25	_	-0.9	_	
	= 13.5 Vdc)	05	7.5	15	-3.6	_	-3.0	-8.8		-2.4	_	
	= 0.4 Vdc)	Sink	lOL	5.0	0.52	_	0.44	0.88		0.36	n articono	mAdc
	= 0.5 Vdc)	t leaves and blaced	TUCOL STATE	10	1.3	on min m	1.1	2.25	to this one	0.9	per Hirk r	ortiA/ s
		riouse be equal th	e suqui suq ino tuotuo	15	3.6	cose adt	3.0	8.8	Little British	2.4	t to summ	
	rrent (AL Devic	THE PERSON NAMED IN		15	0.0.0	± 0.1	0.0	±0.00001	±0.1	0 34-07.7 01	±1.0	μAdc
			lin		-	± 0.3						
	rrent (CL/CP D	evice)	lin	15	-	± 0.3	-	±0.00001	± 0.3	-	±1.0	μAdc
Input Ca (Vin	pacitance = 0)	atic voltages	Cin	anp adi	nst dam	uts agai	t the in	to protect	7.5	aniatno	device c	pF
	t Current (AL		IDD	5.0	LAR 703 LV	5.0	MUNITURS.	0.005	5.0	ontains s	150	μAdc
(Per F	Package)	nmended that	it is recon	10	0 150010	10	mio gan	0.010	10	sages to	300	
				15		20	Juc Y 10	0.015	20	ा भी। व	600	
Quiescen	t Current (CL/C	CP Device)	IDD	5.0	lov_elgo	20	dde un	0.005	20	Jaizin a	150	μAdc
(Per F	Package)			10	-	40	-	0.010	40	-	300	
				15	-	80	-	0.015	80	-	600	
Total Su	pply Current**	t	I _T	5.0			IT = (1	.3 μA/kHz)	f + Inn			μAdc
	amic plus Quies			10				.6 μA/kHz)				mr.uc
	Package)			15				.9 μA/kHz)				
(CL =	= 50 pF on all or ers switching)	utputs, all	re 2 - TY	FIGUR	11111			SOURCE C			- I BAU	HR

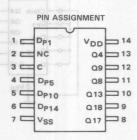
^{*}T_{Iow} = -55°C for AL Device, -40°C for CL/CP Device.

Thigh = +125°C for AL Device, +85°C for CL/CP Device.

#Noise immunity specified for worst-case input combination.

Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc

Noise Margin for both "1" and "0" level = 1.0 Vdc min @ VDD = 5.0 Vdc 2.0 Vdc min @ VDD = 10 Vdc 2.5 Vdc min @ VDD = 15 Vdc 1.0 Vdc min @ VDD = 15 Vdc min @ VDD = 1



NC = No Connection

SWITCHING CHARACTERISTICS* (CL = 50 pF, TA = 25°C)

	Characteri	istic			Symbol	1	DD	20V	Min		Тур	Max	Unit
Output Rise Time	RINT	30,000	997	11/20	tTLH	PSARI		pay	Symbol		34701	10.36.10.00	ns
tTLH = (3.0 ns/pF)	CL + 30 ns	0.05		-	60.0	-	5.0	5.0	JOY		100	200	TuqtuC
tTLH = (1.5 ns/pF)	CL + 15 ns	0.05				-	10	01	-		50	100	niV.
tTLH = (1.1 ns/pF)	CL + 10 ns	0.05				H H.	15	81	-		40	80	
Output Fall Time	4,95	-	0.8	4,25	tTHL	4.95	I	0.8	HOY		ave J "I"		ns
tTHL = (1.5 ns/pF)	CL + 25 ns	-		98.8		8.99	5.0	OF	-		100	200	niV
tTHL = (0.75 ns/pF) CL + 12.5	ns ns		4.95		14.95	10	15	-		50	100	
TTHL= (0.55 ns/pF) CL + 9.5	ns					15		JI Y		40	80	V Iuqn
Propagation Delay	Time	dJ	2.25	-	tPLH	-		0.6			Ist	4.5 or 0.6 V	ns
tPLH, tPHL = (1.7 ns/pF) (CL + 22	0 ns	1	tPHL	-	5.0	10			300	600	lov1
tPLH, tPHL = (0.66 ns/pF)	C1 + 7	7 ns			1	10	15	-		110	220	OVI
tPLH, tPHL = (0.5 ns/pF) (CL + 55	ns				15		BH.		80	160	
Clock Pulse Width	3,5		2.75	3.5	twH	3.5	5.0	0.6	200	T	100	V 6.7 16 6.U	ns
	7.0			2.0	1	7.9	10	01	120		60	V 0.0 to 0.1	OVI
				0.57		0.10	15	15	80		40 (56)	154135	OV)
Clock Pulse Freque	ency				fcl		5.0		He!		5.0	2.5	MH
				A S-		-3.0	10	5.0	-		8.3	4.2	HOVI
				16.0		\$8.0-	15	6.0	-		12	6.0	HOV)
Clock Pulse Rise an	nd Fall Time	e#	02,2-	1 9 1	tTLH	10114	5.0	. UI	-	T		15	μs
				19/2-	tTHL		10	GI			-	(35V 651 =	HDV3
				18.0		0.64	15	5.0	Jel.		Sigk	(56V 40 =	lov)
Setup Time	0.0		63.2		t _{su}	9.5	5.0	91	0		-50	(ubW_0.0 =	ns
				3.4	su	4.2	10	15	0		-15	(bbV_2 f =	JoV)
							15		0		-8.0	Jnehu⊒ evis	turpus
Hold Time	100		2.0	1119	th	1.3	5.0	0.8	180		75	KNOV O.S.	ns
				0.84	-	-0.62	10	5.0	90		25	* 4.8 Vdct	
				1111-		4.1-	15	01	75		20	* 9,5 Vdc?	HOVI.

* The formulae given are for typical characteristics only.

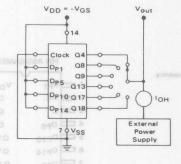
When shift register sections are cascaded, the maximum rise and fall times of the clock input should be equal to or less than the rise and fall times of the data outputs driving data inputs, plus the propagation delay of the output driving stage for the output capacitance load.

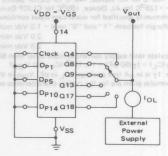
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields: however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$.

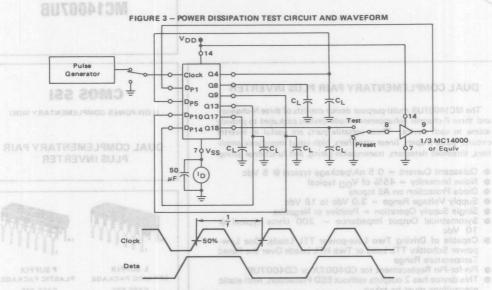
Unused inputs must always be tied to an appropriate logic voltage level (e.g. either VSS or VDD).

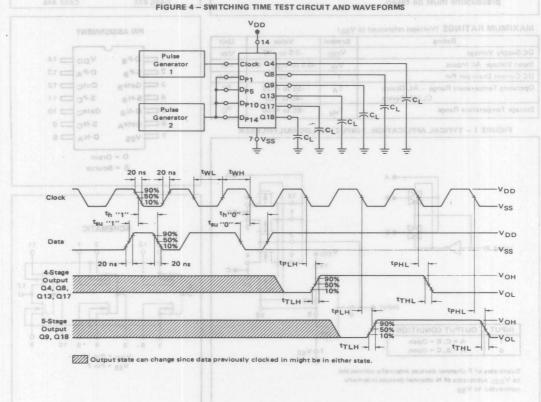
FIGURE 1 – TYPICAL OUTPUT SOURCE CURRENT CHARACTERISTICS TEST CIRCUIT

FIGURE 2 – TYPICAL OUTPUT SINK CURRENT CHARACTERISTICS TEST CIRCUIT









MC14007UB

MC14006B

DUAL COMPLEMENTARY PAIR PLUS INVERTER

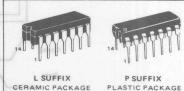
The MC14007UB multi-purpose device consists of three N-channel and three P-channel enhancement mode devices packaged to provide access to each device. These versatile parts are useful in inverter circuits, pulse-shapers, linear amplifiers, high input impedance amplifiers, threshold detectors, transmission gating, and functional gating.

- Quiescent Current = 0.5 nA/package typical @ 5 Vdc
 Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Single Supply Operation = Positive or Negative
 Symmetrical Output Impedance 200 ohms typical @
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range
- Pin-for-Pin Replacement for CD4007A or CD4007UB
- This device has 2 outputs without ESD Protection. Anti-static precautions must be taken.

CMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

DUAL COMPLEMENTARY PAIR PLUS INVERTER



PIN ASSIGNMENT

D-PB

SPB

4 S-NB

Gates

D-NB

CASE 632

CASE 646

VDD 14

D-PA = 13

Outc 12

S-PC 11

Gate_C 10

5 10

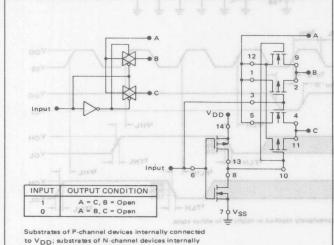
VDD = Pin 14 VSS = Pin 7

MAXIMUM RATINGS (Voltages referenced to

connected to Vss.

Rating	Symbol	Value MO	Unit
DC Supply Voltage	V _{DD}	-0 5 to +18	Vdc
Input Voltage, All Inputs	Vin	-0.5 to VDD + 0.5	Vdc
DC Current Drain per Pin	1	10	mAdd
Operating Temperature Range — AL Device CL/CP Device	TA	-55 to +125 -40 to +85	°C
Storage Temperature Range	T _{stq}	-65 to +150	ос

FIGURE 1 - TYPICAL APPLICATION: 2-INPUT ANALOG MULTIPLEXER



6 Gate S-NC 9 7 - VSS D-NA 3 D = Drain S = Source SCHEMATIC 13

3-24

ELECTRICAL CHARACTERISTICS (Connected as Inverters)

		V _{DD} Vdc	T _{low} *		25°C			Thi		
441	Symbol		Min	Max	Min	Тур	Max	Min	Max	Unit
0" Level	VOL	5.0	-	0.05	-	0	0.05	no - n	0.05	Vdc
06		10	-	0.05	-	0	0.05	00 - 0	0.05	- HUTT
		15	_	0.05	-	0	0.05	0x + 30	0.05	HUTT
	VOH	5.0	4.95	-	4.95	5.0		4.95	-	Vdc
	· OH			JHTP		10	_	9.95		L THT
67		15	14.95	-	14.95	15	- 20	14.95	39/30 V. (152.77
0" Level	VII	2					20	01 + 10	Relan & D	Vdc
	-	5.0	-	1.0	-	2.25	1.0	_	1.0	JITTE TO
		10		2.0	-	4.50	2.0			O-muT
00		15	_	1	-	6.75		15440)	Contract to the	741
1" Level	VIII	1		2.0			- 10	2 12	-	191
67	.10	5.0	40	-	4.0	2.75	20 6,11	4.0	_	Vdc
		10000	1 1 1 1 1 1	THO!			_	100.00		Tum-Or
09	-			-	12.5		ory :01	Other action controls	en (0,T) =	Hidi
evicel	lou	1 2	12.0			0.20		70.100		mAdo
	·OH	5.0	-3.0		-24	-5.0	80.01		an Schiller	Haz
00.00				-						The for
		2000		1 130	HILL DOUGHERS	ELMIN TERRORISM		AND DESIGNATION		
			1	verter.	AL PHE ME D	PERDANDARIO A	olvab 101	THE STREET	Podranda i	witching
ink	lou				-		_	-	_	mAdo
IIIK .	OL				-					IIIAGC
			100000000000000000000000000000000000000			1	1.2.			
DUTPUT.	LEVEICAL	ENRES		2011	3.4	BALIUSSI	LUDZ TU	THE TA	HAAL T	mAdo
	ЮН				2.1	-50	1.10	1.7	1115	MAGC
ource								1000	-	
		7.00		-			_	1000000		
	= maV		1 200	-	0.00		-			
	-			-	-				3/3	-
ink	IOL					1		100000		mAdd
	10				1					1 4 5
	1		3.6		3.0	La Company Company	S. J. C. 1997 11		1000	
			-					- ALC:		μAdc
) 55		15	-	± 0.3	7			-	±1.0	μAdc
	Cin	-		-	-	5.0	7.5	- 1	-	pF
e)	IDD	5.0		0.25	b	0.0005	0.25	(qn)-bezer	7.5	μAdc
		10	-	0.50	-	0.0010	0.50	-	15	
		15		1.00	-	0.0015	1.00	-	30	
evice)	IDD	5.0	-	1.0	-	0.0005	1.0	-	7.5	μAdc
		10	-	2.0	-	0.0010	2.0	-	15	
		15	-	4.0	-	0.0015	4.0	-	30	
I and Do	TIT	5.0		R	IT = (0	.7 µA/kHz	f + IDD	6	1	μAdo
, Per Gate)	1-19-1	10		1995	IT = (1	4 HA/KHZ	f + IDD	6		
The same of	S 11 1	15		11111		2 MA/kHz				
	1" Level 1" Level evice) ource ink P Device) ource ink	1" Level	Symbol Vdc	Symbol Vdc Min O" Level VOL 5.0 -	Symbol Vdc Min Max	Symbol Vdc Min Max Min M	Symbol Vdc Min Max Min Typ	Symbol Vdc Min Max Min Typ Max	Symbol Voc Min Max Min Typ Max Min M	Symbol Volc Min Max Min Typ Max Min Max

^{*}T_{low} = -55°C for AL Device, -40°C for CL/CP Device T_{high} = +125°C for AL Device, +85°C for CL/CP Device †To calculate total supply current at loads other than 50 pF

where: \mathbf{I}_T is in $\mu \mathbf{A}$ (per package), \mathbf{C}_L in pF, \mathbf{V}_{DD} in Vdc, and f kHz is input frequency.

#Noise immunity specified for worst-case input combination.

Noise Margin for both "1" and "0" level =

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields: however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leqslant (V_{in} \text{ or } V_{out}) \leqslant V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g. either VSS or VDD).

 $I_T(C_L) = I_T(50 \text{ pF}) + 3 \times 10^{-3}(C_L - 50) \vee_{DD} f$

^{**}The formulas given are for the typical characteristics only at 25°C .

^{0.5} Vdc min @ V_{DD} = 5.0 Vdc 1.0 Vdc min @ V_{DD} = 10 Vdc

^{1.0} Vdc min @ V_{DD} = 15 Vdc

(VOL = 0.4 Vde)

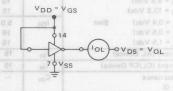
Characteristic	28°C	l askt	Symbol	V _{DD} Vdc	Min	Тур	Max	Unit
Output Rise Time [†] TLH = (1.2 ns/pF) C _L + 30 ns [†] TLH = (0.5 ns/pF) C _L + 20 ns	0	-	HUTTLH 80.0	5.0	T0,A	90 45	180	ns nov roque
tTLH = (0.4 ns/pF) CL + 15 ns				15		35	70	
Output Fall Time tTHL = (1.2 ns/pF) CL + 15 ns	10	9.65	tTHL	5.0	HOV	75 40	150 80	ns ns
THL = (0.5 ns/pF) C _L + 15 ns THL = (0.4 ns/pF) C _L + 10 ns				15	TIA	30	60	put Voltag
Turn-Off Delay Time tp_H = (1.5 ns/pF) C _L + 35 ns tp_H = (0.2 ns/pF) C _L + 20 ns tp_H = (0.15 ns/pF) C _L + 17.5 ns	4.50 6.75 6.75	-	^t PLH	5.0 10 15	FIIA	60 30 25	125 75 55	ns NB OV
Turn-On Delay Time tpHL = (1.0 ns/pF) CL + 10 ns tpHL = (0.3 ns/pF) CL + 15 ns tpHL = (0.2 ns/pF) CL + 15 ns	8,25	0.8	tPHL	5.0 10 15	- uoi	60 30 25	125 75 55	ns _{vy} B.F. oV)

* The formulae given are for the typical characteristics only. Switching specifications are for device connected as an inverter.

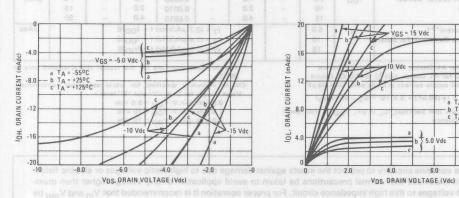
FIGURE 2 - TYPICAL OUTPUT SOURCE CHARACTERISTICS

FIGURE 3 - TYPICAL OUTPUT SINK CHARACTERISTICS

All unused inputs connected to ground

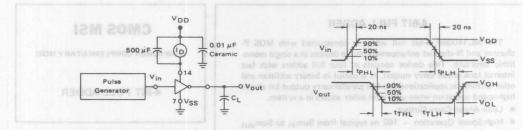


All unused inputs connected to ground.



VGS = 15 Vdc DRAIN CURRENT 12 a T_A = -55°C b T_A = +25°C c T_A = +125°C 8.0 01, Q8 210 0 Ti off 30 2.0 70 4.0 6.0 8.0

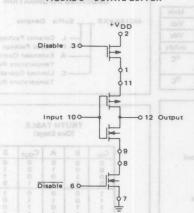
FIGURE 4 - SWITCHING TIME AND POWER DISSIPATION TEST CIRCUIT AND WAVEFORMS



APPLICATIONS ATT 1940G-WOLLOWT BRIVING TO SIGRED

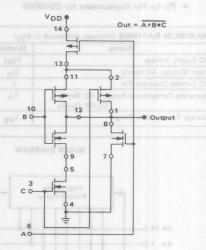
The MC14007UB dual pair plus inverter, which has access to all its elements offers a number of unique circuit applications. Figures 1, 5, and 6 are a few examples of the device flexibility.

FIGURE 5 - 3-STATE BUFFER



INPUT	DISABLE	OUTPUT		
1	0	0		
0	0	1		
X	1	Open		

FIGURE 6 - AOI FUNCTIONS USING TREE LOGIC



Substrates of P-channel devices internally connected to V_{DD} ; Substrates of N-channel devices internally connected to V_{SS} .

MC14008B

NC14007UB

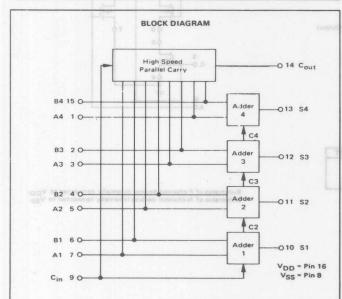
4-BIT FULL ADDER

The MC14008B 4-bit full adder is constructed with MOS Pchannel and N-channel enhancement mode devices in a single monolithic structure. This device consists of four full adders with fast internal look-ahead carry output. It is useful in binary addition and other arithmetic applications. The fast parallel carry output bit allows high-speed operation when used with other adders in a system.

- Look-Ahead Carry Output
- High-Speed Operation 160 ns typical from Sumin to Sumout
- Quiescent Current 5.0 nA/package typical @ 5 Vdc
- Diode Protection on All Inputs
- All Outputs Buffered
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range
- Pin-for-Pin Replacement for CD4008B

MAXIMUM RATINGS (Voltages referenced to VSS)

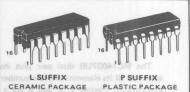
Rating	Symbol	Value	Unit	
DC Supply Voltage	V _{DD}	-0.5 to +18	Vdc	
Input Voltage, All Inputs	Vin	-0.5 to V _{DD} + 0.5	Vdc	
DC Current Drain per Pin	1	10	mAdc	
Operating Temperature Range – AL Device CL/CP Device	nperature Range – AL Device T _A -55 to +125		оС	
Storage Temperature Range	Tstg	-65 to +150	°C	



CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

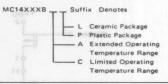
4-BIT FULL ADDER



CASE 620

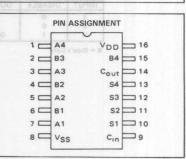
CASE 648

ORDERING INFORMATION



TRUTH TABLE (One Stage)

0 0 0 0	n B		C _{out}	S	
0	0	0	0	0	
0	0	1	0	1	
0	1	0	0	1	
0	An.	01.1.0	1	0	
1	0	0	0	1	
1	0	1	1	0	
1	1	0	1	0	
1	1	1	1	1	



	-	VDD	T _{low} *		25°C			Thigh*		
. Characteristic	Symbol	Vdc	Min	Max	Min	Тур	Max	Min	Max	Unit
Output Voltage "0" Level	VOL	5.0		0.05		0	0.05	-	0.05	Vdd
V: Vpp or 0	02	10	-	0.05	-	0	0.05	- 1	0.05	ndmo
		15	98 _	0.05		0	0.05	10 1 30	0.05	HUT
"1" Level	VOH	5.0	4.95	_	4.95	5.0	- 277	4.95	19 At 1 1-1	Vdc
Vin 0 or VDD	VOH	10	9.95	_	9.95	10	801	9.95		vac
A IU O OL A DD		15	14.95	JETT	14.95	15		14.95	emi7_fis i	ugniO
	1 1/	13	14.33	-	14.00	13	20	14.55	enan d. m	Vdc
Input Voltage "0" Lev	el V _{IL}	5.0				2.25	1.5	FIC: + 1	1.5	Vac
(V _O = 4.5 or 0.5 Vdc)		5.0		1.5	I	2.25	3.0	8 + 10 (F)	3.0	JHT
(V _O = 9.0 or 1.0 Vdc)	-	10		3.0		4.50	4.0	-	4.0	-
(V _O = 13.5 or 1.5 Vdc)		15	-	4.0	-	6.75	4.0	IMIT I	-	SSQ019
"1" Lev	el VIH							7001		HIS .
(V _O = 0.5 or 4.5 Vdc)	-	5.0	3.5 ·	-	3.5	2.75	13713d/	3.5	M61-H18	Vdc
(V _O = 1.0 or 9.0 Vdc)		10	7.0		7.0	5.50	10 fild/st	7.0	Hdj-H7d	1
(V _O = 1.5 or 13.5 Vdc)		15	11.0	-	11.0	8 25	JOE Floh	11.0	Mdj-H7d	
Output Drive Current (AL Device)	ІОН							MO A		mAd
(VOH = 2.5 Vdc) Source	-	5.0	-3.0		-2.4	-4.2	12/1741	-1.7	Hay Hild	
(VOH = 4.6 Vdc)	1	5.0	-0.64	-	-0.51	-0.88	13 Tables	-0.36	HALTHTA	100
(VOH = 9.5 Vdc)		10	-1.6		-1.3	-2.25	TO LADA	-0.9	Hd, THTd	
(VOH = 13.5 Vdc)	11	15	-4.2		-3.4	-8.8	-	-2.4	PS oT ut A	1873
(V _{OL} = 0.4 Vdc) Sink	IOL	5.0	0.64	-	0.51	0.88	Jun Trigg	0.36	M215 1971 A	mAd
(Max = 0 E Mda)	00	10	1.6	_	1.3	2.25	The street can	0.9	HUT HILL	
(V _{OL} = 0.5 Vdc)		15	4.2	-	3.4	8.8	JO (Reli	2.4	Hdj H7d	
Output Drive Current (CL/CP Device)	IOH-					20	0.15.4	6 V. H = 1	12 61 61 V	mAd
(VOH = 2.5 Vdc) Source	-OH	5.0	-2.5	_	-2.1	-4.2	JD (Figla Co.	-1.7	PLH-1PH	1
		5.0	-0.52		-0.44	-0.88	March 1971	-0.36	PUH. ISH	
(V _{OH} = 4.6 Vdc) (V _{OH} = 9.5 Vdc)		10	-1.3		-1.1	-2.25	JOT(Roll	-0.9	Mai_HTA	
(V _{OH} = 13.5 Vdc)		15	-3.6		-3.0	-8.8	the typic	-2.4	wip estur	ne for
			-	-	-	-	and St. Ollo	0.36		mAd
(VOL = 0.4 Vdc) Sink	IOL	5.0	0.52	_	0.44	0.88	-			mAd
(V _{OL} = 0.5 Vdc)		10	1.3	-	1.1	2.25	-	0.9	_	
(V _{OL} = 1.5 Vdc)	ste doid or	15	3.6	maatus	3.0	8.8	circuitre	2.4	entush z	dT.
Input Current (AL Device)	lin	15	ve āt as	± 0.1	hohūsa	± 0.00001	± 0.1	alula al	± 1.0	μAdd
Input Current (CL/CP Device)	nooslin i	15	modern	± 0.3	sio sons	±0.00001	± 0.3	espistion	±1.0	μAdd
Input Capacitance (V _{in} = 0)	Cin	-		gV>	U0 V 10	5.0	7.5	to the s	strained	pF
Quiescent Current (AL Device)	IDD	5.0		5.0	-	0.005	5.0	-	150	μAde
(Per Package)	00	10	-	10	-	0.010	10	-	300	1
		15	-	20	-	0.015	20		600	
Quiescent Current (CL/CP Device)	1 _{DD}	5.0	-	20	1 -	0.005	20		150	µАd
(Per Package)		10	-	40		0.003	40		300	מאת
THE PART OF THE PA		15	-	80	1993	0.015	80	10 -	600	
The state of the s	IT		+	1 00				and sylv	600	1
Total Supply Current**†	5.0	I _T = (1.7 μA/kHz) f + I _{DD}					μAd			
	selv - day	10				3.4 µA/kHz)				
Per Package)		15	T = (5.0 μA/kHz) f + IDD						1	
(CL = 50 pF on all outputs, all buffers switching)	016									

^{*}T_{Iow} = -55°C for AL Device, -40°C for CL/CP Device.
Thigh = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc

^{2.5} Vdc min @ VDD = 15 Vdc

[†]To calculate total supply current at loads other than 50 pF: $I_{T}(C_{L}) = I_{T}(50 \text{ pF}) + 5 \times 10^{-3} \text{ (}C_{L} - 50\text{) V}_{DD}f$ where: I_{T} is in μ A (per package), C_{L} in pF, V_{DD} in Vdc, and f in kHz is input frequency. **The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS* (CL = 50 pF, TA = 25°C)

Characteristic QVT	rije/i	Symbol	V _{DD} Vdc	Min	Тур	Max	Unit
Output Rise Time,		tTLH		01 30	13 18000	0.56	ns
^t TLH = (3.0 ns/pF) C _L + 30 ns			5.0	-	100	200	Echa Bla
tTI H = (1.5 ns/pF) Ci + 15 ns			10	-	50	100	
^t TLH = (1.1 ns/pF) C _L + 10 ns	30.0		15	O TION	40	80	es iiiV
Output Fall Time, again	14.85	tTHL	10.00	ai			ns
t _{THL} = (1.5 ns/pF) C _L + 25 ns			5.0	- W	100	200	anatio V ma
tTHL = (0.75 ns/pF) CL + 12.5 ns			10		50	100	(Vo 4.5
tTHL = (0.55 ns/pF) CL + 9.5 ns			15	0 -	40	80	02 6V
Propagation Delay Time	t	PLH, TPHL	- 1	8		(abV 3.6 to	ns V
Sum In to Sum Out				VIN	fove J "1"		
tplH, tpHL = (1.7 ns/pF) CL + 315 ns	35		5.0	00 -	400	800	1Vo - 0.5
tpLH, tpHL = (0.66 ns/pF) CL + 127 ns	08		10	0 -	160	320	0.1 -0VI
tpLH, tpHL = (0.5 ns/pF) CL + 90 ns	OFF		15	8 -	115	230	IVO-15
Sum In to Carry Out	-			HOT	Texture 1	C 12.1 (mercu	Select three
tplH, tpHL = (1.7 ns/pF) CL + 220 ns	1 3 -		5.0	1 100	305	610	S = HOV
tpLH, tpHL = (0.66 ns/pF) CL + 112 ns	180-		10		145	290	A HOV
tpLH, tpHL = (0.5 ns/pF) CL + 85 ns	2		15	-	110	220	EE = HOV
Carry In to Sum Out						1964/2	
tpLH, tpHL = (1.7 ns/pF) CL + 290 ns			5.0		375	750	EL - HOAL
tpLH, tpHL = (0.66 ns/pF) CL + 122 ns	140		10	0.5 _101	155	310	10 = 10 VI
tpLH, tpHL = (0.5 ns/pF) CL + 90 ns	1 3 1		15	0 _	115	230	10 × 10 V
Carry In to Carry Out	9.6		EA E	8		Vdef	11 × 10 M
tpLH, tpHL = (1.7 ns/pF) CL + 85 ns			5.0	-801	170	340	aput Drive
tpLH, tpHL = (0.66 ns/pF) CL + 42 ns	Diam's		10	0	75	150	IVOH 2
tpLH, tpHL = (0.5 ns/pF) CL + 30 ns	140-		15	0.	55	110	A HOV

*The formulae given are for the typical characteristics only.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields: however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leqslant (V_{in} \text{ or } V_{out}) \leqslant V_{DD}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g. either V_{SS} or V_{DD}).

FIGURE 1 – TYPICAL SOURCE CURRENT CHARACTERISTICS TEST CIRCUIT

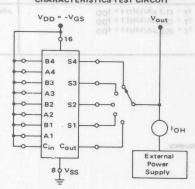


FIGURE 2 – TYPICAL SINK CURRENT CHARACTERISTICS TEST CIRCUIT

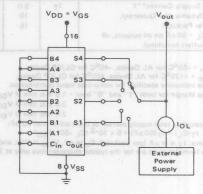


FIGURE 3 - DYNAMIC POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

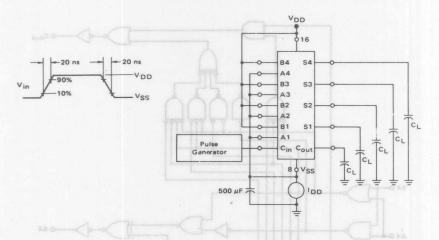
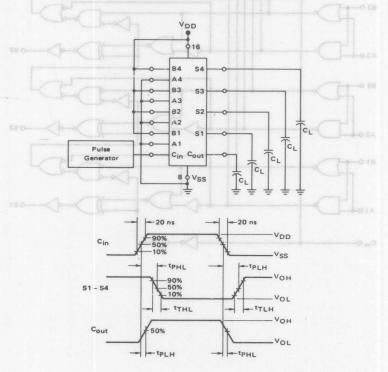
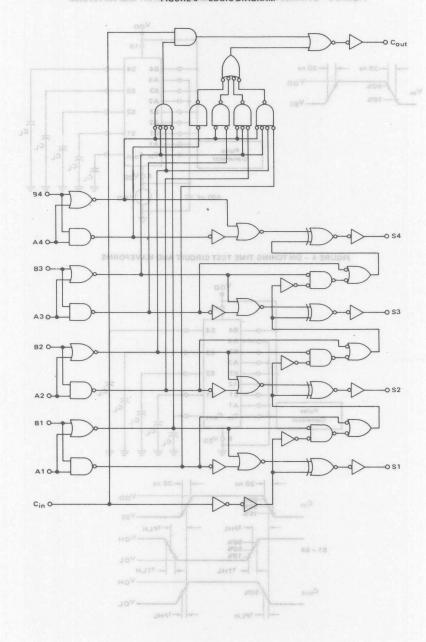


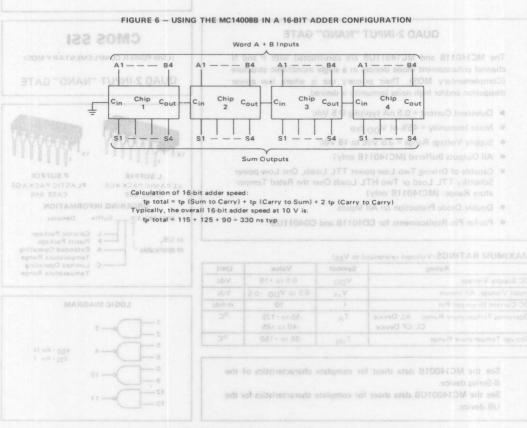
FIGURE 4 - SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

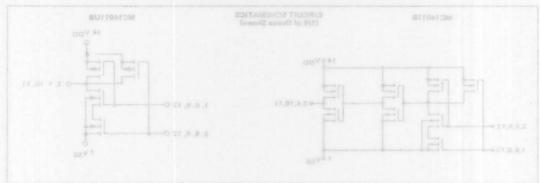






TYPICAL APPLICATION





MC14011B MC14011UB

QUAD 2-INPUT "NAND" GATE

The MC14011B and MC14011UB are constructed with P and N channel enhancement mode devices in a single monolithic structure (Complementary MOS). Their primary use is where low power dissipation and/or high noise immunity is desired.

- Quiescent Current = 0.5 nA typ/pkg @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typ
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered (MC14011B only)
- Capable of Driving Two Low power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range. (MC14011B only)
- Double Diode Protection on All Inputs
- Pin-for-Pin Replacements for CD4011B and CD4011UB **** OEE = GE + B1

MAXIMUM RATINGS (Voltages referenced to Vss)

Rating	Symbol	Value	Unit	
DC Supply Voltage	VDD	-0.5 to +18	Vdc	
Input Voltage, All Inputs	Vin	-0.5 to V _{DD} -0.5	Vdc	
DC Current Drain per Pin	1	10	mAdo	
Operating Temperature Range AL Device CL/CP Device	TA	-55 to +125 -40 to +85	оС	
Storage Température Range	T _{stg}	-65 to +150	оС	

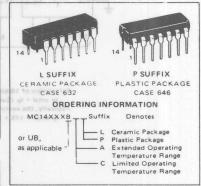
See the MC14001B data sheet for complete characteristics of the B-Series device.

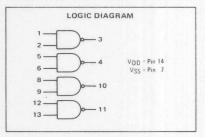
See the MC14001UB data sheet for complete characteristics for the UB device.

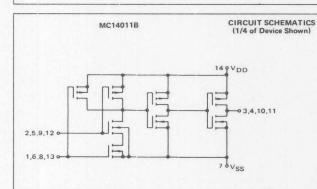
CMOS SSI

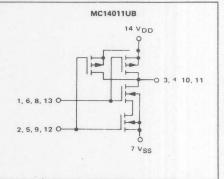
(LOW POWER COMPLEMENTARY MOS)

QUAD 2-INPUT "NAND" GATE









3



MC14012B MC14012UB

DUAL 4-INPUT "NAND" GATE

The MC14012B and MC14012UB are constructed with P and N channel enhancement mode devices in a single monolithic structure (Complementary MOS). Their primary use is where low power dissipation and/or high noise immunity is desired.

- Quiescent Current = 0.5 nA typ/pkg @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typ
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered (MC14012B only)
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range. (MC14012B only)
- Double Diode Protection on All Inputs
- Pin-for-Pin Replacements for CD4012B and CD4012UB

MAXIMUM RATINGS (Voltages referenced to VSS)

Rating	Symbol	Value	Unit
DC Supply Voltage	VDD	-0.5 to +18	Vdc
Input Voltage, All Inputs	Vin	-0 5 to V _{DD} -0 5	Vdc
DC Current Drain per Pin	1	10	mAdc
Operating Temperature Range AL Device CL/CP Device	TA	-55 to +125 -40 to +85	оС
Storage Temperature Range	T _{stg}	-65 to +150	оС

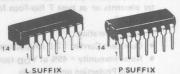
See the MC14001B data sheet for complete characteristics of the B-Series device.

See the MC14001UB data sheet for complete characteristics for the UB device.

A G BAYT CMOS SSI

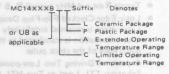
(LOW POWER COMPLEMENTARY MOS)

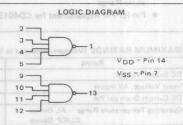
DUAL 4-INPUT "NAND" GATE

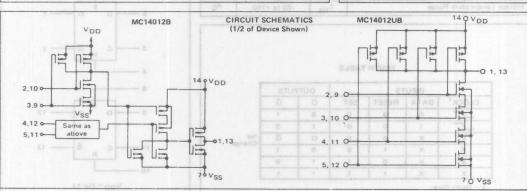


L SUFFIX CERAMIC PACKAGE CASE 632 P SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION







MC14013B

DUAL TYPE D FLIP-FLOP

The MC14013B dual type D flip-flop is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. Each flip-flop has independent Data, (D), Direct Set, (S), Direct Reset, (R), and Clock (C) inputs and complementary outputs (Q and Q). These devices may be used as shift register elements or as type T flip-flops for counter and toggle applications.

- Static Operation
- Quiescent Current = 2.0 nA/package typical @ 5 Vdc
- Noise Immunity = 45% of VDD typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Single Supply Operation
- Toggle Rate = 4 MHz typical @ 5 Vdc
- Logic Edge-Clocked Flip-Flop Design
 Logic state is retained indefinitely with clock level either high or low; information is transferred to the output only on the positive-going edge of the clock pulse
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range
- Pin-for-Pin Replacement for CD4013B

MAXIMUM RATINGS (Voltages referenced to VSS)

Rating	Symbol	Value	Unit
DC Supply Voltage	V _{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	Vin	-0.5 to V _{DD} + 0.5	Vdc
DC Current Drain per Pin	1	arts and 10 salvators	mAdc
Operating Temperature Range AL Device ST CL/CP Device	TA	-55 to +125 -40 to +85	°C
Storage Temperature Range	T _{stg}	-65 to +150	°C

TRUTH TABLE

	PUTS	OUT		INPUTS							
7	ā	Q	SET	RESET	DATA	CLOCK					
	1	0	0	0	0	_					
	0	1	0	0	1	5					
No Change	ā	Q	0	0	×	7					
Change	1	0	0	1	×	X					
	0	. 1	lo cr	0	×	X					
7	- 1	1	1	1	V	~					

X = Don't Care

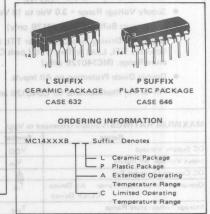
† = Level Change

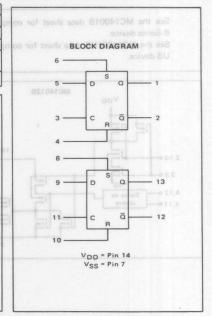
PIE BUSIO CMOS SSIM BOT

ID" GATE

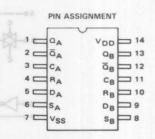
(LOW-POWER COMPLEMENTARY MOS)

plotogram An 3.0 = mmuO messau0





		2007	-199	VDD	10	ow*		25°C			igh*	
	Characteris	stic SYT	Symbol	ol Vdc	Min	Max	Min	Тур	Max	Min	Max	Unit
Output \	/oltage	"O" Level	VOL	5.0	-	0.05	-	0	0.05	-	0.05	Vd
Vin	V _{DD} or 0	001	0.	10	-	0.05	-	0	0.05	00 + 10	0.05	- H.3
	08	00		15	-	0.05	- 1	0	0.05	CL + 15	0.05	- H7.
		"1" Level	VOH	5.0	4.95		4.95	5.0		4.95	THE REAL PROPERTY.	Vd
V _{in}	0 or V _{DD}		VOH	10	9.95	7833	9.95	10	_	9.95	praid his	rugiu
* III	00000	100	-	15	14.95	_	14.95	15		14.95	(Rohan d.)	- 3H
	100	"0" Level	1/	13	14.55		14.00	15	- sn 2.	211101	Parison of the	Vde
Input Vo			VIL	5.0		1.5		2.25	1.5	OC + 12	1.5	Vuc
	4.5 or 0.5 Vdc			10	-	1.5	_	4.50	3.0	smill	3.0	seego:
	9.0 or 1.0 Vdd			15		81,2127			4.0	_	4.0	Clack
100=	13.5 or 1.5 Vo			15	-	4.0	-	6.75	4.0	AR (1)	4.0	+
111	081	11" Level	VIH					62.00	IpF) CL	n 88.0) =	THE BHIL	1
	0.5 or 4.5 Vdd			5.0	3.5	-	3.5	2.75	# J3 (3c	3.5	THAIRM	Vdc
-	1.0 or 9.0 Vdc			10	7.0	-	7.0	5.50	-	7.0	0.0	591 10
	1.5 or 13.5 Vo		-	15	11.0	-	11.0	8.25	* 13 (Re	11.0	Judi III	
	rive Current (A	CONTRACTOR STREET	ІОН					42 ns	/gFI CL	n 00:0) =	LH- TPHL	mAd
	= 2.5 Vdc)	Source		5.0	-3.0	-	-2.4	-4.2	+ JD (Rg	1.7	THE SHIP	43
	= 4.6 Vdc)	Sking and		5.0	-0.64	-	-0.51	-0.88	-	-0.36	TO of	Reserv
	= 9.5 Vdc)	380		10	-1.6	-	-1.3	-2.25	+ 50 (94	-0.9	JHF HJ	1
(VOH	= 13.5 Vdc)	001		15	-4.2	-	-3.1	-8.8	13-(3a)	-2.4	HOT.H.	10
(VOI	= 0.4 Vdc)	Sink	IOL	5.0	0.64	-	0.51	0.88	+ 10 (30	0.36	JHT HJ	mAd
(VOL	= 0.5 Vdc)	20	00	10	1.6	-	1.3	2.25	-	0.9	- terr	T quit
(VOI	= 1.5 Vdc)	10		15	4.2	1084	3.4	8.8	_	2.4	-	
Output D	rive Current (C	I /CP Device)	ГОН									mAd
	= 2.5 Vdc)	Source	·OH	5.0	-2.5	-	-2.1	-4.2	_	-1.7	- 101	-
	= 4.6 Vdc)	Or	20	5.0	-0.52	122	-0.44	-0.88	_	-0.36		1.00
	= 9.5 Vdc)	7.5	25	10	-1.3	_	-1.1	-2.25	_	-0.9	_	13.4
	= 13.5 Vdc)	126	D36	15	-3.6		-3.0	-8.8		-2.4	rishatal/ and	
			1062	1		Market 1	1977				100071 001	lock file
	= 0.4 Vdc)	Sink	IOL	5.0	0.52	-	0.44	0.88	-	0.36		mAd
	= 0.5 Vdc)			10	1.3		1.1	2.25	-	0.9	-	
	= 1.5 Vdc)	0,4		1.00	3.6	- ml	3.0	8.8	-	2.4	ise Freque	Solpol
	rrent (AL Devic		lin	15	-	± 0.1	-	±0.00001	± 0.1	-	± 1.0	μAdd
Input Cu	rrent (CL/CP D	evice)	lin	15	-	± 0.3	-	±0.00001	± 0.3	-	±1.0	μAdd
Input Cap	pacitance		Cin	- 0	-	HJT	-	5.0	7.5	DER 116-1 D	DE REEL SAL	pF
(Vin	= 0)	-				JHT						
Quiescen	t Current (AL D	Device)	IDD	5.0		1.0	_	0.002	1.0	_	30	μAdo
	ackage)	128	Ultis	10	-	2.0	1987 _	0.002	2.0	dibiW	60	bns 25
-5161		50	100	15		4.0	_	0.006	4.0	_	120	
Outosoon	t Current (CL/C	'P Davissa'	- 30	5.0		4.0		0.002	4.0		30	-
	ackage)	r Device)	IDD	10		8.0	ino abita	0.002	8.0			μAde
(rei r	ackage/				-		1110 2008	0.004	16	101_010.0	60	mož sr
				15	-	16	_				120	
Total Sup	oply Current**		IT	5.0			1T = (C).75 μA/kHz)f+ IDD			μAdd
(Dyna	amic plus Quies	ent, soltage on	o high sta	10	ernab ter		adTot (1	.5 μA/kHz	f + IDD			Firit
	'ackage)	ny voltage bi	to noite	15	ove of h		T = (2	.3 μA/kHz	f + DD			worl
	50 pF on all or	itputs, all	nonst el 1		to record							BUTT
											-	
Tlow	55°C for AL De	rice, -40°C for C	L/CP Device					O UAL SO				
Thigh = +	125°C for AL L	Device, +85°C for	CL/CP Dev	ice.	anna mife							
		for worst-case in " and "O" level =			= 5.0 V/de							
ivoise ivia	ingin for both T	and o level -	2.0 Vdc mi									
			2.5 Vdc mi									
		current at loads		O oF.								
To calcu	late total supply											
	late total supply											
17(0	CL) - IT (50 pF)	+ 2 x 10 ⁻³ (C _L - package), C _L in p	50) V _{DD} f				ency.			DIAL C	SSIGNMEN	



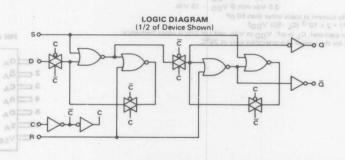
SWITCHING CHARACTERISTICS* (C1 = 50 pF, TA = 25°C)

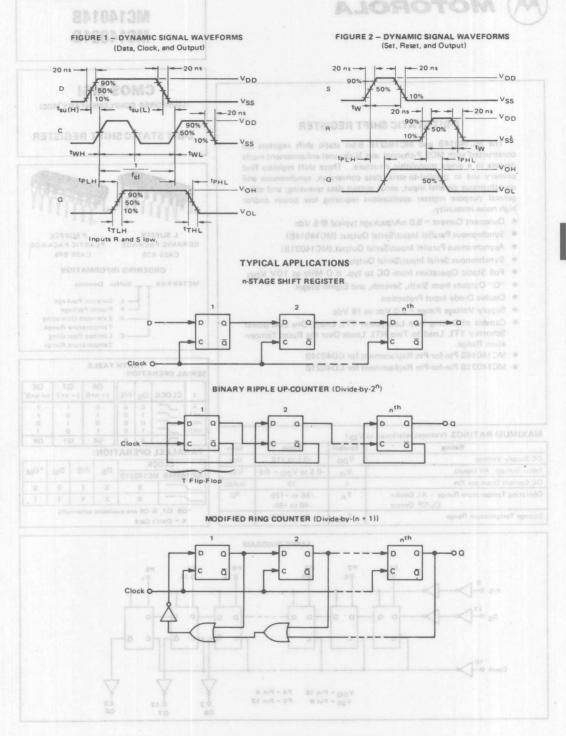
Max Just	Characteris	tic	avT 1	0150	Symbol	- Stin	DD'	nh'U	Min		Тур	Max	Uni
Output Rise Time tTLH = (3.0 ns/pF) tTLH = (1.5 ns/pF) tTLH = (1.1 ns/pF)	CL + 15 ns	0.05	0 0		0.05 0.05		5.0 10 15	6.0 10 15	10 _A		100 50 40	200 100 80	ns / pond
Output Fall Time tTHL = (1.5 ns/pF) tTHL = (0.75 ns/pF tTHL = (0.55 ns/pF	C _L + 25 ns		10	9.95 14.95	tTHL	96.9	5.0 10	10	HOV	leve	100 50 40	200 100 80	ns ni V
Propagation Delay Clock to Q TPLH, TPHL TPLH, TPHL Set to Q TPLH, TPHL	Time = (1.7 ns/pF = (0.66 ns/p) = (0.5 ns/pF = (1.7 ns/pF) = (0.66 ns/p) = (0.5 ns/pF) = (1.7 ns/pF) = (1.7 ns/pF) = (0.66 ns/pF)) C _L + F) C _L +) C _L + F) C _L +) C _L +	+ 42 ns 25 ns 90 ns + 42 ns 25 ns 265 ns + 67 ns	3.8 11.0 11.0 -2.4 -1.3	tPLH tPHL	3.8 7.0 7.0 11.0 -3.0 -7.6 -4.2	5.0 10 15 5.0 10 15 5.0 10	5.0 16 10 16 5.0 5.0 10		lovs	175 75	350 150 100 350 150 100 450 200	o ns ovi ovi ovi ovi ovi
Setup Times	= (0.5 ns/pF) CL +	50 ns 0	0.51 1.3 3.4	t _{su}	1.6	5.0 10 15	10	40 20		75 20 10 7.5	(a6.150 g a (a6.45) (a	Jo Vns
Hold Times	-1.7 -0.0- -0.9	=	-4.2 -0.88 -2.25	-2.1 -0.44 -1.1	th	-2.5 -0.52 -1.3	5.0 10 15	5.0 6.0	15 40 20 15		7.5 20 10 7.5	cive (Turenti (DI = 2.5-Vdc) = 4.5-Vdc) = 9.5-Vdci	HO VINS
Clock Pulse Width	0.36		-9.8 0.88 2.25	0.44	WL, ^t WH	0.52	5.0 10 15	5.0	250 100 70		125 50 35	* 13.5 Vdc) - (0.6—Vdc) - (0.5—Vdc) - (0.5—Vdc)	10 Vns
Clock Pulse Freque	ncy	101	8.8 ±0.00001	3.0	f _{Cl}	0.5	5.0 10 15	16	- 5		4.0 10 14	2.0 5.0 7.0	MH
Clock Pulse Rise an	d Fall Time	7.6	5.0		tTLH tTHL		5.0 10 15	-	c <u>i</u> n		-	15 5.0 4.0	μs
Set and Reset Pulse	Width	2.0	0.084	tW	L, ^t WH	-	5.0 10 15	16	250 100 70		125 50 35	(508.436	ns

*The formulae given are for the typical characteristics only.

e === e0

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields: however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that Vin and Vout be constrained to the range $V_{SS} \leqslant (V_{in} \text{ or } V_{out}) \leqslant V_{DD}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g. either V_{SS} or V_{DD}).







MC14014B MC14021B

WAL WAVEFORMS

NCISULER

8-BIT STATIC SHIFT REGISTER

The MC14014B and MC14021B 8-bit static shift registers are constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These shift registers find primary use in parallel-to-serial data conversion, synchronous and asynchronous parallel input, serial output data queueing; and other general purpose register applications requiring low power and/or high noise immunity.

- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- Synchronous Parallel Input/Serial Output (MC14014B)
- Asynchronous Parallel Input/Serial Output (MC14021B)
- Synchronous Serial Input/Serial Output
- Full Static Operation from DC to typ. 6.0 MHz at 10V VDD
- · "Q" Outputs from Sixth, Seventh, and Eighth Stages
- Double Diode Input Protection
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load to Two HTL Loads Over the Rated Temperature Range.
- MC14014B Pin-for-Pin Replacement for CD4014B
- MC14021B Pin-for-Pin Replacement for CD4021B

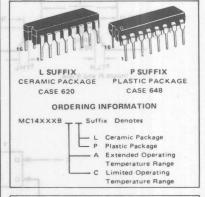
MAXIMUM RATINGS (Voltages referenced to VSS)

Rating	Symbol	Value	Unit
DC Supply Voltage	VDD	-0.5 to +18	Vdc
Input Voltage, All Inputs	Vin	-0.5 to V _{DD} + 0.5	Vdc
DC Current Drain per Pin	1	10	mAdc
Operating Temperature Range AL Device CL/CP Device	TA	-55 to +125 -40 to +85	°C
Storage Temperature Range	T _{stg}	-65 to +150	°C

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

8-BIT STATIC SHIFT REGISTER



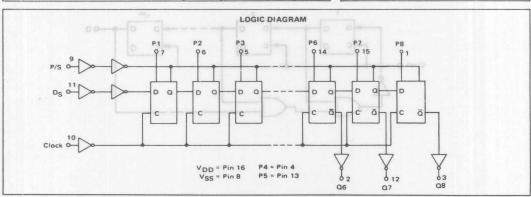
TRUTH TABLE

SERIA	AL OPER	ATIC	ON:			
t	CLOCK	DS	P/S	Q6 t = n+6	Q7 t = n+7	Q8 t = n+8
n	5	0	0	0	?	?
n+1		1	0	1	0	?
n+2	5	0	0	0	1	0
n+3	5	1	0	1	0	1
		×	0	06	0.7	08

PARALLEL OPERATION:

CLOC	K	Ds	P/S	D	*QM	
MC14014B M	C14021B	US	F/3	DM		
	X	X	1	0	0	
	X	X	1	1	1	

*Q6, Q7, & Q8 are available externally X = Don't Care



Holi Lake		-000	VDD	Tio	w*		25°C	-	Thi	gh*	
Characteristi	c dAg	Symbol	Vdc	Min	Max	Min	Тур	Max	Min	Max	Unit
Output Voltage	"0" Level	VOL	5.0	-	0.05	-	0	0.05	-	0.05	Vdc
Vin = VDD or 0	100	-	10	-	0.05	-	0	0.05	CL = 30	0.05	PHOT
100	08	and the same	15	-	0.05	-	0	0.05	C(= 15	0.05	PHI
	"1" Level	VOH	5.0	4.95	-	4.95	5.0	_ 8	4.95	3g/sp 1.1	Vdc
Vin = 0 or VDD		011	10	9.95	3437	9.95	10	-	9.95	notification	Jugiu(
200	001		15	14.95	-	14.95	15	- 3	14.95	Rolan E.I	× 1977
Input Voltage#	"0" Level	VIL	. 0					en ê.	10 + 13	0.75 ns/pl	Vdc
(V _O = 4.5 or 0.5 Vdc)	40	-	5.0		1.5	-	2.25	1.5	81-01	1.5	1 340
(V _O = 9.0 or 1.0 Vdc)			10		3.0	-	4.50	3.0	(5) -nu1	3.0	noneron.
(VO = 13.5 or 1.5 Vdc)	000		15	4	4.0	-	6.75	4.0	Soles C. J	4.0	west.
dag	"1" Level	VIH	0				an \$1	1+101	atin 35.0	P M JQI	1497
(V _O = 0.5 or 4.5 Vdc)	811	- in	5.0	3.5	_	3.5	2.75	00 = 13	3.5	- ferror	Vdc
(V _O = 1.0 or 9.0 Vdc)	160	400	10	7.0		7.0	5.50	-	7.0	dristri eri	R stool
(VO = 1.5 or 13.5 Vdc)		175	15	11.0	HW/	11.0	8.25	-	11.0	ALIDARA DEL	1 3 30
Output Drive Current (AL			10 (1	11.0		11.0	0.20		11.0		mAdo
(VOH = 2.5 Vdc)	Source	ЮН	5.0	-3.0		-2.4	-4.2	-	-1.7		
(V _{OH} = 4.6 Vdc)			5.0	-0.64	102	-0.51	-0.88		-0.36	уэтыра	lock f
(V _{OH} = 9.5 Vdc)	0.8		10	-1.6	_	-1.3	-2.25	_	-0.9		
(V _{OH} = 13.5 Vdc)			15	-4.2	_	-3.4	-8.8	_	-2.4	_	
	150	000		-	11111	-	-	/11/2/2	0.36	-	mAde
(V _{OL} = 0.4 Vdc)	Sink at	OL	5.0	0.64	-	0.51	0.88	_	0.36		MAdd
(V _{OL} = 0.5 Vdc)	- 40	135	10	1.6	-	1.3	8.8		2.4	_	1
(V _{OL} = 1.5 Vdc)	180	350	15	4.2		3.4	8.8	-	2.4	257	T outs
Output Drive Current (CL/	The second secon	IOH	0								mAdd
(V _{OH} = 2.5 Vdc)	Source	69	5.0	-2.5	-	-2.1	-4.2	-	-1.7	-	
(V _{OH} = 4.6 Vdc)			5.0	-0.52	1914	-0.44	-0.88	-	-0.36	Con Figs. 7	Duty Cle
(V _{OH} = 9.5 Vdc)	- 1	11 34	10	-1.3		-1.1	-2.25	-	-0.9	-	
(V _{OH} = 13.5 Vdc)	-		15	-3.6	-	-3.0	-8.8	_	-2.4	-	-
(V _{OL} = 0.4 Vdc)	Sink	IOL	5.0	0.52	-	0.44	0.88	slowt with	0.36	win only	mAdd
$(V_{OL} = 0.5 \text{ Vdc})$			10	1.3	- "	1.1	2.25	sidili au	0.9	ANIB BUILD	1
$(V_{OL} = 1.5 \text{ Vdc})$			15	3.6	-	3.0	8.8	-	2.4	-	
Input Current (AL Device)		lin	15	-	± 0.1	-	±0.00001	±0.1	-	± 1.0	μAdd
Input Current (CL/CP Dev	ice)	e din or	15	nois toni	± 0.3	e element	±0.00001	± 0.3	ani - too	±1.0	μAdd
Input Capacitance	agettoy was	Cin	lio da bio	vs of no	sket Ted	апоілька	5.0	7.5	esivine a	ti Tava	pF
(V _{in} = 0)	afferies a fille	TO SINGE		V 6 40 110	2163 000	a internation	PIQ TENTING	The state of	SQLADE S		Section 1
Quiescent Current (AL De	vica)	1-0	5.0	0.180000	5.0	2012-93/01	0.005	5.0	2008110	150	μAdo
(Per Package)		IDD	10	14	10	tuo⊽ 10	0.010	10	the re	300	91100
100V7	ther Vss o	o .p.ol to	15	ov gigal	20	an_appr	0.015	20	is must	600	Unus
Outcomes Courses ICL ICE	Devise	las	5.0	-			0.005	20			
Quiescent Current (CL/CP	Device)	IDD	10	-	20	-	0.005	40	-	150	μAdo
(Per Package)			15		40	_	0.010	80	-	300	
		1-		-	80					600	1
Total Supply Current**†	NUT SINK CUI	TOUT	5.0				.75 μA/kHz				μAdd
(Dynamic plus Quiesce	nt,		10				.50 μA/kHz				
Per Package)	oov o		15			T = (2	.25 μA/kHz	11 + IDD			
(CL = 50 pF on all out	puts, all			-							
buffers switching)		-	-					+			

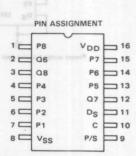
*T_{Iow} = -55°C for AL Device, -40°C for CL/CP Device.

Thigh = +125°C for AL Device, +85°C for CL/CP Device.

#Noise immunity specified for worst-case input combination.

Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc

Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc 2.0 Vdc min @ V_{DD} = 10 Vdc 2.5 Vdc min @ V_{DD} = 15 Vdc 1TO calculate total supply current at loads other than 50 pF: $I_{T}(C_{L}) = I_{T}(50 \, \text{pF}) + 1.5 \times 10^{-3} \, (C_{L} - 50) \, V_{DD}f$ where: I_{T} is in μ A (per package), C_{L} in pF, V_{DD} in Vdc, and f in kHz is input frequency. *The formulas given are for the typical characteristics only at 25° C.

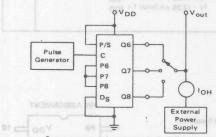


Max Unit	Charac	teristic	28°C	hild	Symbol	V _{DD} Vdc	Min	Тур	Max	Unit
Output Rise Time		0.05	0		TLH	5.0	1 JoV	level 'B'	190	ns alec
tTLH = (3.0 ns/pF)	CL + 30	ns 80.0			0.05	5.0	1 = 0	100	200	V = mV
tTLH = (1.5 ns/pF)	CL + 15	ns 20.0			0.08	10		50	100	
tTLH = (1.1 ns/pF)	CL + 10	ns			- 1	15	I I V	40	80	
Output Fall Time	9.95		101	28.6	tTHL	N. E			gg ^y t	ns
THL = (1.5 ns/pF)	C1 + 25 1	ns			1	5.0	_	100	200	
tTHL = (0.75 ns/pf	-) CL + 12	2.5 ns				10	JIV.	50	100	satioV ruen
tTHL = (0.55 ns/pf	CL + 9.	5 ns			arl	15	-	40	80 0 0	Annyl
Propagation Delay	Time (Clo	ck to Q,	P/S to Q)	1	tPLH,	0.1			156V 0.1 so f	ns
tPHL tPLH = (1.7 ns/pF	CL + 31	5 ns		tPHL	5.0	-	400	800	IVQ e 13
tPHL, tPLH = (10	+IV	170	340	
tpHL, tpLH = (0.5 ns/pF) CL + 90	ns		- 1	15 0.8	-	115	230	LO = GVI
Clock Pulse Width	2.0		5.50	0.1	twH	5.0	400	150	1904 0 6 10	ns
						10	175	75	abV EE1 no	T = OV
						15	135	40	Current IAL	sateut Ories
Clock Frequency	V.1-		5.4-	1.5-	fcl	5.0		3.0	1.5	MHz
					- 14	10 00	_	6.0	3.0	F-BOY
					- 18	15 01	_	8.0	4.0	P HOY!
Parallel/Serial Cont	trol Pulse V	Width	0.0-	2.0-	twH	5.0	400	150	1007 6.6	ns
						10 08	175	75	_1s6-V 8-	D= 10 VI
					-	15	135	40	_isbV a.	a down
Setup Time	675		0.8	9.5	t _{su}	5.0	350	150	T00A 6	ns
						10	80	50	Current (CL)	WinD Juqjul
					- 1	15 08	60	30	.5 Vdc <u>1</u>	(YON =
Input Clock Rise T			88.0-	PP:07	tr(cl)	5.0	_	_	15	μs
					1(01)	10	- 1	-	5	P-RCVI
					- 13	15	J	_	4	= HOV)

^{*}The formulae given are for the typical characteristics only.

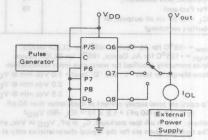
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields: however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leqslant (V_{in} \text{ or } V_{out}) \leqslant V_{DD}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g. either V_{SS} or V_{DD}).

FIGURE 1 - OUTPUT SOURCE CURRENT TEST CIRCUIT



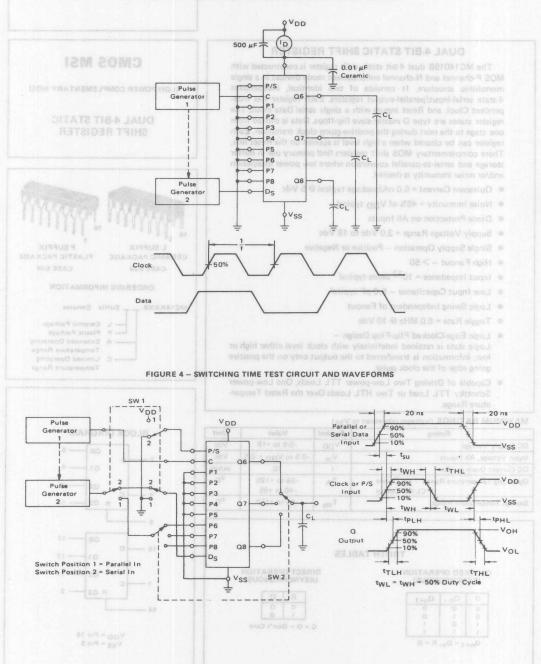
Preset output under test to a logic "1" level.

FIGURE 2 - OUTPUT SINK CURRENT TEST CIRCUIT



3-42

88 10 M 13 M FIGURE 3 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM



MC14015B

DUAL 4-BIT STATIC SHIFT REGISTER

The MC14015B dual 4-bit static shift register is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. It consists of two identical, independent 4-state serial-input/parallel-output registers. Each register has independent Clock and Reset inputs with a single serial Data input. The register states are type D master-slave flip-flops. Data is shifted from one stage to the next during the positive-going clock transition. Each register can be cleared when a high level is applied on the Reset line. There complementary MOS shift registers find primary use in buffer storage and serial-to-parallel conversion where low power dissipation and/or noise immunity is desired.

- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- Noise Immunity = 45% of VDD typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Single Supply Operation -- Positive or Negative
- High Fanout -> 50
- Input Impedance = 10¹² ohms typical
- Low Input Capacitance 5.0 pF typical
- · Logic Swing Independent of Fanout
- Toggle Rate = 6.0 MHz @ 10 Vdc
- Logic Edge-Clocked Flip-Flop Design —
 Logic state is retained indefinitely with clock level either high or
 low; information is transferred to the output only on the positive
 going edge of the clock pulse.
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range.

MAXIMUM RATINGS (Voltages referenced to Voc.)

Rating	Symbol	Value	Unit
DC Supply Voltage	VDD	-0.5 to +18	Vdc
Input Voltage, All Inputs	Vin	-0 5 to V _{DD} + 0.5	Vdc
DC Current Drain per Pin	1	10	mAdc
Operating Temperature Range AL Device CL/CP Device	TA	-55 to +125 -40 to +85	°C
Storage Temperature Range	T _{stg}	-65 to +150	°C

TRUTH TABLES

(SYNCHRONOUS)

D	Qn	Qn+1
0	0	0
0	1	0
1	0	1
1	1	1

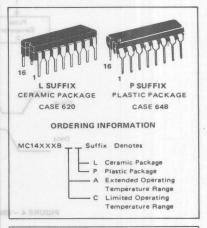
DIRECT OPERATION (ASYNCHRONOUS)

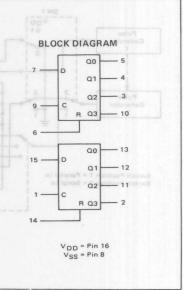


CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

DUAL 4-BIT STATIC SHIFT REGISTER





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		2660	VDD	Tio	w*		25°C	pitritati	Third Chara	gh*	
Characte	ristic	Symbol	Vdc	Min	Max	Min	Тур	Max	Min	Max	Unit
Output Voltage	"0" Level	VOL	5.0	-	0.05	-	0	0.05	06-7-10	0.05	Vdc
Vin VDD or 0		0.2	10	- 1	0.05	-	0	0.05	61 + 101	0.05	- 637
08			15	-	0.05	-	0	0.05	01 - 10	0.05	+ HJT
	"1" Level	VOH	5.0	4.95	HTT-	4.95	5.0	_	4.95	BITH E HET	Vdc
Vin O or VDD		0	10	9.95	-	9.95	10	- 8/1	9.95	19/en 8.11	- JHP
1001			15	14.95	-	14.95	15	en d.i	14.95	(0.75 nu/p	THL
Input Voltage [±]	"0" Level	VIL	-					NAME OF TAXABLE PARTY.	0.301	State St. O.	Vdc
(VO = 4.5 or 0.5 V			5.0		1.5		2.25	1.5	man I	1.5	1000019
(VO = 9.0 or 1.0 V	dc)		10	-	3.0	-	4.50	3.0	_ 0	3.0	0010
(VO = 13.5 or 1.5)	/dc)		15	-	4.0	-	6.75	4.0	in ("1) =	4.0	
200	"1" Level	VIH	1				- 614 7/61 4	Jes Lindik	1 00.01	HER WITH	
(Vo = 0.5 or 4.5 V			5.0	3.5		3.5	2.75	* 10 19d	3.5	HI9_HJ	Vdc
(VO = 1.0 or 9.0 V	dc)	100	10	7.0	-	7.0	5.50	-	7.0	Q or 1	15014
(VO = 1.5 or 13.5)			15	11.0	-	11.0	8.25	(pF) Cu	11.0	IKT_HJ9	
Output Drive Current	AL Device)	Іон	1 2					D (74)	- V-01	H17 302	mAdo
(VOH = 2.5 Vdc)	Source	·On	5.0	-3.0		-2.4	-4.2	POFF CL V	-1.7	ING RU	
(VOH = 4.6 Vdc)			5.0	-0.64	HWZ	-0.51	-0.88	-	-0.36	rise Width	FI XDQID
(VOH = 9.5 Vdc)		-	10	-1.6	-	-1.3	-2.25	_	-0.9		
(V _{OH} = 13.5 Vdc)		-	15	-4.2	_	-3.4	-8.8	_	-2.4	_	
(V _{OI} = 0.4 Vdc)	Sink	IOL	5.0	0.64	197-	0.51	0.88	-	0.36	Uparn sen	mAdo
(VOL = 0.5 Vdc)	0.0	IOL	10	1.6		1.3	2.25	_	0.9	_	1
(VOL = 1.5 Vdc)		-	15	4.2		3.4	8.8	_	2.4	_	
Output Drive Current	(CL (CR Davies)	1-0	10	310	7,8377	0.4	0.0	101	T 100 T 100	or selft self	mAdo
	Source	ІОН	5.0	-2.5		-2.1	-4.2	- 12	-1.7		Imade
(V _{OH} = 2.5 Vdc)	Source	_	5.0	-0.52		-0.44	-0.88		-0.36		
(V _{OH} = 4.6 Vdc) (V _{OH} = 9.5 Vdc)		000	10	-1.3	HIVE	-1.1	-2.25		-0.9	ristoliW outs	Reset F
(V _{OH} = 13.5 Vdc)		160	15	-3.6		-3.0	-8.8		-2.4		
	03	120		_		-			0.36		- 0.1
(V _{OL} = 0.4 Vdc)	Sink	OL	5.0	0.52	ugl	0.44	0.88		0.36	BITT	mAdo
$(V_{OL} = 0.5 \text{ Vdc})$		190	10	1.3	100-		2.25			_	
(V _{OL} = 1.5 Vdc)	0.5	25	15	3.6	-	3.0	8.8	-	2.4	_	-
Input Current (AL Dev		lin	15	-	± 0.1	-	±0.00001	±0.1	_	± 1.0	μAdc
nput Current (CL/CP	Device)	lin	15		± 0.3	skillio sz	±0.00001	± 0.3	יו פופַ יוטו	±1.0	μAdc
Input Capacitance (Vin = 0)		Cin	-	-	-	-	5.0	7.5		-	pF
Quiescent Current (AL	Device)	IDD	5.0	-	5.0	-	0.005	5.0	-	150	μAdc
(Per Package)			10	-	10	-	0.010	10	-	300	
		VAN ONA	15	TEST M	20	о явио	0.015	20	-	600	
Quiescent Current (CL	/CP Device)	lpp	5.0	-	20	-	0.005	20	-	150	μAdc
(Per Package)			10	00¥e	40	-	0.010	40	_	300	
			15		80	-	0.015	80	-	600	
Total Supply Current*	*†	IT 3	5.0	60	末1.00	IT = 11	1.2 µA/kHz				μAdc
(Dynamic plus Quit		3100	10	- 3			2.4 µA/kHz				MAGC
Per Package)			15	UQV S			3.6 µA/kHz				
(C ₁ = 50 pF on all	outputs, all			6400 0		1		MAX . DO			
buffers switching)				0110							

*Tlow = -55°C for AL Device, -40°C for CL/CP Device.

Thigh = +125°C for AL Device, +85°C for CL/CP Device.

Noise immunity specified for worst-case input combination.

Noise Margin for both "1" and "0" level = 1.0 Vdc min @ VDD = 5.0 Vdc.

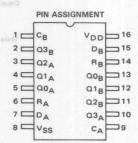
2.0 Vdc min @ V_{DD} = 10 Vdc 2.5 Vdc min @ V_{DD} = 15 Vdc

1 To calculate total supply current at loads other than 50 pF.

IT(C_L) = IT(50 pF) + 2'x 10⁻³ (C_L - 50) V_{DD}f

where: IT is in µA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.

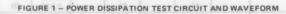
*The formulas given are for the typical characteristics only at 25°C.

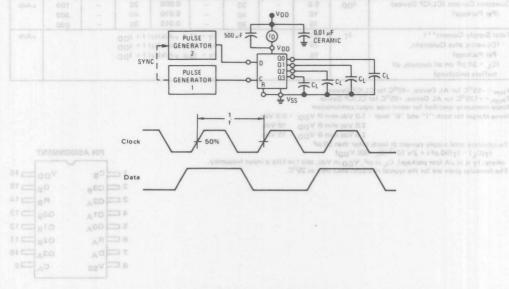


SWITCHING CHARACTERISTICS* (C1 = 50 pf. TA = 25°C)

Characteristic	2500		Symbol	VDD	Min	Тур	Max	Unit
Output Rise Time	Typ	nibl	* TLH	Vac 8	Symbol		Characteriati	ns
TLH = (3.0 ns/pF) CL + 30 ns			80.0	5.0	TOV	100	200	HaV ream
TLH = (1.5 ns/pF) C1 + 15 ns			80.0	10	200	50	100	V mV
TLH = (1.1 ns/pF) CL + 10 ns			80.0	15	- 1	40	80	
Output Fall Time	0.0	60.8	tTHL :	5.0 4	HOV	leved "I"		ns
THL = (1.5 ns/pF) CL + 25 ns			1 20	5.0	-	100	200	Vin De
THL = (0.75 ns/pF) CL + 12.5 ns				10	- 1	50	100	121
THL = (0.55 ns/pF) CL + 9.5 ns			-	15	TOV	40	80	and and the
Propagation Delay Time	2.25		tPLH,	5.0	1 1		Or D.S. Videl	ns
Clock, Data to Q			tPHL	01			fish V D. f. so.	18-0VI
tplH tpHL = (1.7 ns/pF) CL	+ 225 ns		0.4	5.0	_	310	750	
tpLH, tpHL = (0.66 ns/pF) C	+ 92 ns			10		125	250	
tpLH, tpHL = (0.5 ns/pF) CL Reset to Q	+ 65 ns		- 6	15 0.8	HIV	90		10 = 0V1
tplH tpHL = (1.7 ns/pF) CL	+ 375 ne		- 1 4	5.0		460	750	
tpLH, tpHL = (0.66 ns/pF) C	+ 147 pc		- 0	10		180	250	II-OV
tpLH, tpHL = (0.5 ns/pF) CL	+ 95 ns			15	HO!	120	170	atour Drive
Clock Pulse Width	88.0-	-0.61	twH s	5.0	-	185	400	ns
			1	10	-	85	175	
			0.1	15	- 1	55	135	S - HOAL
Clock Pulse Frequency	88.0	18.0	fcl	5.0	1-7	2.0	1.5	MHz
			- 0	10	30,	6.0	3.0	A 2 70.24
				15	- 1	7.5	3.75	10,48
Clock Pulse Rise and Fall Times	-	-	tTLH, tTHL	5.0	-	(P (Javice)	15	μs
	4.2		20	10	HO	Source	5	
			1 02	15		201006	5	HOV)
Reset Pulse Width	-2.25	117-	twH	5.0	400	200	Tiesv a	ns
			l ale	10	160	80	(55 V d.)	E HOV
				15	120	60		HOY
Setup Time	0000	1 777	1	5.0	350	100	Toby 8	ns
80 1 -			t _{su}	10	100	50		
			- 3	15	75	40	TobV 8	I a Jovi

^{*}The formulae given are for typical characteristics only.







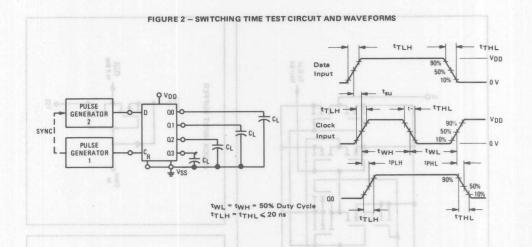
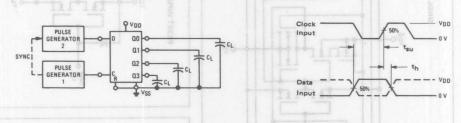
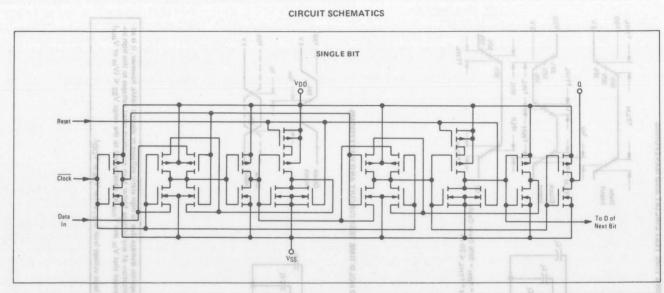


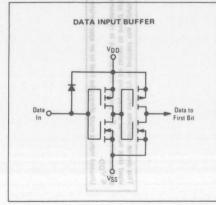
FIGURE 3 - SETUP AND HOLD TIME TEST CIRCUIT AND WAVEFORMS

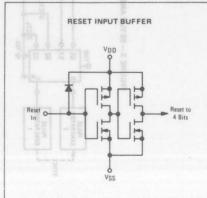


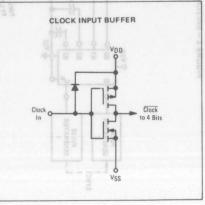
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in} \text{ or } V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD).

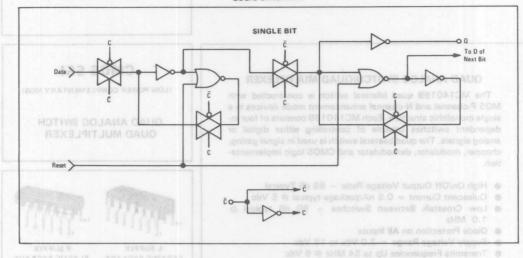


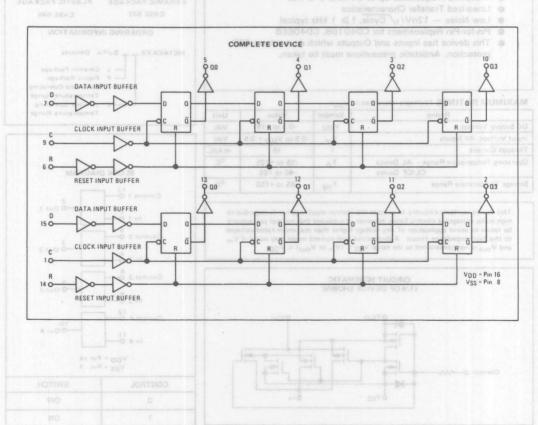






LOGIC DIAGRAMS





MC14016B

QUAD ANALOG SWITCH/QUAD MULTIPLEXER

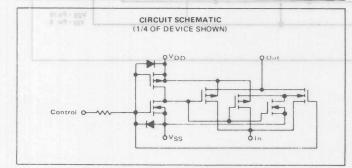
The MC14016B quad bilateral switch is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. Each MC14016B consists of four independent switches capable of controlling either digital or analog signals. The quad bilateral switch is used in signal gating, chopper, modulator, demodulator and CMOS logic implementation.

- High On/Off Output Voltage Ratio 65 dB Typical
- Quiescent Current = 0.5 nA/package typical @ 5 Vdc
- Low Crosstalk Between Switches 80 dB typical @ 1.0 MHz
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Transmits Frequencies Up to 54 MHz @ 5 Vdc
- Linearized Transfer Characteristics
- Low Noise 12nV/ √ Cycle, f ≥ 1 kHz typical
- Pin-for-Pin Replacement for CD4016B, CD4066B
- This device has Inputs and Outputs which do not have ESD protection. Antistatic precautions must be taken.

MAXIMUM RATINGS (Voltages referenced to VSS)

Rating	Symbol	Value	Unit
DC Supply Voltage	V _{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	Vin	-0.5 to V _{DD} + 0.5	Vdc
Through Current	f	10	mAdc
Operating Temperature Range - AL Device	TA	-55 to +125	°C
CL/CP Device		-40 to +85	
Storage Temperature Range	T _{stg}	-65 to +150	°C

This device contains circuitry to protect the control inputs agains+ damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit. A destructive high-current mode may occur if V_{in} and V_{out} is not constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$.



CMOS SSI

(LOW POWER COMPLEMENTARY MOS)

QUAD ANALOG SWITCH QUAD MULTIPLEXER



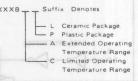


L SUFFIX
CERAMIC PACKAGE
CASE 632

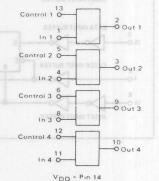
P SUFFIX
PLASTIC PACKAGE
CASE 646

CASE 64

ORDERING INFORMATION



BLOCK DIAGRAM



	ADD				
	Vss	12	Pin	7	
OI					

 CONTROL
 SWITCH

 0
 OFF

 1
 ON

	9109	Ser Rossia	VDD	TI	ow"		25°C	this par	1 h	igh "	
Characteristics	Figure	Symbol	Vdc	Min	Max	Min	Тур	Max	Min	Max	Unit
nput Voltage#	- 1	VIL	5.0	-	_	-	1.5	0.9	-	su o V o	Vdc
Control Input	- 3	1	10	-	-	-	1.5	0.9	01-10	J.OUV -	(VC
	- 0	3	15	a -	-	-	1.5	0.9	-	until of	loutro
	- 1 0	VIH	5.0	-	-	3.5	2.0	(04 01	= 50.0	OV EL >	Vdc
	- 3		10	-	-	8.0	6.0	-	-	-	
Vm - 06	- 0	8	15	8 -	-	13	(55.11) = 5	eVT1ug	WOTEL I	Copyre	RETURN'S
nput Current (AL Device) Control	0	lin	15	-	±0.1	-	±0.00001	±0.1	$ \cdot \cdot = mi$	±1.0	μAdc
nput Current (CL/CP Device) Control		lin	15	-	±0.3	7-7-59	±0.00001	±0.3	_	±1.0	μAdc
Input Capacitance	-	Cin					00	,sH66	0.1-1	0 × 0.1 ×	pF
Control			7	-	-	-	5.0 5.0	7.2100	040	00 - 31-1	
Switch Input Switch Output			I	-	-	-	5.0	Stud	Vo-		1
Feed Through	- 0		1		Jobs	0 = 8	0.2	Pulse Fa	none i	n Contro	amical
Quiescent Current (AL Device)	2,3	lon	5.0		0.25		0.0005	0.25		7.5	μAdc
(Per Package)	2,3	IDD	10		0.50	_	0.0005	0.50	_	15	1
(i el i dekage)	- 0	0	15	1.01	1.00		0.0015	1.00	0 - 30	30	V saiol
Quiescent Current (CL/CP Device)	2,3	IDD	5.0	-	1.0	-	0.0005	1.0	-	7.5	μAdc
(Per Package)	2,0	.00	10	_	2.0	-	0.0000	2.0	007 -	15	gV)
	_ 0		15	-	4.0	-	0.0015	4.0	-	30	241
"ON" Resistance (AL Device)	4,5,6	RON									Ohms
$(V_C = V_{DD}, R_L = 10 \text{ k}\Omega)$	- 0	0 -	-	-			(ebV	38		m Disto	and Vila
(V _{in} = +5.0 Vdc)			5.0	-	600	- 8	300	660 660	SIVIE SI	960	ni ^V l
$(V_{in} = -5.0 \text{ Vdc}) V_{SS} = -5 \text{ Vdc}$ $(V_{in} = \pm 0.25 \text{ Vdc})$					600	-	280	660	0.7 =	960	JR
(Vin = +7.5 Vdc)	- 0	0	7.5	83	360	- 22	240	400	DV P D	600	Olivision
$(V_{in} = +7.5 \text{ Vdc})$ $(V_{in} = -7.5 \text{ Vdc}) V_{SS} = -7.5 \text{ Vdc}$			7.5		360		240	400	0.75	600	EME
$(V_{in} = \pm 0.25 \text{ Vdc})$					360		180	400	100 0	600	reo.t
(Vin = +10 Vdc)			10		600		260	660	Min	960	
(Vin = +10 Vdc) (Vin = +0.25 Vdc) VSS = 0 Vdc			10		600		260	660		960	380
(V _{in} = +5.6 Vdc)				-	600	_	310	660	- 1	960	750
(Vin = +15 Vdc)			15	_	360		260	400	_	600	180
(V _{in} = +0.25 Vdc) V _{SS} = 0 Vdc	- 0	U	0 0		360	-	260	400	- 10	600	J. of
(V _{in} = +9.3 Vdc)				-	360	-	300	400	1 = 1	600	510
"ON" Resistance (CL/CP Device)	4,5,6	RON		13.4				(ob)	0.08	denatingo	Ohms
$(V_C = V_{DD}, R_L = 10 k\Omega)$	-									UN 0. E +	1 FIV
(V _{in} = +5.0 Vdc) —			5.0	-	610	-	300	660	-	840	(A)
$(V_{in} = -5.0 \text{ Vdc}) V_{SS} = -5 \text{ Vdc}$ $(V_{in} = \pm 0.25 \text{ Vdc})$				-	610 610		300 280	660 660	- 1	840	(8)
	- 0	12	7.5		370		240	400	= 28V	520	riches ²
$(V_{in} = +7.5 \text{ Vdc})$ $(V_{in} = -7.5 \text{ Vdc}) V_{SS} = -7.5 \text{ Vdc}$			7.5		370		240	400		520	
$(V_{in} = \pm 0.25 \text{ Vdc})$					370		180	400	Difficil 6	520	3,63
(Vin = +10 Vdc)	-		10	_	610	_	260	660		840	(50)
(Vin = +0.25 Vdc) VSS = 0 Vdc	-			_	610	_	260	660	_	840	(8)
(V _{in} = +5.6 Vdc)	-			-	610	-	310	660	_ 1	840	JRI.
(Vin = +15 Vdc)	-		15		370		260	400	_ (520	J(R)
(Vin = +0.25 Vdc) VSS = 0 Vdc				-	370	cheros	260	400	ene no	520	not en
(V _{in} = +9.3 Vdc)				-	370		300	400	-	520	
5"ON" Resistance Between any 2 circuits in a common package (VC = VDD) (Vin = ±5.0 Vdc) VSS = -5 Vdc	-	ΔRON	5.0	ISSA K	77 -	-	15	_		_	Ohms
(V _{in} = ±7.5 Vdc) V _{SS} = -7.5 Vdc		h1	7.5	-	1	-	10	-	_	-	-
Input/Output Leakage Current ($V_C = V$ ($V_{in} = +7.5$, $V_{out} = -7.5$ Vdc)	ss) –	ET 65	7.5	0 120	±0.100	_	±0.0015	±0.100	_	±1.0	μAde
(V _{in} = -7.5, V _{out} = +7.5 Vdc)		01	7.5		±0.100	_	±0.0015	±0.100	_	21.0	1

^{*}T_{low} = -55°C for AL Device, -40°C for CL/CP Device.

T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

Input Voltage specified as the voltage required at the Control In-

input-to-output stress of $V_{DD} - V_{SS}$ for V_{IL} and V_{IH} .

put for a 10 µA current through the transmission gate with an appropriate for the circuit application.

CWITCHING	CHARACTERISTICS*	(C 50 of T. = 250C)

Character Character	ristic		*wol	Figure	Symbol	VDD	Min	Тур	Max	Unit
Propagation Delay Time (VSS = 0	Vdc)	251941	20070	7	tPLH,	5.0	1 -	15	45	ns
Vin to Vout					TPHL	10	-	7.0	15	
(VC = VDD, RL = 10 kΩ)				- 1	32	15	-	6.0	12	
Control to Output				8	1	5.0	_	34	90	ns
$(V_{in} \le 10 \text{ Vdc}, R_L = 10 \text{ k}\Omega)$					8 141	10		20	45	
TVIN = 10 Vdc, 11[- 10 Kd2)					1 111	15		15	35	
		61	-	- 0		-			-	>/
crosstalk, Control to Output (Ve				9	1	5.0		30	-	mV
$(V_C = V_{DD}, R_{in} = 1.0 k\Omega, R)$	out = 10 ks2			- 1 -	di ne	10	-	50	(BolysO J	
f = 1kHz)	+0.0000.0+		103			15		100	WO 501 II	N. Daleston C. San
crosstalk between any two switc	hes (VSS = (Vdc)			1 100	5.0		-80	-	dB
$(R_L = 1.0 \text{ k}\Omega, f = 1.0 \text{ MHz},$					ni	2 -			91	
Vout1				-	+					
$crosstalk = 20 log_{10} \frac{Vout1}{V_{out2}}$				-						
	0.0	0	Vdal	-		5.0		5.0	-	MHz
Maximum Control Input Pulse F	equency (V	55 - 0	v dc/	- 1		10		10	- 0	MHz
$(R_L = 1.0 \text{ k}\Omega)$				- 1	18 m	15		12	ed JA) m	
	0100.0				1		_			
loise Voltage (VSS = 0 Vdc)				10,11	10 +	5.0	-	24	-	nV/√Cycle
(VC = VDD, f = 100 Hz)						10	-	25	-	
				- 1	0 g (G)	15	-	30	ILLICPICE	ersul During
(VC = VDD, f = 100 kHz)				-	92	5.0	-	12	_	
0.5			4.0	-		10	_	12	_	
					187	15		15	un(I-JA)	Nº Resistano
Sine Wave (Distortion) (VSS = -!	5 Vdc)		1			5.0		0.16	(0)L01 =	111.00%
(Vin = 1.77 Vdc RMS Center				1-11-	a a	0.0		0.10	fabi	(Vin = +5.0)
$R_L = 10 \text{ k}\Omega$, $f = 1.0 \text{ kHz}$	000	,		- 1				-5 Vdo	ggV (bbV	(Vin = -5.0
nsertion Loss (VC = VDD, Vin =	1 77 Vdc	V00 =	- 5 Vdc	12		5.0	_	+	(ap)	dB
RMS centered = 0.0 Vdc, f =		VSS -	-5 Vac,	12	7.8	5.0		1	(55)	(V ₁₀ = +7.5)
000 1000	1.0 IVITIZI					1		-7.5 Value		IV 7.5
$I_{loss} = 20 log_{10} \frac{V_{out}}{V_{in}}$					1					85.0x = aiVi
				Tell .					1	
$(R_L = 1.0 k\Omega)$				-			-	2.3		(Vin =+10)
$(R_L = 10 k\Omega)$				-			-	0.2		$(V_{10} = +0.25$
$(R_L = 100 k\Omega)$				-		19 18 19	-	0.1	_ (ab)	(Vin = +6.6)
$(R_L = 1.0 \mathrm{M}\Omega) - 0.08$				-	di l		_	0.05	- tob	(Vin - +16 V
Bandwidth (-3 dB)	005	1	390	12,13	BW	5.0		20 A 0 d	SSA (spA	MHz
(V _C = V _{DD} , V _{in} = 1.77 Vdc,	Vec = -5 V	de				0.0			(ab)	(E.e+ = n(V)
RMS centered @ 0.0 Vdc)	33 0 0					a laa		legive	0 90(10)	
(R _L = 1.0 kΩ)					NC.	0,0,		54		
						5 8 54		40	= 10+kn)	uR las V = a
$(R_{\perp} = 10 \text{ k}\Omega)$ $(R_{\perp} = 100 \text{ k}\Omega)$					98	100		38		(V)0 = +6.0 V
$(R_L = 1.0 \text{ M}\Omega)$				-		18 6 1		37	28/# (pp/	234
	280		0.19			F.0		37	HabV	(V _{in} = ±0.28
Feedthrough (VSS = -5 Vdc)					BX T	5.0	-		(de)	kHz /
$(V_C = V_{SS}, 20 \log_{10} \frac{V_{out}}{V_{in}} =$	-50 dB)			-				-7.5 Vdc		(Vin = ±0.26
$(R_L = 1.0 \text{ k}\Omega)$							_	1250	- (ab	0.00
(=)							-	140		V 01+ = n: V1
(5 100 141)						1 1 2		18		(V _{in} = +0.28
$(R_L = 100 \text{ k}\Omega)$ $(R_L = 1.0 \text{ M}\Omega)$				- 1			8 1		(56)	(A.B+ = niV)
				1	de l	2	-	2.0	-	The second second second

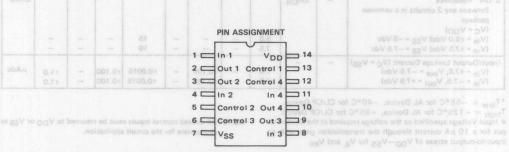
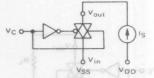
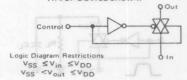


FIGURE 1 - INPUT VOLTAGE TEST CIRCUIT



 $V_{IL}=V_C$ when V_C has been raised from V_{SS} and when $I_S=10~\mu A$ $V_{IH}=V_C$ when V_C has been lowered from V_{DD} and when $I_S=10~\mu A$

LOGIC DIAGRAM



V _{control}	Vin to Vout Resistance
Vss	>10 ⁹ Ohms typ
VDD	3 × 10 ² Ohms typ

FIGURE 2 – QUIESCENT POWER DISSIPATION TEST CIRCUIT

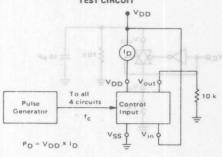
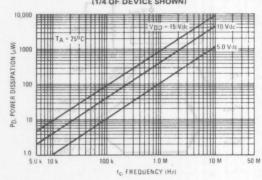
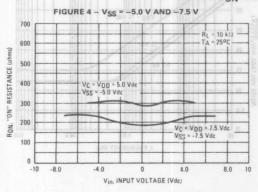


FIGURE 3 – TYPICAL POWER DISSIPATION PER CIRCUIT (1/4 OF DEVICE SHOWN)



TYPICAL RON versus INPUT VOLTAGE



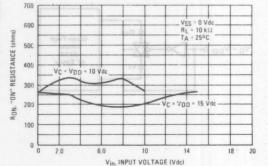


FIGURE 5 - VSS = 0 V

FIGURE 6 - RON CHARACTERISTICS TEST CIRCUIT

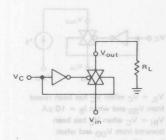
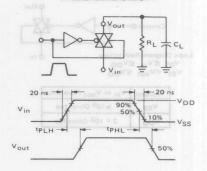


FIGURE 7 – PROPAGATION DELAY TEST CIRCUIT
AND WAVEFORMS



3

FIGURE 8 – TURN-ON DELAY TIME TEST CIRCUIT

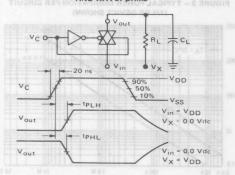


FIGURE 9 - CROSSTALK TEST CIRCUIT

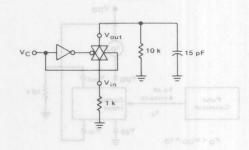


FIGURE 10 - NOISE VOLTAGE TEST CIRCUIT

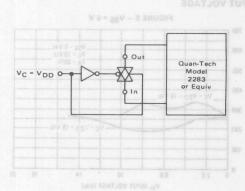
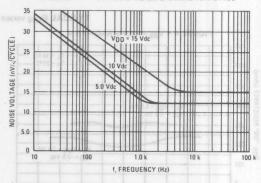
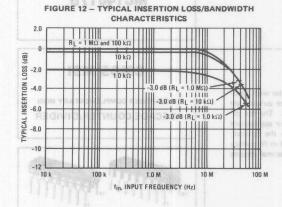
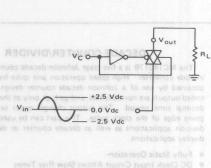


FIGURE 11 - TYPICAL NOISE CHARACTERISTICS





OF FOR FORE



MOTOROLA

CASE 620 CASE 648

ORDERING INFORMATION

ORDERING PROCESS

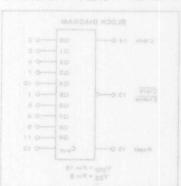
U Ceramic Fackage

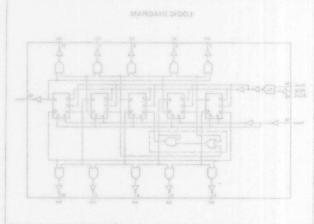
F Factor Fackage

Campbinature Range

Tampbinature Range

Reting		
Operating Temperature Range - AL Device CLICP Device		







MC14017B

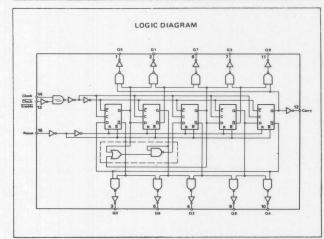
DECADE COUNTER/DIVIDER

The MC14017B is a five-stage Johnson decade counter with built-in code converter. High speed operation and spike-free outputs are obtained by use of a Johnson decade counter design. The ten decoded outputs are normally low, and go high only at their appropriate decimal time period. The output changes occur on the positive going edge of the clock pulse. This part can be used in frequency division applications as well as decade counter or decimal decode display applications.

- Fully Static Operation
- DC Clock Input Circuit Allows Slow Rise Times
- Carry Out Output for Cascading
- 12 MHz (typical) Operation @ VDD = 10 Vdc
- Divide-by-N Counting
- Quiescent Current = 5.0 nA/package Typical @ 5 Vdc
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range
- Pin-for-Pin Replacement for CD4017B

MAXIMUM RATINGS (Voltages referenced to VSS)

Rating	Symbol	Value	Unit
DC Supply Voltage	VDD	-0 5 to +18	Vdc
Input Voltage, All Inputs	Vin	-0 5 to VDD + 0 5	Vdc
DC Current Drain per Pin	1	10	mAdc
Operating Temperature Range - AL Device CL/CP Device	TA	-55 to +125 -40 to +85	ос
Storage Temperature Range	T _{stg}	-65 to +150	°C



CMOS MSI

DECADE COUNTER/DIVIDER



L SUFFIX
CERAMIC PACKAGE

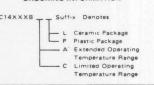
P SUFFIX PLASTIC PACKAGE

MULTAGLER

CASE 620

CASE 648

ORDERING INFORMATION

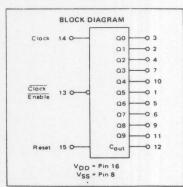


FUNCTIONAL TRUTH TABLE

(Positive Logic)

	(1.0311)	ve Logici	
CLOCK	CLOCK ENABLE	RESET	DECODE OUTPUT = n
0	×	0	n
X	-1	0	n
X	×	1	. 00
5	0	0	n+1
~	×	0	n
X	5	0	n
1	~	0	n+1

X = Don't Care If n < 5 Carry = "1", Otherwise = "0"



	qyT	nine	VDD	TI	ow*		25°C	nitalest	Thi	igh*	
Characterist		Symbol	Vdc	Min	Max	Min	Тур	Max	Min	Max	Unit
Output Voltage	"0" Level	VOL	5.0	-	0.05	-	0	0.05	-	0.05	Vdc
Vin VDD or 0	001		10	-	0.05	-	0	0.05	(bE)70 ^{[-4}	0.05	HJT ²
100	08	100	15	-	0.05	-	0	0.05	+ 10 (3d)	0.05	177
	"1" Level	VOH	5.0	4.95	-	4.95	5.0	an 91	4.95	W P. D	Vdc
Vin - 0 or VDD		- OH	10	9.95	INTL	9.95	10	_	9.95	emiT tle	Juggin C
200	100	-	15	14.95	-	14.95	15	25 n <u>s</u>	14.95	an ä_1) -	HTI
Input Voltage#	"0" Level	VIL	1					80 0.51 1	Totadn	0.07:01	Vdc
(Vo = 4.5 or 0.5 Vdc)	0.6		5.0		1.5	-	2.25	1.5	73 [Jols	1.5	1477
(VO = 9.0 or 1.0 Vdc)			10	_	3.0	-	4.50	3.0	2017	3.0	anguigo16
(V _O = 13.5 or 1.5 Vdd)		15		4.0	-	6.75	4.0	100toO (4.0	Reset
1000	"1" Level	VIH	- 0.			1	275	374+33	HdZsu 275	31497	(19)
$(V_0 = 0.5 \text{ or } 4.5 \text{ Vdc})$	230	.111	5.0	3.5	-	3.5	2.75	RT + 10 P	3.5	1914	Vdc
(VO = 1.0 or 9.0 Vdc)	175	-	10	7.0	-	7.0	5.50	CL ± 150	7.0	22197	191
(Vo = 1.5 or 13.5 Vdc	1	-	15	11.0	iù ret	11.0	8.25	_	11.0	yelsel no	entoon?
Output Drive Current (AL		71	10	11.0	784	11.0	0.25		11.0	nue 2 or	mAdc
	Source	ЮН	5.0	-3.0	2410	-2.4		CL £31	Holan S) = <u>uu</u> (q)	MAGC
(V _{OH} = 2.5 Vdc)	Source		5.0	-0.64		-0.51	-4.2	10,00	-1.7	1 - Janet	1397
(V _{OH} = 4.6 Vdc)	128		1000		-	2000	-0.88	OL 7 100	-0.36		1,191
(V _{OH} = 9.5 Vdc)	1001		10	-1.6	-	-1.3	-2.25	-	-0.9	TO THE PARTY	
(V _{OH} = 13.5 Vdc)			15	-4.2	[H]43	-3.4	-8.8	-	-2.4	ys B4J no	Bagagan*
$(V_{OL} = 0.4 \text{ Vdc})$	Sink	IOL	5.0	0.64	THE	0.51	0.88	-	0.36	000000101	mAdc
$(V_{OL} = 0.5 \text{ Vdc})$	800		10	1.6	-	1.3	2.25	LINE TO	0.9	TOPHS.	1,197
$(V_{OL} = 1.5 \text{ Vdc})$	230		15	4.2	-	3.4	8.8	11 +710 to	2.4	_ TE(d)	17.61
Output Drive Current (CL	/CP Device)	ГОН	1				251	101 7 10	rigitali U.U	1884	mAdc
(VOH = 2.5 Vdc)	Source		5.0	-2.5	HJQ	-2.1	-4.2	-	-1.7	Delay Tw	(Omnu)
(VOH = 4.6 Vdc)			5.0	-0.52	-	-0.44	-0.88	-	-0.36	Tue Ceut	. Fresot
(VOH = 9.5 Vdc)	009	-	10	-1.3	-	-1.1	-2.25	215 03	-0.9	(12 ns)	R.JAT
(VOH = 13.5 Vdc)	175	-	15	-3.6	-	-3.0	-8.8	142_ns	-2.4	n 88_01 =	U97
(V _{OL} = 0.4 Vdc)	Sink	IOL	5.0	0.52	-	0.44	0.88	80 000	0.36	(20 G:07	mAdc
(VOL = 0.5 Vdc)	125	-OL	10	1.3	HIME	1.1	2.25	_	0.9	dibliW as	
$(V_{OL} = 1.5 \text{ Vdc})$	00	1.00	15	3.6	-	3.0	8.8	_	2.4		
Input Current (AL Device	1 00	lin	15	-	± 0.1	-	±0.00001	± 0.1	-	± 1.0	μAdc
Input Current (CL/CP De			15	-	± 0.3	-	±0.00001	± 0.3		±1.0	μAdc
	/ice/	lin	15	-		-			-	₹1.0	-
Input Capacitance (V _{in} = 0)	18 nac	Cin	- 8		and .	-	5.0	7.5	-	ofitivities are	pF
Quiescent Current (AL De	vice)	IDD	5.0	-	5.0	-	0.005	5.0	-	150	μAdc
(Per Package)	- 86	081	10	-	10	-	0.010	10	-	300	
	ner.	OSE	15		20	-	0.015	20	- 1	600	
Quiescent Current (CL/CF	Device)	IDD	5.0	-	20	-	0.005	20	-	150	μAdc
(Per Package)	105	210	10	-	40	_	0.010	40	_	300	pride.
	001	015	15		80	-	0.015	80		600	
Total Supply Current**1		IT	5.0	31	00	1 10		- 00	the state of	000	μAdc
(Dynamic plus Quiesce	nt Limit	.1	10				.27 µA/kHz				имас
Per Package)	,		15				.55 μA/kHz				
(C ₁ = 50 pF on all out	outs all	000	15			IT = (0	.83 μA/kHz)f+ IDD			Steek E
		180									

*Tlow = -55°C for AL Device, -40°C for CL/CP Device.
Thigh = +125°C for AL Device, +85°C for CL/CP Device.

#Noise immunity specified for worst-case input combination.

Noise Margin for both "1" and "0" level = 1.0 Vdc min @ VDD = 5.0 Vdc

2.0 Vdc min @ V_{DD} = 10 Vdc

2.5 Vdc min @ V_{DD} = 15 Vdc

†To calculate total supply current at loads other than 50 pF: $l_T(C_L) = l_T(50 \text{ pF}) + 1.1 \times 10^{-3} (C_L - 50) \text{ VDDf}$ where: l_T is in μ A (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency. **The formulas given are for the typical characteristics only at 25°C.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it

is recommended that V_{in} and V_{out} be constrained to the range $V_{SS}\leqslant (V_{in}$ or $V_{out}) \leq V_{DD}$.

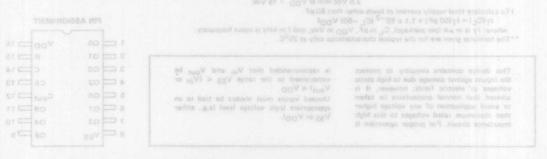
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD).

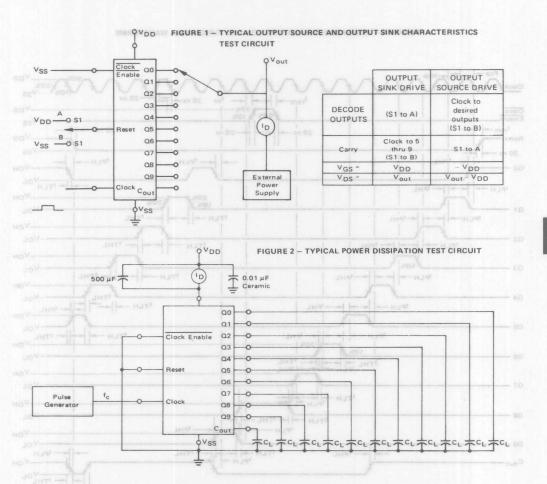
PIN ASSIGNMENT 1 05 V_{DD} 16 2 - 01 R 15 3 00 C 14 4 - 02 CE 13 Cout 12 5 06 09 11 6 = 07 7 = 03 04 10 8 = VSS 08 - 9

SWITCHING CHARACTERISTICS* (CL = 50 pF, TA = 25°C)

rinu neM nin	aracteristic			Symbol	VDD	SQV SSV	Min	Тур	Max	Unit
Output Rise Time	1 20.0	0		TLH		0.8		1009.7 301	401	ns
tTLH = (3.0 ns/pF) C	+ 30 ns			80.0	5.0	31		100		
tTLH = (1.5 ns/pF) C				30.0	10	21	_	50	100	
tTLH = (1.1 ns/pF) C				00.0	15	61	_	40	80	
ALVE TO THE REAL PROPERTY.	L 10 110	0.5	BD A			0.8	- WOW	leve 1 T		
Output Fall Time	9			THL a	2	01		100	200	ns
tTHL = (1.5 ns/pF) C				- 0	5.0	15	-	100	200	
tTHL = (0.75 ns/pF)					10		VIE	50	100	
tTHL = (0.55 ns/pF)	CL + 12.5 ns			27	15	6.0	_	40	80	
Propagation Delay Time	3.0	4.60	-	tPLH.		01	1		TobV D.T so	ns
Reset to Decade Outp	out 0.0			tPHL		31				
tPLH tPHL = (1.7 ns				1	5.0	-	- 1	500	1000	
tPLH tPHL = (0.66 n					40	-	FIN	230	460	
tpLH, tpHL = (0.5 ns					15	6.8	_	175	350	3.1 = 0.4)
		-	7.0	-		101		170	I may a from the	The second second
Propagation Delay Time				tPLH,		81			or 13.5 Vdc	ns
Clock to Cout		1 500 -		tPHL			, Hol	Device	Current IAL	utgut Drive
tPLH, tPHL = (1.7 ns			-2.4	- 0	5.0	ひき		400	800	IVOH = 2
tpLH, tpHL = (0.66 m				- 04	10	0.2	-	175	350	Nº NOV
tpLH, tpHL = (0.5 ns	/pF) CL + 10	00 ns		- 8	15	01	-	125	250	8 - HOW
Propagation Delay Time		98 8 TE	5.6-	TPLH,	Dan 1	15	1		1.5 Vdo) .	ns
Clock to Decode Out	put	88.0		tPHL		0.2		Sink	forth K	0 - (nV)
tpLH, tpHL = (1.7 ns				1	5.0	0.2	10,	500	1000	D JOY
tpLH tpHL = (0.66 m					10	25	_	230	460	
tpLH, tpHL = (0.5 ns			3.4		15	G1		175	350	L = 10A)
SECURITY OF A SE	/pi / C[. 10	-		1	13	- 1	NO.	teored 40	Chattananan	SWIND JURIS
Turn-Off Delay Time				tPLH		0.8		Snurce-	5 Voct	ns
Reset to Cout				52 -		6.0		1		RE KOVI
tpLH = (1.7 ns/pF) C				- 18	5.0	Ot	-	400	800	(Volt = 8
tpLH = (0.66 ns/pF)				- 18	10	15	-	175	350	I = HOV!
tpLH = (0.5 ns/pF) C	L + 100 ns				15	0.0		125	250	0 - 10377
Clock Pulse Width	0	2.25	1.7	tWH	5.0	20	250	125	5 VideF	ns
				-	10	21	100	50		(Vot = 1
					15	-	75	35	130 * 0	76.4
Clock Frequency		110000 04		1.01	5.0	91		5.0	2.0	MHz
Clock Frequency				fcl	10	91	rich.	12	5.0	manual Just
					15		Cin	16	6.7	ipage D rug
								1	0.7	400
Reset Pulse Width	6.0	-	-	HW	5.0	0.0	500	250	18 18 1 L	ns
				0.0	10	0.0	250	125	ed JA) Inpo	UD tospesio
				01	15	01	190	95	_ 190	IPer Pacin
Reset Removal Time	6.7	010.0		trem	5.0	51	750	375		ns
				02	10	0.0	275	135	Pent (CL/CP	uQ masesiu
		010.0		40	15	0.1	210	105		IPer Pack
Clock Input Rise and Fal	LTime	1 870.0			5.0	81	1	1		
Clock input Hise and Fai				tTLH, tTHL		5.0		No. 1 insti		vfotus2 tere
				1 - 13-1	10	01		No Limit		
				-	15			-		1100
Clock Enable Setup Time	00141	BB #A/KHz)	1.01 = 71	t _{su}	5.0	201	350	175	evo de no 3s	ns
					10		150	75		e asultud
				-	15		115	52	tgritcolle	e-assistand
Clock Enable Removal T	i			1	5.0	1929	420	260	O JA HID	ns
Clock Enable Removal 1	ime			trem		RVICE		THE PART STREET	SSOC for All	ns
					10	tenie	200 140	100 70	unity specific	Maise una

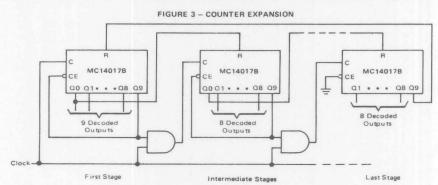
^{*}The formula given is for the typical characteristics only.

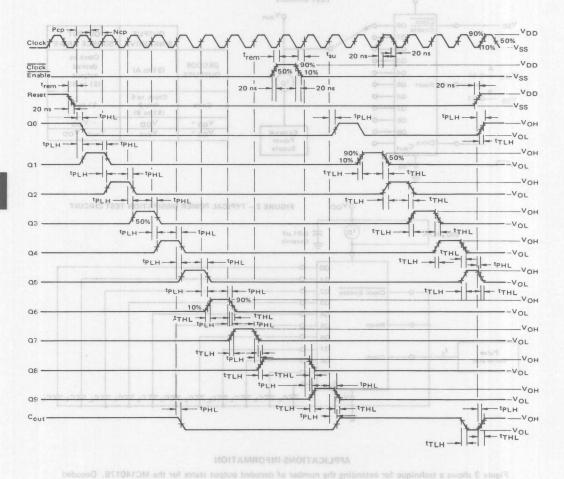


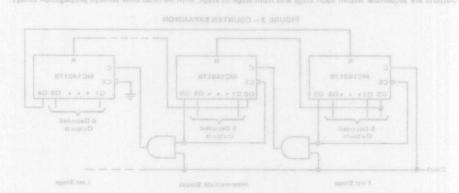


APPLICATIONS INFORMATION

Figure 3 shows a technique for extending the number of decoded output states for the MC14017B. Decoded outputs are sequential within each stage and from stage to stage, with no dead time (except propagation delay).









MC14018B

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

PRESETTABLE **DIVIDE-BY-N COUNTER**

PRESETTABLE DIVIDE-BY-N COUNTER

The MC14018B contains five Johnson counter stages which are asynchronously presettable and resettable. The counters are synchronous, and increment on the positive going edge of the clock.

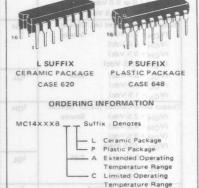
Presetting is accomplished by a logic 1 on the preset enable input. Data on the Jam inputs will then be transferred to their respective outputs (inverted). A logic 1 on the reset input will cause all Q outputs to go to a logic 1 state.

Division by any number from 2 to 10 can be accomplished by connecting appropriate $\overline{\mathbf{Q}}$ outputs to the data input, as shown in the Function Selection table. Anti-lock gating is included in the MC14018B to assure proper counting sequence.

Fully Static Operation

Storage Temperature Range

- Medium Speed 6.5 MHz typical @ 10 V
- Schmitt Trigger on Clock Input
- · Capable of Driving Two Low-Power TTL Loads, One Low-Power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range
- Pin-for-Pin Replacement for CD4018B



MAXIMUM RATINGS (Voltages referenced to VSS) Rating Symbol Value Unit VDD -0 5 to +18 Vdc DC Supply Voltage Vdc Input Voltage, All Inputs Vin -0.5 to V_{DD} + 0.5 DC Current Drain per Pin mAdc oc Operating Temperature Range -- AL Device TA -55 to +125 CL/CP Device -40 to +85 Tstg

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that Vin and Vout be constrained to the range VSS ≤ (Vin or Vout) ≤ VDD.

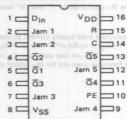
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD).

FUNCTIONAL TRUTH TABLE

Clock	Reset	Preset Enable	Jam Input	Qn							
~	0	0	×	Qn							
	0	0	×	Dn°							
×	0	1	0	1							
×	0	1-1,000	up ¹ vleo	0							
×	1 ,12	×	MX ma	nyCl.							

*Do is the Data input for that stage. Stage 1 has Data brought out to Pin 1.

PIN ASSIGNMENT



-65 to +150

°C







		VDD	T	ow*		25°C		Th	igh *	2 13
Characteristic	Symbol	Vdc	Min	Max	Min	Тур	Max	Min	Max	Unit
Output Voltage "0" Level	VOL	5.0	-	0.05	-	0.	0.05	-	0.05	Vdc
$V_{in} = V_{DD}$ or 0		10	-	0.05	-	0	0.05	-	0.05	
	. 1	15	-	0.05	-	0	0.05	-	0.05	
1" Level	VOH	5.0	4.95	-	4.95	5.0	-	4.95	-	Vdc
V _{in} = 0 or V _{DD}	0,,	10	9.95	- 1	9.95	10	-	9.95	-	
		15	14.95	BIHLL	14.95	15	0.7 (8)	14.95	199-	11.5
nput Voltage# "0" Level	VIL									Vdc
(Vo = 4.5 or 0.5 Vdc)		5.0	vyhijch e	1.5 191	n goun	2.25	1.5	0188 0	1.5	
(V _O = 9.0 or 1.0 Vdc)		10	es ana s	3.0	ole_The	4.50	3.0	W Brand	3.0	74X86
(V _O = 13.5 or 1.5 Vdc)		15	clouk	4.0	os galoj	6.75	4.0	mirani i	4.0	cinco
"1" Level	VIH	3	grif blds	DE FERRICI	ord ord	alpol s v	o berisila	T100006 21	DOLL 19291	1
(V _O = 0.5 or 4.5 Vdc)	1111	50	3.5	tients of I	3.5	2.75	Hiller and	3.5	grit-no	Vdc
(V _O = 1.0 or 9.0 Vdc)		10	-	iw t uani	7.0	and the same of th	inot A	7.0	() amagin	0 0
(VO = 1.5 or 13.5 Vdc)	Sten	15	11.0	-	11.0	8.25	sta + since	11.0	of Euch	150
Output Drive Current (AL Device)	Sta.		dished	mann or	065 01	0.20	if yeding	O VES V		mAdo
(V _{OH} = 2.5 Vdc) Source	ІОН	5.0		mooos so	-2.4	-4.2	un-Ö a	-1.7	d noisive	1
	191		0.01	input, at	-0.51	-0.88	100 00 10	-0.36	a gridosi	MED.
(V _{OH} = 4.6 Vdc)		10	-1.6	is melue	-1.3	-2.25	aldet ud	-0.9	Function	ent
(V _{OH} = 9.5 Vdc)			-4.2		-3.4	-8.8	ob Tegoti	-2.4	40188 to	MC
(V _{OH} = 13.5 Vdc)	1075	15		-		-	1701		STREET, STREET	19
(VOL = 0.4 Vdc) Sink	IOL	5.0	0.64	-	0.51	0.88	S MHz	0.36	lection S	mAdd
(V _{OL} = 0.5 Vdc)		10	1.6	-	1.3	2.25		0.9		
(V _{OL} = 1.5 Vdc)		15	4.2	-	3.4	8.8	Cloude In	2.4	T zumdo	
Output Drive Current (CL/CP Device)	ІОН			2010	BOOD IN	1511103 777	ADT OW I	buskind	to striede	mAdd
(V _{OH} = 2.5 Vdc) Source		5.0	-2.5	L Loads	-2.1	-4.2	TT watte		1,049-P0	
(VOH = 4.6 Vdc)	MC14	5.0	-0.52		-0.44	-0.88	Tempera	-0.36	Over th	
(V _{OH} = 9.5 Vdc)		10	-1.3	-	-1.1	-2.25	rol +nem	-0.9	m-for-Pin	3 0
(V _{OH} = 13.5 Vdc)		15	-3.6	-	-3.0	-8.8	-	-2.4	-	
(VOI = 0.4 Vdc) Sink	IOL	5.0	0.52	-	0.44	0.88	_	0.36	-	mAdo
(VOI = 0.5 Vdc)	02	10	1.3	- 1	1.1	2.25	-	0.9	-	
(VOL = 1.5 Vdc)		15	3.6	-	3.0	8.8	- 1	2.4	-	
nput Current (AL Device)	lin	15	-	± 0.1		± 0.00001	± 0.1	_	±1.0	μAdc
nput Current (CL/CP Device)		15	-	± 0.3	_	±0.00001	± 0.3 1		±1.0	μAdc
	lin	15		10.3			-	-	11.0	-
nput Capacitance (Vin ·· 0)	Cin			-		5.0	7.5			pF
Quièscent Current (AL Device)	IDD	5.0	-	5.0	-	0.005	5.0	-	150	μAdo
(Per Package)	3	10		10		0.010	10	-	300	
	-	15	1	20	-	0.015	20	-	600	1
uiescent Current (CL/CP Device)	IDD	5.0	-	20	_ (8	0.005	20	JOAN SE	150	μAdo
(Per Package)	00	10	_ 8	40	Joseph	0.010	40	gpituß	300	200
1 0 1 0 X		15	-811	80	no.V	0.015	80	_	600	Utmesii
otal Supply Current**†	IT	5.0	80.		1- = 10).3 µA/kHz)				1000000
(Dynamic plus Quiescent,	1	10	8.0 + 0).7 µA/kHz)				μAdo
Par Packago)	-									anpityu!
(CL = 50 pF on all outputs, all buffers switching)	0,	15			T = (1	I.O µA/kHz)	1 + 'DD			I enits

 $^*T_{low}$ = -55°C for AL Device, -40°C for CL/CP Device. T_{high} = +125°C for AL Device, +85°C for CL/CP Device. #Noise immunity specified for worst-case input combination.

*Tlow = -55°C for AL Device, +85°C for No.

Thigh = +125°C for AL Device, +85°C for No.

Thigh = +125°C for AL Device, +85°C for No.

#Noise immunity specified for worst-case input combination.

*Noise Margin for both "1" and "0" level = 1.0 Vdc min @ VDD = 5.0 Vdc

2.0 Vdc min @ VDD = 10 Vdc

2.5 Vdc min @ VDD = 15 Vdc

*To calculate total supply current at loads other than 50 pF:

IT(CL) = IT(50 pF) + 1 x 10-3 (CL -50) VDDf

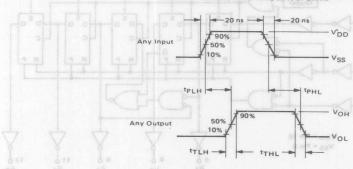
where: IT is in µA (per package), CL in pF, VDD in Vdc, and f in kHz is input frequency.

**The formulas given are for the typical characteristics only at 25°C.

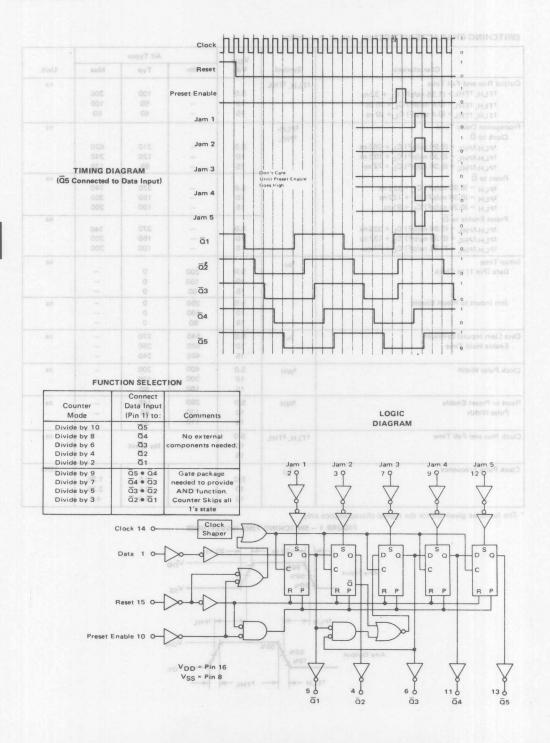
	nnnnnn	VDD		All Types			
Characteristic	Symbol	Vdc	Min	Тур	Max	Unit	
Output Rise and Fall Time	tTLH, tTHL	5.0 10 15	siden Sessor 9	100 50 40	200 100 80	ns	
Propagation Delay Time Clock to ① tp_H,tpHL = (0.90 ns/pF) C_L + 265 ns tp_H,tpHL = (0.36 ns/pF) C_L + 102 ns tp_H,tpHL = (0.26 ns/pF) C_L + 72 ns	tpLH, tpHL	5.0 10 15	E mus.	310 120 85	620 240 170	ns	
Reset to \overline{Q} $tp_{LH} = (0.90 \text{ ns/pF}) C_L + 325 \text{ ns}$ $tp_{LH} = (0.36 \text{ ns/pF}) C_L + 132 \text{ ns}$ $tp_{LH} = (0.26 \text{ ns/pF}) C_L + 81 \text{ ns}$	Midge S Times F Lives	5.0 10 15	& mai_	370 150 100	740 300 200	ns (de f	
Preset Enable to Q tp_H,tpHL = (0.90 ns/pF) C _L + 325 ns tp_H,tpHL = (0.36 ns/pF) C _L + 132 ns tp_H,tpHL = (0.26 ns/pF) C _L + 81 ns		5.0 10 15	10 -	370 150 100	740 300 200	ns	
Setup Time Data (Pin 1) to Clock	t _{su}	5.0 10 15	200 100 80	0 0 0	=	ns	
Jam Inputs to Preset Enable		5.0 10 15	200 100 80	0 0 0	-	ns	
Data (Jam Inputs)-to-Preset Enable Hold Time	t _h	5.0 10 15	540 500 480	270 250 240	-	ns	
Clock Pulse Width	tWH	5.0 10 15	400 200 160	200 100 80	FUNCT	ns	
Reset or Preset Enable Pulse Width	tWH .	5.0 10 15	290 130 110	145 65 55	Tight Tight		
Clock Rise and Fall Time	[†] TLH, [†] THL	5.0 10 15	No external need components need to be seen to to be see	No Limit		blyic ns	
Clock Pulse Frequency	o f _C I	5.0 10 15	Gare parkapi needed to prov ANO-function Country Skips	2.5 6.5 8.0	1.25 3.25 4.0	MHz blviG blviG blviG	

* The formulae given are for the typical characteristics only.

FIGURE 1 - SWITCHING TIME WAVEFORMS



3





MC14020B

14-BIT BINARY COUNTER

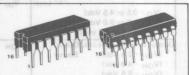
The MC14020B 14-stage binary counter is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. This part is designed with an input wave shaping circuit and 14 stages of ripple-carry binary counter. The device advances the count on the negative-going edge of the clock pulse. Applications include time delay circuits, counter controls, and frequency-dividing circuits.

- Fully Static Operation
- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- Noise Immunity = 45% of VDD typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range
- Low Input Capacitance = 5.0pF typical
- Buffered Outputs Available from stages 1 and 4 thru 14
- Common Reset Line
- 13 MHz Typical Counting Rate @ VDD = 15V
- Pin-for-Pin Replacement for CD4020B

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

14-BIT BINARY COUNTER



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX PLASTIC PACKAGE CASE 648

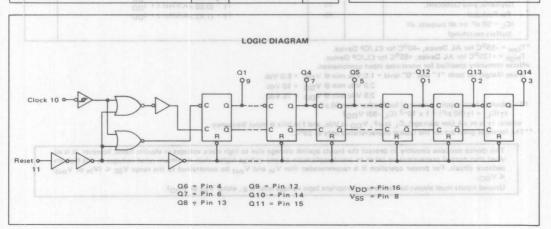
ORDERING INFORMATION



MAXIMUM RATINGS (Voltages referenced to Vsc)

Rating			Symbol	Value	Unit
DC Supply Voltage	0.0	600	VDD	-0.5 to +18	Vdc
Input Voltage, All Inputs	20	310	Vin	-0.5 to V _{DD} + 0.5	Vdc
DC Current Drain per Pin	ac l	200	1	10	mAdc
Operating Temperature Range - CL/	AL Device CP Device	010	TA	-55 to +125 -40 to +85	°C
Storage Temperature Range	out tills	BILA	Tstg	-65 to +150	°C

TRUTH TABLE CLOCK RESET OUTPUT STATE O No Change O Advance to next state X 1 All Outputs are low





		VDD	Tic	w*		25°C		Th	igh *	
Characteristic	Symbol	Vdc	Min	Max	Min	Тур	Max	Min	Max	Unit
Output Voltage "0" Level	VOL	5.0	-	0.05		0	0.05	-	0.05	Vdc
Vin VDD or 0	02	10	-	0.05	-	0	0.05	-	0.05	
		15	-	0.05	_	0	0.05	-	0.05	
Level	VOH	5.0	4.95	_	4.95	5.0	AMAG T	4.95	_	Vdc
Vin Oor VDD	.04	10	9.95		9.95	10		9.95	DECMO	
W-POWER COMPLEMENTARY MOST	Sup len la	15	14.95	r betoun	14.95	15	nid egst	14.95	DET ONE B	1
nput Voltage" "0" Level	VIL		mont alg	110 D 111 EE	DIVISIO DIS	torn discourse	OTTOMICO I	THE PARTY OF	DITO TON	Vdc
(Va = 45 or 05 Vdc)	-IL	5.0	enigarla t	1.5	ni ng rin	2.25	1.5	e, Triis	1.5	11121107
(VO = 9.0 or 1.0 Vdc)		10	DIVED S	3.0	DOD_YTE	4.50	3.0	1189982	3.0	circuit
(V _O = 13.5 or 1.5 Vdc)	السسا	15	selve do	4.0	o egips i	6.75	4.0	no Inuo	4.0	navbs
"1" Level	VIH	10	911 Dine	HOMEOS	197/10/03	, BI OB BS	(6180 60	ID SOUIS	ations in	HUUPA
(V _O = 0.5 or 4.5 Vdc)	*IH	5.0	3.5		3.5	2.75		3.5	nib <u>i</u> vib-y	Vdc
(V _O = 1.0 or 9.0 Vdc)		10	7.0		7.0	5.50	_	7.0		1
(VO = 1.5 or 13.5 Vdc)	in I	15	11.0		11.0	8.25		11.0		
	200	15	11.0		11.0	0.23		11.0	core 2 cel	mAdc
Output Drive Current (AL Device)	ІОН	5.0	20		2.4	4.0	19	1.7	Control As	
(VOH = 2.5 Vdc) Source	o lar	5.0	-3.0	56V (-2.4	-4.2	q\An 0.	-1.7 -0.36	O Inspent C	10 0
(V _{OH} = 4.6 Vdc)		5.0	-0.64	-	-0.51	-0.88	V 10 8		ummit az	DV1 8
(V _{OH} = 9.5 Vdc)		10	-1.6	-	-1.3	-2.25		-0.9		0 0
140H - 13.5 AGC	AHHO I	15	-4.2	-	-3.4	-8.8	vont IIA	-2.4	sto Fl'ab	-
(VOL = 0.4 Vdc) Sink	IOL	5.0	0.64	-	0.51	0.88	0.5 = 8	0.36	How yiq	mAdc
(V _{OL} = 0.5 Vdc)		10	1.6	w 1 com	1.3	2.25	The Paris	0.9	to side	45 p
(V _{OL} = 1.5 Vdc)		15	4.2	One_Lor	3.4	8.8	wo_l ov	2.4	10,3000	
Output Drive Current (CL/CP Device)	ГОН		1	DOTE WITH	1040 2172	2271110	NESCHOLDS	0.00	death of the same	mAdc
(V _{OH} = 2.5 Vdc) Source	MOTAS	5.0	-2.5	-	-2.1	-4.2	C- 9	-1.7	STOCIDS I	
(V _{OH} = 4.6 Vdc)	CALDER	5.0	-0.52	-	-0.44	-0.88	cs + 5,0	-0.36	Dueni v	0.1 0.
(V _{OH} = 9.5 Vdc)		10	-1.3	a with t	-1.1	-2.25	aldelle	-0.9	O Ferei	B W
(V _{OH} = 13.5 Vdc)		15	-3.6	A District of	-3.0	-8.8	2100110	-2.4	20 02101	1
(VOL = 0.4 Vdc) Sink	101	5.0	0.52	-	0.44	0.88	-	0.36	M. GODAN	mAdc
(VOL = 0.5 Vdc)	OL.	10	1.3	-	V31.1=	2.25	office Ri	0.9	WT -HM	E 13
(V _{OL} = 1.5 Vdc)		15	3.6	_	3.0	8.8	_	2.4	t and the	
nput Current (AL Device)	lin	15	-	± 0.1		± 0.00001	± 0.1	medical	±1.0	μAdc
nput Current (CL/CP Device)		15	-	± 0.3		±0.00001	± 0.3		11.0	μAdc
	lin		_		-			-		
nput Capacitance (V _{in} = 0)	Cin	- Lintt	-	suleV	Lincon	5.0	7.5	alow) SE	RATIN	pF
Quiescent Current (AL Device)	IDD	5.0	- 01	5.0	-	0.005	5.0	-	150	μAdc
(Per Package)		10	- 01	10	90	0.010	10		300	Andries
egnand on 0	-	15	190 +	20	miV	0.015	20	- "	600	Pariety I
Quiescent Current (CL/CP Device)	IDD	5.0	1	20		0.005	20		150	μAde
(Per Package)		10	25 _	40	-AT	0.010	40	- sonsH	300	Tonite
Land and the second		15	25	80	-	0.015	80	UQ_	600	
Total Supply Current**†	1 _T	5.0	1 08	- 65 10 -	110	.42 µA/kHz		60/10	N manual	μAdc
(Dynamic plus Quiescent,	- 1	10	1							ДАОС
Per Package)		15				.85 μA/kHz .43 μA/kHz				
(CL = 50 pF on all outputs, all buffers switching)		15			17 - (1	.43 µм/кнг	סטי די וו			

^{*}T_{IOW} = -55°C for AL Device, -40°C for CL/CP Device. Thigh = +125°C for AL Device, +85°C for CL/CP Device. #Noise immunity specified for worst-case input combination.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in} \text{ or } V_{out})$ < VDD.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD).

Noise Margin for both "1" and "0" level = 1.0 Vdc min @ VDD = 5.0 Vdc 2.0 Vdc min @ V_{DD} = 10 Vdc 2.5 Vdc min @ V_{DD} = 15 Vdc

[†]To calculate total supply current at loads other than 50 pF:

I_T(C_L) = I_T(50 pF) + 1 x 10⁻³ (C_L -50) V_{DD}

where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.

*The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS* (CL = 50 pF, TA = 25°C) T - 8 384313

Characteristic	Symbol	V _{DD} Vdc	Min	Тур	Max	Unit
Output Rise Time	tTLH	UU		T U U	UUT	ns
TLH = (3.0 ns/pF) CL + 30 ns		5.0	-	100	200	Separate .
tTLH = (1.5 ns/pF) CL + 15 ns		10		50	100	
tTLH = (1.1 ns/pF) CL + 10 ns		15		40	.80	9
Output Fall Time	THL					ns
THL = (1.5 ns/pF) C _L + 25 ns	ment ment	5.0	-	100	200	4
THL = (0.75 ns/pF) C _L + 12.5 ns		10		50	100	c c
THL = (0.55 ns/pF) C _L + 9.5 ns	r r	15	- 1	40	80	
Propagation Delay Time	tPLH,			1		ns
Clock to Q1	tPHL			-	1	0
tpHL, tpLH = (1.7 ns/pF) CL + 315 ns		5.0	_	400	750	
tpHL tpLH = (0.66 ns/pF) C ₁ + 137 ns		10	-	170	300	
tPHL, tPLH = (0.5 ns/pF) CL + 95 ns		15	_	120	230	d
Clock to Q14				-	-	μѕ
tpHL tpLH = (1.7 ns/pF) CL + 2715 ns		5.0		2.8	5.6	μ
tpHL, tpLH = (0.66 ns/pF) CL + 967 ns		10		1.0		10
		15	<u>.</u>	100000	1.5	
tpHL, tpLH = (0.5 ns/pF) CL + 575 ns		15		0.6	1.5	10
Propagation Delay Time	tPHL					ns
Reset to Q _n						
tpHL = (1.7 ns/pF) CL + 510 ns		5.0		595		10
tpHL = (0.66 ns/pF) CL + 197 ns		10	-	230	900	
tpHL = (0.5 ns/pF) CL + 155 ns		15	-	180	680	
Clock Pulse Width	tWH	5.0	500	140	-	ns
		10	165	55	-	
		15	125	38	-	
Clock Pulse Frequency	f _{cl}	5.0	-	3.5	1.0	MHz
		10	_	9.0	3.0	
21 (2)		15	-	13	4.0	
Clock Rise and Fall Time	TLH, THL	5.0				_
Market State of the Control of the C	010	A1010 E		No Limit		
		15				
Reset Pulse Width	tWL	5.0	3000	320	_	ns
Tieset Fulse Width	90	10	550	120		113
ne ne		15	420	80		

^{*} The formulae given are for the typical characteristics only.

FIGURE 1 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

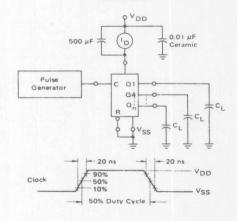


FIGURE 2 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

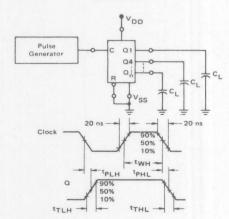
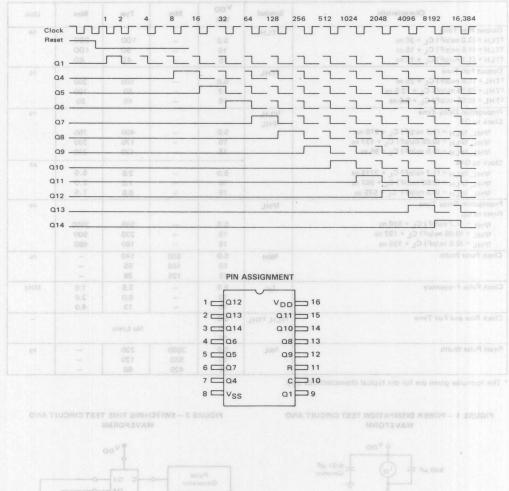
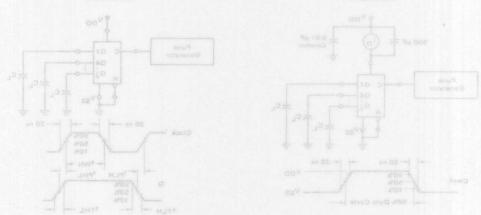


FIGURE 3 - TIMING DIAGRAMUS - JOI *20172183TOARAND DIMINOTIWS









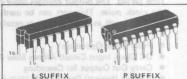
MC14021B

FOR COMPLETE DATA

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

8-BIT STATIC SHIFT REGISTER



L SUFFIX CERAMIC PACKAGE CASE 620 P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB Suffix Denotes

L Ceramic Package
P Plastic Package
A Extended Operating
Temperature Range
C Limited Operating

SERIA	AL OPER			TABLE		
t	CLOCK	Ds	P/S	Q6 t = n+6	Q7 t = n+7	Q8 t = n+8
n	5	0	0	0	7	?
n+1		10	0	1	0	?
n+2	5	0	0	0	1	0
n+3	5	1	0	1	0	1
	7	X	0	06	Q7	08

PARALLEL OPERATION:

CLC	OCK	De	0/0	D	*0	
MC14014B	014B MC14021B		P/S	DM	UM	
	X	X	1	0	0	
	×	X	1	1	1	

*Q6, Q7, & Q8 are available externally X = Don't Care

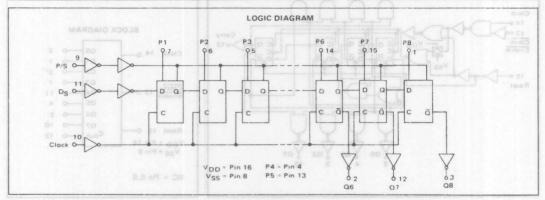
8-BIT STATIC SHIFT REGISTER

The MC14014B and MC14021B 8-bit static shift registers are constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These shift registers find primary use in parallel-to-serial data conversion, synchronous and asynchronous parallel input, serial output data queueing; and other general purpose register applications requiring low power and/or high noise immunity.

- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- Synchronous Parallel Input/Serial Output (MC14014B)
- Asynchronous Parallel Input/Serial Output (MC14021B)
- Synchronous Serial Input/Serial Output
- Full Static Operation from DC to typical 6.0 MHz at 10 V VDD
- "Q" Outputs from Sixth, Seventh, and Eighth Stages
- Double Diode Input Protection
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load to Two HTL Loads Over the Rated Temperature Range.
- MC14014B Pin-for-Pin Replacement for CD4014B
- MC14021B Pin-for-Pin Replacement for CD4021B

MAXIMUM RATINGS (Voltages referenced to Vss)

Rating	Symbol	Value	Unit
DC Supply Voltage	VDD	-0.5 to +18	Vdc
Input Voltage, All inputs	Vin	-0.5 to V _{DD} + 0.5	Vdc
DC Current Drain per Pin	1	10	mAdc
Operating Temperature Range - AL Device CL/CP Device	TA	-55 to +125 -40 to +85	°C
Storage Temperature Range	T _{stg}	-65 to +150	ос



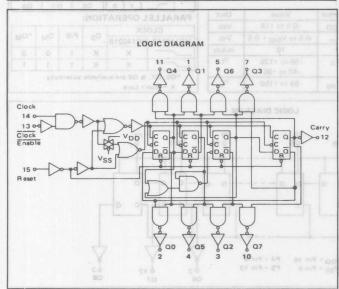


The MC14022B is a four-stage Johnson octal counter with built-in code converter. High-speed operation and spike-free outputs are obtained by use of a Johnson octal counter design. The eight decoded outputs are normally low, and go high only at their appropriate octal time period. The output changes occur on the positive-going edge of the clock pulse. This part can be used in frequency division applications as well as octal counter or octal decode display applications.

- Fully Static Operation
- DC Clock Input Circuit Allows Slow Rise Times
- Carry Out Output for Cascading
- 12 MHz (typical) Operation @ VDD = 10 Vdc
- Divide-by-N Counting
- Quiescent Current = 5.0 nA/package Typical @ 5 Vdc
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range
- Pin-for-Pin Replacement for CD4022B

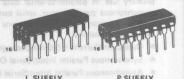
MAXIMUM RATINGS (Voltages referenced to VSS)

Rating	Symbol	Value	Unit
DC Supply Voltage	VDD	-0.5 to +18	Vdc
Input Voltage, All Inputs	Vin	-0.5 to V _{DD} + 0.5	Vdc
DC Current Drain per Pin	2 1	10	mAdc
Operating Temperature Range AL Device CL/CP Device	TA	-55 to +125 -40 to +85	°C
Storage Temperature Range	T _{stg}	-65 to +150	°C



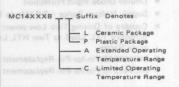
CMOS MSI

(LOW-POWER COMPLEMENTARY MOS) OCTAL COUNTER/DIVIDER



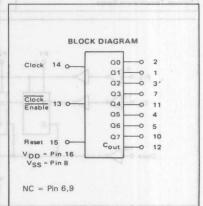
CERAMIC PACKAGE PLASTIC PACKAGE CASE 620 CASE 648

ORDERING INFORMATION



FUNCTIONAL TRUTH TABLE (Positive Logic)

CLOCK	CLOCK	RESET	OUTPUT - n
0	×	0	n
×	1 '88	0	n
5	0	0	W v n+1 30
~	×	0	n
1	~	0	n+1
×		0	n 30
×	X	Rentzen	00



ELECTRICAL CHARACTERISTICS

Alle Typ Max Unit	300	VDD	Tic	w*		25°C	net market	Thi	gh°	
Characteristic	Symbol	Vdc	Min	Max	Min	Тур	Max	Min	Max	Unit
Output Voltage "0" Level	VOL	5.0	-	0.05	-	0	0.05	-	0.05	Vdd
Vin VDD or 0	U.G	10	-	0.05	-	0	0.05	o/psf) CL	0.05	T
08 08	01	15	-	0.05	-	0	0.05	15 (Jd/s	0.05	TT.
08 04 "1" Level	VOH	5.0	4.95	_	4.95	5.0	611 107	4.95	THE	Vdd
Vin O or VDD		10	9.95	-	9.95	10	-	9.95	miT_lis (andang.
00% 00% -	9.0	15	14.95	-	14.95	15	1.25 <u>-</u> 01	14.95	1937= 7	HTI .
Input Voltage# "0" Level	VIL						PE 0.51 T	in today	and the same	Vdc
(V _O = 4.5 or 0.5 Vdc)	61	5.0	_	1.5	-	2.25	1.5	ns/pF) C	1.5	112
(V _O = 9.0 or 1.0 Vdc)		10	-	3.0	-	4.50	3.0	smil A	3.0	Propuga
(V _O = 13.5 or 1.5 Vdc)		15	-	4.0	-	6.75	4.0	de Output	4.0	maPi
"1" Level	VIH					80 61	Fr. 154	1675u 7111	1. 16 Hd. 'H	1.01
(V _O = 0.5 or 4.5 Vdc)	01	5.0	3.5	-	3.5	2.75	+ 10 (4)	3.5	, 11F181 'F	Vdc
(V _O = 1.0 or 9.0 Vdc)	15	10	7.0	-	7.0	5.50	1+101	7.0	1, 19291	197
(V _O = 1.5 or 13.5 Vdc)		15	11.0	-	11.0	8.25	-	11.0	sinG_noin	Property
Output Drive Current (AL Device)	ІОН	JHP							902 01 X	mAde
(VOH = 2.5 Vdc) Source	0.0	5.0	-3.0	-	-2.4	-4.2	E+_10 (-1.7	HELPT , H	19
(V _{OH} = 4.6 Vdc)	01	5.0	-0.64	-	-0.51	-0.88	+ 10/13	-0.36	1, 1241, "	197
(V _{OH} = 9.5 Vdc)	81	10	-1.6	-	-1.3	-2.25	1+10(-0.9	" JIMBI 'H	1497
(V _{OH} = 13.5 Vdc)		15	-4.2	-	-3.4	-8.8	-	-2.4	nion_Data	MagarS.
(VOL = 0.4 Vdc) Sink	IOL	5.0	0.64	_	0.51	0.88	-	0.36	Sett of the	mAd
(Vol = 0.5 Vdc)	Aca 13	10	1.6	-	1.3	2.25	9.4.70 ts	0.9	JEEP! , P	47
(V _{OL} = 1.5 Vdc)	10	15	4.2	-	3.4	8.8	+ 10 (st	2.4	H. PEHL.	qI
Output Drive Current (CL/CP Device)	ЮН					50.5	12 14 15 1	Total B.D.	METE I	mAd
(VOH = 2.5 Vdc) Source	011	5.0	-2.5	-	-2.1	-4.2	-	-1.7	Valid II	9-mul
(Vou = 4.6 Vdc)		5.0	-0.52	_	-0.44	-0.88	d = 1	-0.36	000 at 11	NUR .
(Val) = 9.5 Vdc)	-5.0	10	-1.3	-	-1.1	-2.25	an drs 4	-0.9	(23) = H	qf
(Val) = 13.5 Vdc)	10	15	-3.6	-	-3.0	-8.8	+ 142 mi	-2.4	88.0) = H	93
(Va. = 0.4 Vds) Sink	IOL	5.0	0.52		0.44	0.88	20 001	0.36	- C.O.	mAde
(Vol = 0.5 Vdc)	000	10	1.3	_	1.1	2.25	_	0.9	biW salu	Clock
(V _{OL} = 1.5 Vdc)	01	15	3.6	_	3.0	8.8	_	2.4	_	
Input Current (AL Device)	lin	15		± 0.1		±0.00001	±0.1	_	± 1.0	μAdd
nput Current (CL/CP Device)	lin	15	-	± 0.3	-	±0.00001	± 0.3	-	±1.0	μAdo
		_	-	_	-	5.0		-	- 1.0	pF
011	Cin			-		5.0	7.5	_	_	PF
187 1 000 1 000	0.8	E 0			-	0.000			ability auto	Sasat P
Quiescent Current (AL Device)	IDD	5.0	-	5.0	-	0.005	5.0	-	150	μAdd
(Per Package)	81	15		20		0.010	10	-	300	
780 378 - 08	9.8	Contract of			-	0.015	20	sini	600	Thought in
Quiescent Current (CL/CP Device)	IDD	5.0	-	20	-	0.005	20	-	150	μAdd
(Per Package)	23	10	-	40	-	0.010	40	-	300	
	5.6	15	veri -	80	-	0.015	80	He-Thos	600	Disclo
Total Supply Current**†	dr	5.0			IT = (0	.28 μA/kHz) f + IDD			μAdd
(Dynamic plus Quiescent,	87	10				.56 μA/kHz				
Per Package)	9.8	15			IT = (0	.85 μA/kHz)f+ IDD	noriT out	enable Se	Clock
(C _L = 50 pF on all outputs, all	10	62								1
buffers switching)	10									

*Tlow = -55°C for AL Device, -40°C for CL/CP Device.

Thigh = +125°C for AL Device, +85°C for CL/CP Device.

#Noise immunity specified for worst-case input combination.

Noise Margin for both "1" and "0" level = 1.0 Vdc min @ VDD = 5.0 Vdc

2.0 Vdc min @ VDD = 10 Vdc

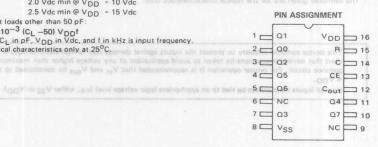
2.5 Vdc min @ VDD = 15 Vdc

PIN ASSIGNMENT

†To calculate total supply current at loads other than 50 pF:

If (CL) = $I_T(50 \text{ pF}) + 1.25 \times 10^{-3}$ (CL -50) VDDf where: I_T is in I_M (per package), CL in pF, VDD in Vdc, and f in kHz is input frequency.

*The formulas given are for the typical characteristics only at 25°C. ixem nests restalt egation you to noise Roge blove as nester ed and 3 @ 020 con sets bac 14



NC = No Connection

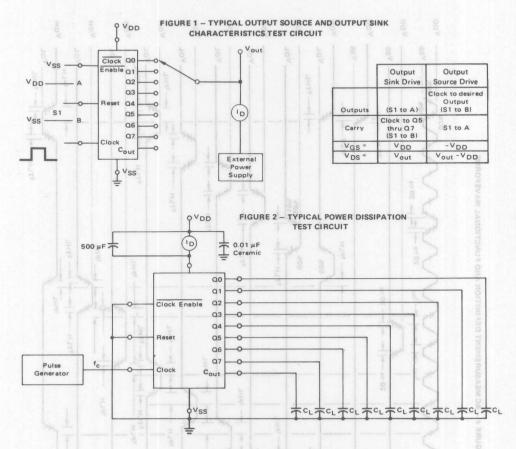
SWITCHING CHARACTERISTICS* (CL = 50 pF, TA = 25°C)

Output Rise Time t _{TLH} = (3.0 ns/pF) C _L + 30 ns t _{TLH} = (1.5 ns/pF) C _L + 15 ns		the second second								
tTLH = (3.0 ns/pF) CL + 30 ns			- 80.0		tTLH	100	The same of the	NI-	The same of the sa	ns
					07	5.0	lora.i	100	200	1100011
						10	-	50	100	miV
tTLH = (1.1 ns/pF) CL + 10 ns						15	-	40	80	
All the second s	50	4.05		30.6	0.8	HoV	Invest 1	10		ns
Output Fall Time				38.6		F 0		100	200	113
tTHL = (1.5 ns/pF) CL + 25 ns				62.8		5.0	-			
tTHL = (0.75 ns/pF) CL + 12.5						10	level "0"	50	100	ov tu
tTHL = (0.55 ns/pF) CL + 12.5	ns				5.0	15	-	40	80	-ava
Propagation Delay Time	4.50		3.0		tPLH,	1 - 1		Vde).	0.1 10 0.8	ns
Reset to Decode Output					tPHL			laby i	13.8 or 1	FoV)
tpLH, tpHL = (1.7 ns/pF) CL +						5.0	Jova J "T"	500	1000	
tpLH, tpHL = (0.66 ns/pF) CL	+ 197 ns			3.5		10	-	230	460	- ovi
tpLH, tpHL = (0.5 ns/pF) CL +	150 ns			4.5		15	-	175	350	- ovi
Propagation Delay Time	8.28	0.11	-	1.8	and the second second			(abV i	E1 10 8 1	ns
Clock to Cout				-	tPHL	1	-			-
tplH tpHL = (1.7 ns/pF) CL +	315 ns			ole.		5.0	1931	400	800	CI sugi
tpLH, tpHL = (0.66 ns/pF) CL	+ 142 ns					10	8216	175	350	HOV
tpLH, tpHL = (0.5 ns/pF) CL +				0.84		15	_	125	250	HOV
	ATTACABLE PARTY OF THE PARTY OF	8.1		911-	- 01		-	-	DELA R. H.	Now!
Propagation Delay Time				2 1	tPLH,			- 6	SV8.II	ns
Clock to Decode Output	88.0			48.0	tPHL		1 3	075	1000	VOL
tPLH, tPHL = (1.7 ns/pF) CL +				8,0		5.0	-	275	1 N. Phys. 527 (1987)	TOVI
tPLH, tPHL = (0.66 ns/pF) CL	+ 197 ns			1.0		10	-	125	460	(VOL
tpLH, tpHL = 0.5 ns/pF) CL +	150 ns					15	Tonal and	95	350	
Turn-Off Delay Time				218	tPLH =		5210	See	2.5. Vde	ns
Reset to Cout				0.62					Show A No	HOVI
tpLH = (1.7 ns/pF) CL + 315 n	s acc_			811		5.0	-	400	800	MOV)
tpLH = (0.66 ns/pF) CL + 142	ns			- 20		10	-	175	350	
tpLH = (0.5 ns/pF) CL + 100 n	S			- 4		15	-	125	250	HOV)
Clock Pulse Width	1	1000			tWH	5.0	250	125	-	ns
				1		10	100	50	06 V 8.0	TOM
				3.5		15	75	35	1.6 V do	TOA
OL 1 F	10000 0 :		1.01			-		- Linning	20	2411
Clock Frequency					fcl	5.0	-	5.0	2.0	MH:
						10	-	12	5.0	-
	0.0					15	-	16	6.7	PA D 10
Reset Pulse Width					tWH	5.0	500	250	- 10	ns
				-		10	250	125	Curuent I	1000389
						15	190	95	(egs/s)	19 1091
Reset Removal Time	810.0		05		trem	5.0	750	375	_	ns
20 - I ISB - PAd				-	8.0	10	275	135	town 0	Residen
				-		15	210	105	(4000	19 16 PE
Clock Input Rise and Fall Time	aro.e		08			5.0	-	1		1
					TLH, THL	10	1	No Limit		Duz Te
						15				
	T (SHIN) AUL OS			-		-			1 1000	-
Clock Enable Setup Time					t _{su}	5.0	350	175	of one de de	ns
						10	150	75	in produced	
and the second second second					1	15	115	52	s sw <u>it</u> chile	PHOG
Clock Enable Removal Time	9.0				trem	5.0	420	260	en 32 aa-	ns
				1 9	Device	10	200	100	+12500	rigin?
				1		15	140	70	vi itumi	00101

^{*} The formulae given are for the typical characteristics only.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range V_{SS} < (V_{in} or V_{out}) < V_{DD}.

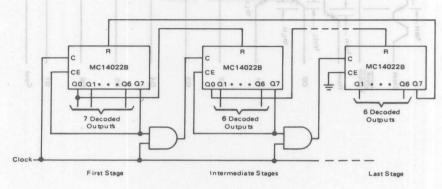
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD).

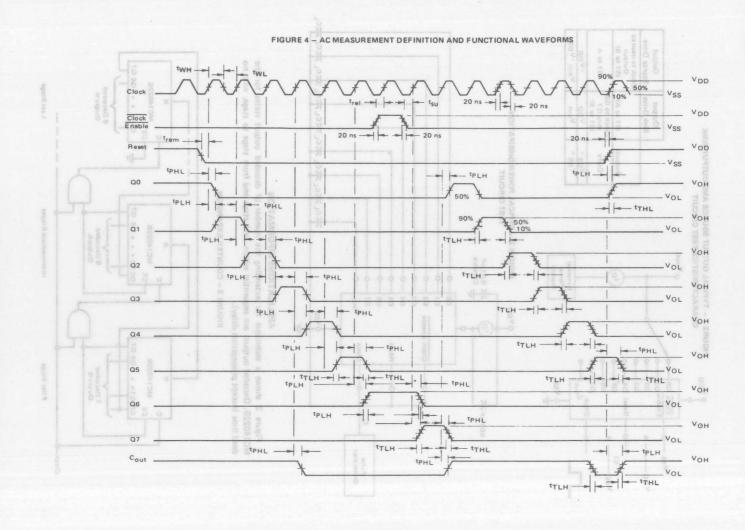


APPLICATIONS INFORMATION

Figure 3 shows a technique for extending the number of decoded output states for the MC14022B. Decoded outputs are sequential within each stage and from stage to stage, with no dead time (except propagation delay).

FIGURE 3 - COUNTER EXPANSION





3-7



MC14023B MC14023UB

TRIPLE 3-INPUT "NAND" GATE

The MC14023B and MC14023UB are constructed with P and N channel enhancement mode devices in a single monolithic structure (Complementary MOS). Their primary use is where low power dissipation and/or high noise immunity is desired.

- Quiescent Current = 0.5 nA typ/pkg @ 5 Vdc
- Noise Immunity = 45% of VDD typ
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered (MC14023B only)
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range. (MC14023B only)
- Double Diode Protection on All Inputs
- Pin-for-Pin Replacements for CD4023B and CD4023UB.

MAXIMUM RATINGS (Voltages referenced to VSS)

Rating	Symbol	Value	Unit
DC Supply Voltage	VDD	-0.5 to +18	Vdc
Input Voltage, All Inputs	Vin	-0.5 to V _{DD} +0.5	Vdc
DC Current Drain per Pin	11.1	10	mAdd
Operating Temperature Range - AL Device CL/CP Device	TA	-55 to +125 -40 to +85	оС
Storage Temperature Range	Tstg	-65 to +150	°C

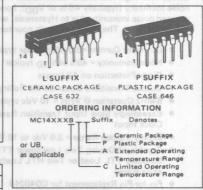
See the MC14001B data sheet for complete characteristics of the B-Series device.

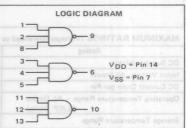
See the MC14001UB data sheet for complete characteristics for the UB device.

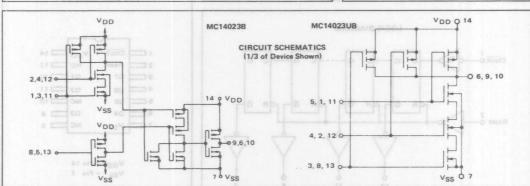
CMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

TRIPLE 3-INPUT "NAND" GATE







This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields, however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper

operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leqslant (V_{in}$ or $V_{out}) \leqslant V_{DD}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

3

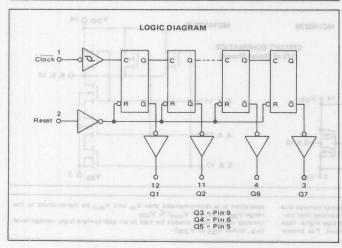
SEVEN STAGE RIPPLE COUNTER

The MC14024B is a seven stage ripple counter with short propagation delays and high maximum clock rates. The Reset input has standard noise immunity (typically 45% of $V_{\overline{\rm DD}}$), however the $\overline{\rm Clock}$ input has increased noise immunity due to Hysteresis, with no maximum Clock input rise or fall time. The output of each counter stage is buffered.

- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- Noise Immunity = 45% of VDD typical
- Diode Protection on All Inputs
- Output Transitions Occur on the Falling Edge of the Clock Pulse
 - 8-MHz Operation @ VDD = 10 Vdc typical
 - Exceedingly Slow Input Transition Rates may be Applied to the Clock Input
 - Supply Voltage Range = 3.0 Vdc to 18 Vdc
 - Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range
 - Pin-for-Pin Replacement for CD4024B

MAXIMUM RATINGS (Voltages referenced to Vss)

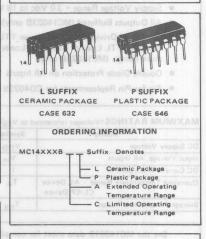
Rating	Symbol	Value	Unit
DC Supply Voltage	V _{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	Vin	-0.5 to V _{DD} + 0.5	Vdc
DC Current Drain per Pin	1	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	TA	-55 to +125 -40 to +85	°C
Storage Temperature Range	T _{stg}	-65 to +150	°С



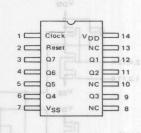
CMOS SSI

(LOW POWER COMPLEMENTARY MOS)

SEVEN STAGE
RIPPLE COUNTER



PIN ASSIGNMENT



V_{DD} = Pin 14 V_{SS} = Pin 7

NC = No Connection

ELECTRICAL CHARACTERISTICS

			VDD						Th		
Characteristic		Symbol	Vdc	Min	Max	Min	Тур	Max	Min	Max	Unit
ne "0" L	Level	VOI	5.0	-	0.05	-	0	0.05	To (ad/s	0.05	Vdc
010	-	037	10	_	0.05	-	0	0.05	70 Test/8	0.05	4.1
40 80	-	81	15	-	0.05	-	0	0.05	JO [Role	0.05	A1
"1" L	Level	VOH	5.0	4.95	-	4.95	5.0	-	4.95	entil Tale 13	Vdc
VDD	-	nig 1	10	9.95	_	9.95	10		9.95		TI
007 08	-	10	15	14.95	-	14.95	15	n 3.51 +	14.95	BC (0) = 16	41
0.	" Level	VII						BLOS A	Po Londzan	ed m = 11	Vdc
			5.0	-	1.5		2.25	1.5	egull y	1.5	Proper
			10		3.0	-	4.50	3.0	-	3.0	010
	- 1	6.0	15	-		-	6.75	4.0	17.11 - 3	4.0	
	" Level	VIL					67 7 1 1 7	JUL TO VAN	80.U/ - 7	H41, H141	
	-	- 10	5.0	3.5	-	3.5	2.75	13 [30/8	3.5	HELTHIAL	Vdc
				21.75	-			-		KD_pt sta	10
	-	5.0	15	1.00	_			"b] Jah	ALT DE S	Hal Trial	
THE CHIEF	10	lou		1110		1	-	13 13 9/10	200.01	17 15J T	mAdc
		OH .	5.0	-30	-	-24	-4.2	TO LAME	-1.7	Hot Hilds	
										nE7 03 103	374
	-							30 14d/s		HAT "H" ANH	
								(D) (Fighan		HAL'W' LAN	100
						-	-			1000	mAdo
										Pulls That	MAGC
						1					
		27	15	4.2	-	3.4	8.8	_	2.4	-	
		ОН							1 4	Puise Widt	mAdc
	e	. 01			-	775505				-	100
	260	81		50000	-					-	
	825	6.8		1	-		1			T townson-P	Reset
.5 Vdc)	190	02	15	-3.6	-	-3.0	-8.8	-	-2.4	-	
Vdc) Sink	145	IOL	5.0	0.52	-	0.44	0.88	-	0.36	-	mAdc
Vdc)		0.8	10	1.3	-	1.1	2.25	20000	0.9	and Transit	doelO
Vdc)		01	15	3.6	-	3.0	8.8	-	2.4	-	
(AL Device)		lin	15	-	± 0.1	-	±0.00001	± 0.1	-	± 1.0	μAdc
(CL/CP Device)	-		15	-1	± 0.3	-	±0.00001	± 0.3	3'2091	±1.0	μAdc
			_			-	5.0	7.5	-	_	pF
12 4.0	-	olu e			1		0.0	7.5			
rent (AL Device)	-	Inn	5.0	-	5.0	1 -	0.005	5.0	-	150	μAdc
		100		_	110000000000000000000000000000000000000	to apirali			not are no	PARE COSTULTY	07 313
					20		1 1000000000000000000000000000000000000		-	-	
root ICL ICP Device	(2	lan				-	-				0 -1
and the second s	61	DD							-		μAdc
ye i						-			-		
2	-				80					600	-
		T									μAdc
			15			T = (0.	89 μA/kHz	1 + IDD			
F on all outputs, a ritching)				BJEATI							
	VDD "1" VDD "1" VDD "1" "0 or 0.5 Vdc) or 1.0 Vdc) or 1.0 Vdc) or 1.5 Vdc) or 1.5 Vdc) or 3.5 Vdc) Current (AL Device) 5 Vdc) (Current (CL/CP Device) 5 Vdc) (AL Device) (CL/CP Device) ince rent (AL Device) ge) Current **† plus Quiescent, ge) F on all outputs, a	y or 0 "1" Level "0" Level "0" Level or 1.5 Vdc) or 1.5 Vdc) or 1.5 Vdc) or 1.5 Vdc) Current (AL Device) 5 Vdc) 6 Vdc) 5 Vdc) 6 Vdc) 5 Vdc) 6 Vdc) 5 Vdc) 5 Vdc) 6 Vdc) 5 Vdc) 6 Vdc) 5 Vdc) 6 Vdc) 6 Vdc) 6 Vdc) 5 Vdc) 6 Vd	VOD	O or 0	Vod	10	10	10	10	10	10

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in} \text{ or } V_{out})$ < VDD.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD).

^{*}T_{low} = -55°C for AL Device, -40°C for CL/CP Device. T_{high} = +125°C for AL Device, +85°C for CL/CP Device. =Noise immunity specified for worst-case input combination.

Noise Margin for both "1" and "0" level = 1.0 Vdc min @ VDD = 5.0 Vdc 2.5 Vdc min @ VDD = 15 Vdc 2.5 Vdc min @ VDD = 15 Vdc

¹To calculate total supply current at loads other than 50 pF:

| T(C_L) = | T₁(50 pF) + 1 x 10⁻³ (C_L -50) V_{DD}f

where: | T₁ is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.

**The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS* (CL = 50 pF, TA = 25°C)

Characte	ristic			Symbol	VDD	Min	Тур	Max	Unit
Output Rise Time	gyT	mild	NaN	tTLH T	Symbol		aidzinad	Charac	ns
tTLH = (3.0 ns/pF) CL + 30 ns				- 0.8	5.0	lave J	100	200	V man
tTLH = (1.5 ns/pF) CL + 15 ns				- 07	10	-	50	100	n.V
tTLH = (1.1 ns/pF) CL + 10 ns	1 0			- E at	15	-	40	80	615
Output Fall Time	B.è	4.95		tTHL	Tank!	IsvaJ	igit.		ns
tTHL = (1.5 ns/pF) CL + 25 ns				10 9.9	5.0	-	100	200	Vin
tTHL = (0.75 ns/pF) CL + 12.5	ns			18 14.98	10	-	50	100	1
tTHL = (0.55 ns/pF) CL + 9.5 ns					15	Town 1 170	40	80	No. of London
Propagation Delay Time	2.25		8.4	tPLH,			lesson.	3.0 to 8.	ns
Clock to Q1				tPHL			Indian.	0.1 40 0.1	OVI
tpLH, tpHL = (1.7 ns/pF) CL	+ 295 ns			ar ar	5.0	-	380	600	- ovi
tpLH, tpHL = (0.66 ns/pF) (L + 117 ns				10	Invest or	150	230	1911
tpLH, tpHL = (0.5 ns/pF) CL	+ 85 ns			50 33	15	-	110	175	-6V9-
Clock to Q7				10 7.0			(shar	de in a	OVI
tpLH, tpHL = (1,7 ns/pF) C	+ 915 ns			15 11.0	5.0	-	1000	3000	- /5VI
tpLH, tpHL = (0.66 ns/pF) (L + 367 ns			1000	10	-	400	750	-
tpLH, tpHL = (0.5 ns/pF) CI	+ 275 ns			0.8- 0.8	15	_ 100	300	565	nd rugin
Reset to Qn				5.0 -3.0	1	95	hoc		HO.VI
tPLH, tPHL = (1.7 ns/pF) C	+ 415 ns				5.0	-	500	800	HOV)
tpLH, tpHL = (0.66 ns/pF) (01 — 01 01 — 01	10	-	250	400	HOV
tpLH, tpHL = (0.5 ns/pF) C				78- 01	15	-	180	300	HOV
Clock Pulse Width	88.0	16.0		twH	5.0	500	200	120 K + 0	ns
- 0.0				0.1 1 01	10	165	60	0.5.V.6c)	30 VI
- 2.6 -		3.4		S.A. 21	15	125	40	1,5_2/00	1017
Reset Pulse Width				twH	5.0	600	375	rent <u>u</u> D ev	ns
n =1.7 =				5.0 -2.5	10	350	200	2 5_Vdc)	HOVI
				5.0 -0.02	15	260	150	4.8_Vdg)	HOV
Reset Removal Time	62.2-	1.1-		6.7- 01	5.0	625	250	130 A C S	ns
				trem	10	190	75	13.5 Vide	HON
				6:0 0.83	15	145	50	0.4_3/863	10V)
Clock Input Rise and Fall Times	67.7	100		tTLH, THL	5.0	_	_	0	TOAL
				DE . 211, 1112	10	_	_	8.0	ms
				- 31	15	_	<u>fararen</u>	200	μs
Input Pulse Frequency	10000.0±	-	€.0.5	fcl	5.0	-	2.5	1.0	MHz
				'CI	10	-	8.0	3.0	aut Capa
					15	-	. 12	4.0	- Wi

^{*} The formulae given are for the typical characteristics only.

TRUTH TABLE

CLOCK	RESET	STATE
0	0	No Change
0	1	All Outputs Low
1	0	No Change
1	1 ab	All Outputs Low
	0	No Change
	1	All Outputs Low
_	0	Advance One Count
	1	All Outputs Low



VDD VOL * Vout

VDD VOUT

VDD VOUT

VD VOUT

VD VOUT

VD VOUT

VD VOUT

VD VOU

FIGURE 2 – TYPICAL OUTPUT SINK CHARACTERISTICS TEST CIRCUIT

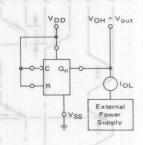


FIGURE 3 - POWER DISSIPATION TEST CIRCUIT

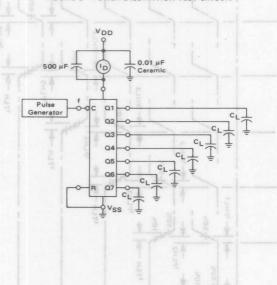
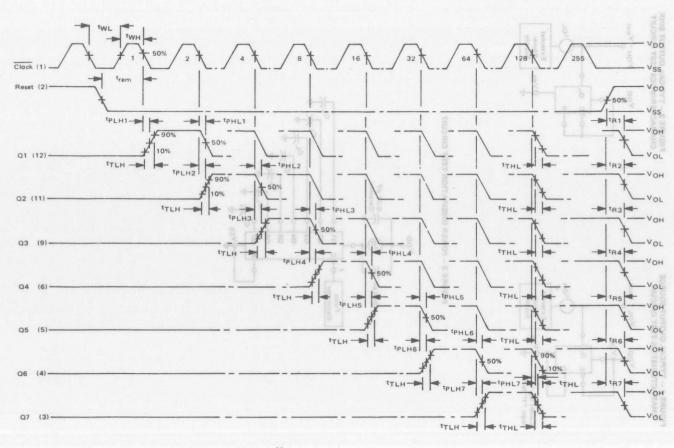


FIGURE 4 - FUNCTIONAL WAVEFORMS



Input tTLH and tTHL = 20 ns



MC14025B MC14025UB

TRIPLE 3-INPUT "NOR" GATE

The MC14025B and MC14025UB are constructed with P and N channel enhancement mode devices in a single monolithic structure (Complementary MOS). Their primary use is where low power dissipation and/or high noise immunity is desired.

- Quiescent Current = 0.5 nA typ/pkg @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typ
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered (MC14025B only)
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range. (MC14025B only)
- Double Diode Protection on All Inputs
- Pin-for-Pin Replacements for CD4025B and CD4025UB.

MAXIMUM RATINGS (Voltages referenced to VSS)

astone Rating 2 - 8XXX	Symbol	Value	Unit
DC Supply Voltage	VDD	-0.5 to +18	Vdc
Input Voltage, All Inputs	Vin	-0.5 to V _{DD} +0.5	Vdc
DC Current Drain per Pin	1	10	mAdc
Operating Temperature Range AL Device CL/CP Device	TA	-55 to +125 -40 to +85	°C
Storage Temperature Range	T _{stg}	-65 to +150	°C

See the MC14001B data sheet for complete characteristics of the

See the MC14001UB data sheet for complete characteristics for the non-B device.

CMOS SSI

(LOW POWER COMPLEMENTARY MOS)

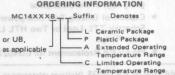
TRIPLE 3-INPUT "NOR" GATE

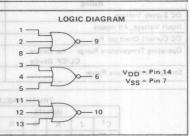


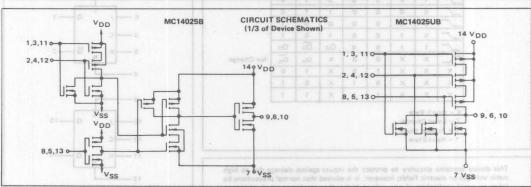
CERAMIC PACKAGE PLASTIC PACKAGE CASE 632

CASE 646

ORDERING INFORMATION







This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper

operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leqslant (V_{in} \text{ or } V_{out}) \leqslant V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD).

INTERPTORIES

DUAL J-K FLIP-FLOP

The MC14027B dual J-K flip-flop has independent J, K, Clock (C), Set (S) and Reset (R) inputs for each flip-flop. These devices may be used in control, register, or toggle functions.

- Quiescent Current = 2.0 nA/package typical @ 5 Vdc
- Noise Immunity = 45% of VDD typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Single Supply Operation Positive or Negative
- Toggle Rate = 3.0 MHz typical @ 5 Vdc
- Logic Swing Independent of Fanout
- Logic Edge-Clocked Flip-Flop Design Logic state is retained indefinitely with clock level either high or low; information is transferred to the output only on the positivegoing edge of the clock pulse
 - Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range
 - Pin-for-Pin Replacement for CD4027B

MAXIMUM RATINGS (Voltages referenced to Voc.)

Rating	Symbol	Value	Unit
DC Supply Voltage	VDD	-0.5 to +18	Vdc
Input Voltage, All Inputs	Vin	-0.5 to V _{DD} + 0.5	Vdc
DC Current Drain per Pin	1	10	mAdc
Operating Temperature Range AL Device CL/CP Device	TA	-55 to +125 -40 to +85	°C
Storage Temperature Range	T _{stg}	-65 to +150	ос

TR	LIT	M T	FA	DI.	c

Ditt	UTS*	OUTP		12	JTS	INPL	-0(10
T	$\overline{Q_{n+1}}$	Q _{n+1}	Qn‡	R	S	K	J	C†
-	0	1	0	0	0	X	1	5
	0	1	1	0	0	0	Х	7
100	1	0	0	0	0	X	0	
	1	0	1	0	0	1	×	7
	Qo	Qo	Qo	0	0	1	1	
No	$\overline{\alpha}_n$	Qn	×	0	0	×	×	7
G.A.	0	1	X	0	1	X	X	X
	1	0	×	1	0	×	×	×
	4		1					~

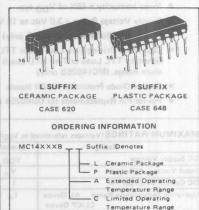
- X = Don't Care
- t = Level Change
- ‡ = Present State
- * = Next State

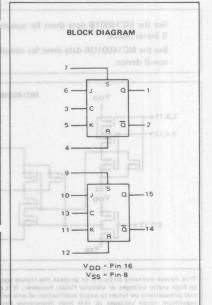
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that Vin and Vout be constrained to the range VSS < (Vin or Vout) < VDD. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD).

CMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

DUAL J-K FLIP-FLOP



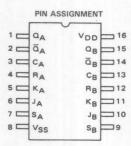


Change

ELECTRICAL CHARACTERISTICS

	NEW		MIN	00x	VDD	Tlo	w"		25°C	NO DETAINS	Th	igh *	-
611	Charact	eristic		Symbol	Vdc	Min	Max	Min	Тур	Max	Min	Max	Unit
Output V	oltage	0	" Level	VOL	5.0		0.05	-	0	0.05	100	0.05	Vdc
Vin =	V _{DD} or 0			15	10		0.05	-	0	0.05	13 640	0.05	71.42
				91	15	_	0.05	-	0	0.05	PF) CL +	0.05	UT.
		1	" Level	VOH	5.0	4.95	-	4.95	5.0	-	4.95	2010 107	Vdc
Vin "	O or VDD		-	1000	10	9.95	_	9.95	10	25 ns	9.95	an 8,71 =	HE
	007		-	07	15	14.95	-	14.95	15	12.5 ns	14.95	= 10,75 a	HT7
Input Vol	tage #		"0" Level	VIL						30 0.81	30.1400	10000	Vdc
200	4.5 or 0.5			"-	5.0		1.5	-	2.25	1.5	<u>e</u> miT	1.5	agedo.
	9.0 or 1.0				10	_	3.0	-	4.50	3.0	-	3.0	Cioc
	13.5 or 1.5		-	0.0	15		4.0	-	6.75	4.0	an 1_11 =	4.0	1
			"1" Level	VIH					वार देख	"In (4d)	H 60.0) *	JHTP HJE	7
(VO =	0.5 or 4.5	/dc)	-	61	5.0	3.5	_	3.5	2.75	+ JD (Rg	3.5	JHT HIS	Vdc
	1.0 or 9.0 V				10	7.0	_	7.0	5.50	-	7.0	0.0	265
	1.5 or 13.5			0.8	15	11.0		11.0	8.25	+ 10 (99	11.0	PLH, IPHIL	
	ive Current		vice)	ГОН				11.0	0.20	3 (Fight	1	215 T 152	mAdo
	= 2.5 Vdc)		urce	·On	5.0	-3.0	_	-2.4	-4.2	PF) CL +	-1.7	THAT HTA	
	= 4.6 Vdc)		1		5.0	-0.64	_	-0.51	-0.88		-0.36	Port	Pass Fi
	= 9.5 Vdc)		-	0.8	10	-1.6	_	-1.3	-2.25	+ 15 (39	-0.9	PEH, TPHE	
0	= 13.5 Vdc		-	01	15	-4.2	-	-3.4	-8.8	JOT (Pigl)	-2.4	1H92 HJ9	
	= 0.4 Vdc)	Sir	k	IOL	5.0	0.64	_	0.51	0.88	-10110	0.36		mAdo
	= 0.5 Vdc)		10000		10	1.6		1.3	2.25		0.9	agens	THE STATE OF
	= 1.5 Vdc)		00	101	15	4.2	_	3.4	8.8		2.4	_	
	ive Current		_					-	0.0		290	niT blott m	mAdo
	= 2.5 Vdc)		urce	ІОН	5.0	-2.5		-2.1	-4.2		-1.7	R I Diper in	IIIAuc
0	= 4.6 Vdc)		1	10	5.0	-0.52		-0.44	-0.88		-0.36		
0	= 9.5 Vdc)		35	- 15	10	-1.3		-1.1	-2.25		-0.9		
	= 13.5 Vdc	166	330	6.0	15	-3.6	_	-3.0	-8.8		-2.4	utge Wicton	Hospit P
			011	01		0.52	_	-		_		-	0.4
	= 0.4 Vdc)	Sir	nk av	IOL	5.0	0.000	_	0.44	0.88	_	0.36	-	mAdd
	= 0.5 Vdc)		-	6.0	15	1.3 3.6		3.0	8.8		0.9	superit cale	Stock F
	= 1.5 Vdc)	0.8		-01				-			-		
	rent (AL De	12 10 10 10 10 10	-	lin	15		± 0.1	-	±0.00001	±0.1	-	±1.0	μAdc
	rent (CL/CI	Device)		lin	15	175-	± 0.3	-	±0.00001	± 0.3	IT Its 9 be	±1.0	μAdc
Input Cap (V _{in} =			-	Cin	-		-	-	5.0	7.5	-	-	pF
Quiescent	Current (A	L Device	280 (IDD	5.0	-	1.0	-	0.002	1.0	rith(W)	30	μAdc
(Per Pa	ickage)		100	03	10	-	2.0	-	0.004	2.0	-	60	1.2.9
	- 1	36	70	31	15		4.0	-	0.006	4.0	-	120	
Quiescent	Current (C	L/CP De	vice)	IDD	5.0	- 1	4.0	o salisis	0.002	4.0	ol dis no	30	μAdo
(Per Pa	ickage)		-		10		8.0	-	0.004	8.0	-	60	
					15	-	16	-	0.006	16	-	120	
Total Sup	ply Current	**†		· IT	5.0			IT = (0	.80 μA/kHz) f + Ipp			μAdd
(Dynar	nic plus Qu	iescent,	1100		10	. 100		IT = (1	.60 µA/kHz) f + Ipp			
	ickage)				15	TO BE			.40 μA/kHz				
(CL = !	50 pF on al	outputs	s, all							50			
buffer	s switching)											

†To calculate total supply current at loads other than 50 pF: $I_{T}(C_{L}) = I_{T}(50 \text{ pF}) + 2 \times 10^{-3} \text{ (}C_{L} - 50\text{) V}_{DD}\text{f}$ where: I_{T} is in μA (per package), C_{L} in pF, V_{DD} in Vdc, and f in kHz is input frequency. **The formulas given are for the typical characteristics only at 25°C.



 $^{^*}T_{low} = -55^{o}C$ for AL Device, $-40^{o}C$ for CL/CP Device. $T_{high} = +125^{o}C$ for AL Device, $+85^{o}C$ for CL/CP Device. "Noise immunity specified for worst-case input combination.

Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc 2.0 Vdc min @ V_{DD} = 10 Vdc 2.5 Vdc min @ V_{DD} = 15 Vdc

CI	naracte	ristic			T. June	S	ymbol	VDD	Min	Тур	Max	Unit
Output Rise Time	xsM	Typ	rishi	asM.	I	1	TLH	todmy2		piteines	Charac	ns
tTIH = (3.0 ns/pF) CI + 30					-			5.0	Tave J	100	200	Vitua
tTLH = (1.5 ns/pF) CL + 15								10	1909.3	50	100	
tTLH = (1.1 ns/pF) CL + 10								15	-	40	80	niV
Output Fall Time	2000	A	-	0.05								ns
					1 9	E.A.	THE	5.0	feveJ	100	200	
tTHL = (1.5 ns/pF) CL + 25					1 8	8.6		1	-		100	niV
t _{THL} = (0.75 ns/pF) C _L + 1					1 4	14.8		10	-	50		les t
tTHL = (0.55 ns/pF) CL +	12.5 ns							15	love 1 "O"	40	80	HoV-se
Propagation Delay Time	3.5					t	PLH,			(abV		ns
Clock to Q		00.5				1	TPHL	1 6 4		CodstA		- ov
tpLH, tpHL = (1.7 ns/pl					1.			5.0	-	175	350	o oV
tpLH, tpHL = (0.66 ns/s	F) CL	+ 42 ns			1			10	Section 1 772	75	150	1
tpLH, tpHL = (0.5 ns/pl	F) CL +	+ 25 ns						15	TovoJ "T	50	100	ROV
Set to Q					1 1	16.		-		15000	0.0 10.0	-
tPLH, tPHL = (1.7 ns/pl	F) C1 4	+ 90 ns			1 1	3.0		5.0	-	175	350	BV
tpLH, tpHL = (0.66 ns/s	F) C	+ 42 ns			Li	2.11		10	-	75	150	ns
tpLH tpHL = (0.5 ns/pl	F) Ci +	+ 25 ns						15	_ (93	50	100	(C) tulo
Reset to Q		N.A-				8-			333	Le.2	Into V. A. C.	HOV
tPLH. tPHL = (1.7 ns/pl	F) Ci +	+ 265 ns			148	1.0-		5.0	-	350	450	HOV
tPLH, tPHL = (0.66 ns/s	F) C	+ 67 ns				1-		10	_	100	200	ns
tplH tpHL = (0.5 ns/pl	F) Ci d	+ 50 ns				P-		15	_	75	150	HOV
Setup Times	-	88:0	18.0		-	0.0	. U.S	5.0	140	70	CONTRO	ns
setup Tilles						3.7	tsu	10	50	25	0.5 Vac	Jov
2.4		8.8	3.4			13		15	35	17	1.5 Vde	JOV
Minimum Hold Times	-	1			-	-					ve Curren	-
William Floid Times						2	th	5.0	140	70	2.5_Videl	ns
						0-		10	50	25		HOV
		00.0	e mon	7	1 33	- U	0.0	15	35	17	latiV_B, i-	HOY
Clock Pulse Width						tW	H, tWL	5.0	330	165	WALL ST. C. C.	ns
								10	110	00	13 5 Vd	1 1 1
0.36 - mAde					1 5	0.5		15	75	38	0,4_Pdc)	JOY
Clock Pulse Frequency	-	92.5				S. I.	fcl	5.0	-	3.0	1.5	MH:
2.4						3.6	'cl at	10	-	9.0	4.5	LOV
						-		15	-	13	6.5	NUO 16
Clock Pulse Rise and Fall Time	± 0,3	10000 0:		€03		tTI	H, THL	5.0	-	Р Оршсе	15	μѕ
							,	10	-	-	5.0	di O h
								15	-	-	4.0	N. V
et and Reset Pulse Width	1.0	0.002		0.7	1		hw	5.0	250	125	il tomasus	ns
08							HW	10	100	50		9 119
								15	70	35	- Allen	1 100

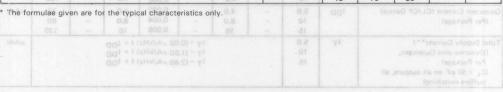




FIGURE 2 - DYNAMIC SIGNAL WAVEFORMS FIGURE 1 - DYNAMIC SIGNAL WAVEFORMS (Set, Reset, and Output) (J, K, Clock, and Output) - 20 ns 20 ns ---VDD. - 20 ns -VDD 90% -Vss 50% HW CODER 20 ns VDD 10% Vss 20 ns -20 ns -90% HOCTAL DECODER VDD 90% 10%--Vss - twh 10% PHL _VOH 20 ns -Expanded decoding a ggVlw fugtue shoo DECODER 90% 50% -VOL 10% Tor code conversion agov. twH best to prixelablemen forthern J and K low. - twL fcl TPLH - tPHL -VOH 90% Noise Immunity = 45% of Vnn typical Q 50% Supply Voltage Range = 3.0 Vdc to 18 Vdc 10% Capable of Driving Two Low-power TTL Loads, One Low-power tTLH-Inputs R and S low. For the measurement of tWH, I/fcI, and PD the Inputs J and K are kept high. Positive Logic Design Ourescent Current 5.0 nA /package typical @ 5 Vdc . Low Outputs on All Illegal Input Combinatio LOGIC DIAGRAM Similar to CD4028B. (1/2 of Device Shown) SO-C KO 5 6 6 oā V_{OD} = Fin 16 V_{SS} = Fin 8

MC14028B

ACT4027B

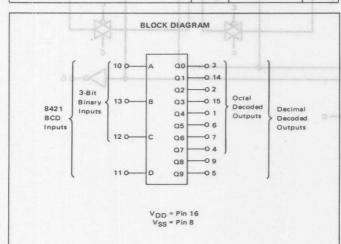
BCD-TO-DECIMAL DECODER BINARY-TO-OCTAL DECODER

The MC14028B decoder is constructed so that an 8421 BCD code on the four inputs provides a decimal (one-of-ten) decoded output, while a 3-bit binary input provides a decoded octal (one-of-eight) code output with D forced to a logic "0". Expanded decoding such as binary-to-hexadecimal (one-of-16), etc., can be achieved by using other MC14028B devices. The part is useful for code conversion, address decoding, memory selection control, demultiplexing, or readout decoding.

- Diode Protection on All Inputs
- Noise Immunity = 45% of V_{DD} typical
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range
- Positive Logic Design
- Quiescent Current 5.0 nA /package typical @ 5 Vdc
- Low Outputs on All Illegal Input Combinations
 ARDARG CHOOL
- Similar to CD4028B.

MAXIMUM RATINGS (Voltages referenced to Vss)

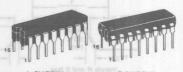
martinom tratting (voltages referenced	10 4221		
Rating	Symbol	Value	Unit
DC Supply Voltage	V _{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	Vin	-0.5 to V _{DD} + 0.5	Vdc
DC Current Drain per Pin	3	10	mAdc
Operating Temperature Range – AL Device CL/CP Device	TA	-55 to +125 -40 to +85	°C
Storage Temperature Range	T _{stg}	-65 to +150	°C



CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

BCD-TO-DECIMAL DECODER BINARY-TO-OCTAL DECODER



L SUFFIX CERAMIC PACKAGE CASE 620 P SUFFIX PLASTIC PACKAGE CASE 648

ORDERING INFORMATION

XXB Suffix Denotes

L Ceramic Package
P Plastic Package
A Extended Operating
Temperature Range
C Limited Operating
Temperature Range

TRUTH TABLE

	INF	TU					0	UT	PU	Т			
D	С	В	Α	Qg	0.8	Q7	Q6	Q5	Q4	Q3	Q2	Q1	QO
0	0	0	0	0	0	0	0	0	0	0	0	0	1
0	0	0	1	0	0	0	0	0	0	0	0	1	0
0	0	1	0	0	0	0	0	0	0	0	1	0	0
0	0	1	1	0	0	0	0	0	0	1	0	0	0
0	1	0	0	0	0	0	0	0	1	0	0	0	0
0	1_	0	1	0	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	0	1	0	0	0	0	0	0
0	1	1	1	0	0	1	0	0	0	0	0	0	0
1	0	0	0	0	1	0	0	0	0	0	0	0	0
1	0	0	1	1	0	0	0	0	0	0	0	0	0
1	0	1	0	0	0	0	0	0	0	0	0	0	0
1	0	1	1	0	0	0	0	0	0	0	0	0	0
1	1	0	0	0	0	0	0	0	0	0	0	0	0
1	1	0	1	0	0	0	0	0	0	0	0	0	0
1	1	1	0	0	0	0	0	0	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0	0	0	0	0

ELECTRICAL CHARACTERISTICS

nou rem Typ Max Uen	aav 1	VDD	Tio	w *		25°C	Characte	Thi	igh *	
Characteristic	Symbol	Vdc	Min	Max	Min	Тур	Max	Min	Max	Unit
Output Voltage "0" Level	VOL	5.0	-	0.05	-	0	0.05	- lo lade	0.05	Vdc
Vin VDD or 0	01	10	-	0.05	-	0	0.05	10-13e/	0.05	NAT.
OB OF -	18	15	-	0.05	-	0	0.05	10_(1g)	0.05	115
"1" Level	VOH	5.0	4.95	-	4.95	5.0	-	4.95	MINT 1874	Vdc
Vin - 0 or Vnn	0.0	10	9.95	-	9.95	10	26 ns	9.95	in 8.1) = 3	1111
007 08 -	10	15	14.95	-	14.95	15	BH 6721 4	14.95	1, = (0.75)	411
Input Voltage# "0" Leve	VIL						365 040	Try surfles	100.07	Vdc
(V _O = 4.5 or 0.5 Vdc)		5.0	-	1.5	-	2.25	1.5	SEDI-L.	1.5	Stobail.
(VO = 9.0 or 1.0 Vdc)	0.0	10	-	3.0	-	4.50	3.0	11.7 <u>n</u> s/pF	3.0	341
(V _O = 13.5 or 1.5 Vdc)	01	15	-	4.0	-	6.75	4.0	t/an_88.01	4.0	392
"1" Leve	VIH					400	00+73	10/20/9/01	TURN'S	ldr.
(V _O = 0.5 or 4.5 Vdc)		5.0	3.5		3.5	2.75	over-selt-	3.5	in sēlumn	Vdc
(V _O = 1.0 or 9.0 Vdc)		10	7.0	-	7.0	5.50	-	7.0	-	
(V _O = 1.5 or 13.5 Vdc)	1.12.14	15	11.0	-	11.0	8.25	-	11.0	-	
Output Drive Current (AL Device)	ГОН									mAdo
(VOH = 2.5 Vdc) Source		5.0	-3.0	-	-2.4	-4.2	-	-1.7	-	
(V _{OH} = 4.6 Vdc)		5.0	-0.64	-	-0.51	-0.88	-	-0.36	-	
(V _{OH} = 9.5 Vdc)		10	-1.6	-	-1.3	-2.25	-	-0.9	-	11.00
(V _{OH} = 13.5 Vdc)		15	-4.2	-	-3.4	-8.8	-	-2.4	-	
(VOI = 0.4 Vdc) Sink	IOL	5.0	0.64	-	0.51	0.88	-	0.36	-	mAdd
(V _{OL} = 0.5 Vdc)	2000	10	1.6	MATAYO	1.3	2.25	-	0.9	-	
(V _{OL} = 1.5 Vdc)	SHORT	15	4.2	-	3.4	8.8	-	2.4	-	230
Output Drive Current (CL/CP Device)	ТОН									mAdo
(VOH = 2.5 Vdc) Source		5.0	-2.5	-	-2.1	-4.2	-	-1.7	-	
(VOH = 4.6 Vdc)		5.0	-0.52	_	-0.44	-0.88	-	-0.36	-	
(VOH = 9.5 Vdc)		10	-1.3	100-	-1.1	-2.25	-	-0.9	-	
(V _{OH} = 13.5 Vdc)	ogv	15	-3.6	F - 20	-3.0	-8.8	-	-2.4	(ngu r s II)	
(VOL = 0.4 Vdc) Sink	IOL	5.0	0.52	980 2	0.44	0.88	-	0.36	animpher	mAdo
(V _{OL} = 0.5 Vdc)	esV	10	1.3		1.1	2.25	-	0.9	0.38 a 91	
(VOL = 1.5 Vdc)	68.	15	3.6	-	3.0	8.8	-	2.4		
Input Current (AL Device)	lin	15	-	± 0.1	,-	±0.00001	±0.1	-	±1.0	μAdc
Input Current (CL/CP Device)	lin	15	-	± 0.3	-	±0.00001	±0.3	-	±1.0	μAdc
Input Capacitance	Cin	_			-	5.0	7.5	-	-	pF
(V _{in} = 0)	-in					0.0	7.0			-
Quiescent Current (AL Device)	IDD	5.0	and - lake	5.0	nd -in-	0.005	5.0	-	150	μAdc
(Per Package)	100	10		10		0.010	10		300	
	1	15	12	20	1	0.015	20	-	600	100
Quiescent Current (CL/CP Device)	IDD	5.0	12 300	20	130.36	0.005	20	-	150	μAdd
(Per Package)	88.00	10		40		0.010	40		300	µAGC
		15	To-	80	100-1	0.015	80	elot @ bns	600	1
Total Supply Current**†	İ	5.0		00	110	.3 µA/kHz			000	μAdo
(Dynamic plus Quiescent,	HO JT	10	1			0.6 µA/kHz				MAGC
Per Package)		15	1			0.9 μA/kHz				
(C _L = 50 pF on all outputs, all	100	10			7 2011	, we will	· · · · · · · · · · · · · · · · · · · ·			LV
buffers switching)	10 V									

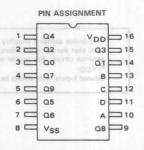
*Tlow = -55°C for AL Device, -40°C for CL/CP Device.

Thigh = +125°C for AL Device, +85°C for CL/CP Device.

#Noise immunity specified for worst-case input combination.

Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc

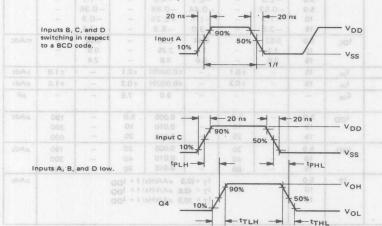
Noise Margin for both 1 and 0 level = 1.0 vac min @ V_{DD} = 5.0 vdc 2.0 vdc min @ V_{DD} = 10 vdc 2.5 vdc min @ V_{DD} = 15 vdc 1To calculate total supply current at loads other than 50 pF: $I_T(C_L) = I_T(50 \text{ pF}) + 1 \times 10^{-3} \text{ (C}_L - 50) \text{ V}_{DD}$ where: I_T is in μ A (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency. *The formulas given are for the typical characteristics only at 25°C.



Characteri	stic			Symbol	VDD	Min	Тур	Max	Unit
Output Rise Time	gyT	nibit	xall/i	tTLH '	Symbol		tavistic	Charac	ns
tTLH = (3.0 ns/pF) CL + 30 ns				0.6	5.0	16ve.1	100	200	V root
tTLH = (1.5 ns/pF) CL + 15 ns				0.1	10	-	50	100	
tTLH = (1.1 ns/pF) CL + 10 ns					15	-	40	80	- MISS
Output Fall Time	6.6	4.25		tTHL.	T Look	levaJ "	2.00		ns
t _{THL} = (1.5 ns/pF) C _L + 25 ns				10 9	5.0	-	100	200	ni V
tTHL = (0.75 ns/pF) CL + 12.5 ns				ar lar	10	-	50	100	- Inte
tTHL = (0.55 ns/pF) CL + 9.5 ns					15	January 1 11/01	40	80	
Propagation Delay Time	200.0		1.5	tPLH.		100000	telev	2.0 m 2.1	ns
tpLH, tpHL = (1.7 ns/pF) CL + 215	ns			tPHL	5.0	1-	300	600	200
tpLH, tpHL = (0.66 ns/pF) CL + 97				ai	10	-	130	260	200
tpLH, tpHL = (0.5 ns/pF) CL + 65 r	IS				15	Invited trans	90	180	00

* The formulae given are for the typical characteristics only.





All outputs connected to respective C_L loads. f in respect to a system clock.

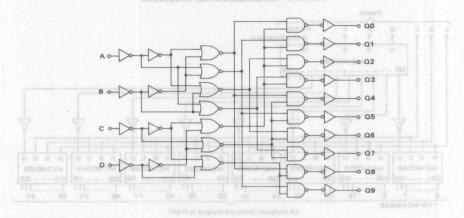
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in} \text{ or } V_{out})$

3-88

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD).

aeV = a

RECOGGE SE LOGIC DIAGRAM

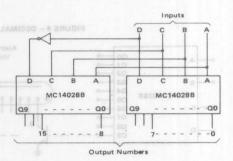


APPLICATION INFORMATION

Expanded decoding can be performed by using the MC14028B and other McMOS Integrated Circuits. The circuits in Figure 2 converts any 4-bit code to a decimal or hexadecimal code. The accompanying table shows the input binary combinations, the associated "output numbers" that go "high" when selected, and the "redefined output numbers" needed for the proper code. For example: For the combination DCBA = 0111 the output number 7 is redefined for the 4-bit binary, 4-bit gray, excess-3, or excess-3 gray codes as 7, 5, 4, or 2, respectively. Figure 3 shows a 6-bit binary 1-of-64 decoder using nine MC14028B circuits and two MC14069B inverters.

The MC14028B can be used in decimal digit displays, such as, neon readouts or incandescent projection indicators as shown in Figure 4.

FIGURE 2 – CODE CONVERSION CIRCUIT AND TRUTH TABLE



															+						E AND				D
																				Hexad	ecimal		Decin	nal	
1	NP	UTS	3					(וטכ	PL	1 T	NUN	иве	RS						4-Bit Binary	4-Bit Gray	xcess-3	xcess-3 Gray	Aiken	4221
D	С	В	A	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Big	40	Ex	Exc	A	A
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0			0	0
0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1			1	1
0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	2	3		0	2	2
0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	3	2	0	3	3	
0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	4	7	1	4	4	Г
0	1	0	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	5	6	2			3
0	1	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	6	4	3	1	1	4
0	1	1	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	7	5	4	2		
1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	8	15	5			Г
1	0	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	9	14	6			5
1	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	10	12	7	9		6
1	0	1	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	11	13	8		5	1
1	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	12	8	9	5	6	
1	1	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	13	. 9		6	7	7
1	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	14	11	1	8	8	8
1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	15	10		7	9	9

FIGURE 3 - SIX-BIT BINARY 1-OF-64 DECODER

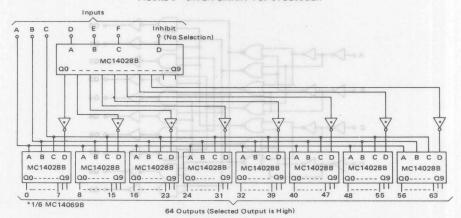
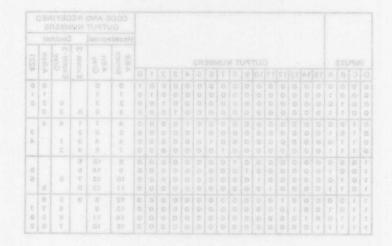


FIGURE 4 - DECIMAL DIGIT DISPLAY APPLICATION OF A PROPERTY OF THE PROPERTY OF and not below Appropriate guaruo Voltage suggest that = ASOG notisenide Voltage Q1 Q2 1 Neon Incandescent Display Display 03 04 MC14028B Q5 0.6 Q7 0 9 08 ouch as, nego

09

Expanded decoding can be performed by using the



MC14029B



BINARY/DECADE UP/DOWN COUNTER

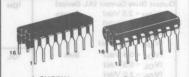
The MC14029B Binary/Decade up/down counter is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. The counter consists of type D flip-flop stages with a gating structure to provide toggle flip-flop capability. The counter can be used in either Binary or BCD operation. This complementary MOS counter finds primary use in up/down and difference counting and frequency synthesizer applications where low power dissipation and/or high noise immunity is desired. It is also useful in A/D and D/A conversion and for magnitude and sign generation.

- Quiescent Current = 5.0 nA/package typical @ 5.0 Vdc
- Noise Immunity = 45% of VDD typical
- Diode Proection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Low Input Capacitance 5.0 pF typical
 - Internally Synchronous for High Speed
 - Logic Edge-Clocked Design Count Occurs on Positive Going Edge of Clock
 - 8.0 MHz Counting Rate Typ at 10 Vdc
 - Asynchronous Preset Enable Operation
- Capable of Driving Two Low-Power TTL Loads,
 One Low-Power Schottky TTL Load or Two HTL Loads
 Over the Rated Temperature Range
- Pin for Pin Replacment for CD4029B

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

BINARY/DECADE
UP/DOWN COUNTER

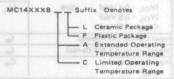


L SUFFIX CERAMIC PACKAGE CASE 620

8.1-

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION



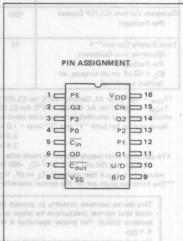
MAXIMUM RATINGS (Voltages referenced to Vss)

The state of the s	10 . 22		
Rating Rating	Symbol	Value	Unit
DC Supply Voltage	VDD	-0.5 to +18	Vdc
Input Voltage, All Inputs	Vin	-0.5 to V _{DD} + 0.5	Vdc
DC Current Drain per Pin	1	10	mAdc
Operating Temperature Range - AL Device CL/CP Device	TA	-55 to +125 -40 to +85	°С
Storage Temperature Range	T _{stg}	-65 to +150	°C

TRUTH TABLE

Carry In	Up/Down	Preset Enable	Action
1	X	0	No Count
0	et dir efect _i nc freids; in	0	Count Up
0	0	0	Count Down
×	X	1	Preset

X = Don't Care





MOTOROLA

ELECTRICAL CHARACTERISTICS

		VDD	TI	ow*		25°C		Th	igh *	
Characteristic	Symbol	Vdc	Min	Max	Min	Тур	Max	Min	Max	Unit
Output Voltage "0" Level	VOL	5.0	-	0.05	-	0	0.05	-	0.05	Vdc
V _{in} = V _{DD} or 0	-	10	-	0.05	-	0	0.05	-	0.05	
		15	-	0.05		0	0.05		0.05	
"1" Level	Vон	5.0	4.95	DIMAN	4.95	5.0	UNGS	4.95	10.07	Vdc
V _{in} = 0 or V _{DD}		10	9.95	-	9.95	10	est-Toronto	9.95	the MC1	
SOM LEMENSTAND HEAD-IN	par	15	14.95	unter is	14.95	15	inary/Di	14.95	1 DW 911	
Input Voltage# "0" Level	VIL	50	HARD RD	1000	STATERAL	a Ismitalion	IT DRS	SULBRUDS	L GOM (Vdc
(V _O = 4.5 or 0.5 Vdc)		5.0	edAT to	1.5	TREPLIES	2.25	1.5	nonalith	1.5	181
(V _O = 9.0 or 1.0 Vdc)		10 90	t-quit el	3.0	10-pro	4.50	3.0	es with	3.0	giff
(V _O = 13.5 or 1.5 Vdc)		15	100 t001	4.0	a ratitie	6.75	4.0	mudo se	4.0	can
"1" Level	VIH		ablau a	SSU VYKE	alan sho	retnuma i	IOM vist	namalon	This col	mit
(V _O = 0.5 or 4.5 Vdc)		5.0	3.5	pesizer	3.5	2.75	ma pnis	3.5	neraltib	Vdc
(V _O = 1.0 or 9.0 Vdc)		10	7.0	TOATEOU	7.0	5.50	- State	7.0	-	
(V _O = 1.5 or 13.5 Vdc)		15	11.0	TIONAMON	11.0	8.25	noutsqu	11.0	ורפ ופשע סו	riw
Output Drive Current (AL Device)	ІОН		E BOUTH	18(F) 10(F)	ME HOR	A COUAR	I bas u	AMINU	also dise	mAdc
(VOH = 2.5 Vdc) Source		5.0	-3.0	-	-2.4	-4.2	-	-1.70	generativ	ngia
(V _{OH} = 4.6 Vdc)	Time 1	5.0	-0.64	-	-0.51	-0.88	-	-0.36	-	
(V _{OH} = 9.5 Vdc)		10	-1.6	15.0-Vdq	-1.3	-2.25	= 5.0 nA	-0.9	ina sc eluí	- 0
(V _{OH} = 13.5 Vdc)	2007	15	-4.2	-	-3.4	-8.8	(No. 302)	-2.4	and Torint	-
(VOL = 0.4 Vdc) Sink	IOL	5.0	0.64	-	0.51	0.88	-	0.36	-	mAdc
(V _{OL} = 0.5 Vdc)		10	1.6	-	1.3	2.25	qni_llA	0.9	ode_Pro	
(VOL = 1.5 Vdc)		15	4.2	-	3.4	8.8 V	nge - 3.0	2.4	V vHqqui	
Output Drive Current (CL/CP Device)	ЮН				lst	nor Roya	l - sons	Cassaci	tion! wo.	mAdc
(VOH = 2.5 Vdc) Source		5.0	-2.5	-	-2.1	-4.2	-	-1.7	-	
(V _{OH} = 4.6 Vdc)		5.0	-0.52	-	-0.44	-0.88	toj snou	-0.36	nternally	
(V _{OH} = 9.5 Vdc)		10	-1.3	n Positiv	o #1.450	-2.25	d Design	-0.9	.agic-Edg	8
(V _{OH} = 13.5 Vdc)		15	-3.6	-	-3.0	-8.8	- Shoot	-2.4	Golne	
(VOL = 0.4 Vdc) Sink	OL	5.0	0.52	-	0.44	0.88	Rate Ty	0.36	SHM 0.	mAdc
(VOL = 0.5 Vdc)		10	1.3	-	1.1	2.25	-	0.9	A ZLUM OT	
(V _{OL} = 1.5 Vdc)		15	3.6	-	3.0	8.8	et Esabi	2.4	syndrino!	. 0
Input Current (AL Device)	1 _{in}	15	-	± 0.1	so.FJT	±0.00001	±0.1	Driving	±1.0	μAdc
Input Current (CL/CP Device)	lin	15	-bao	± 0.3	oT res bu	±0.00001	± 0.3	w-Powe	±1.0	μAdc
Input Capacitance	Cin	-	-	-	-	5.0	7.5	bate R s	17 18 1 O	pF
(V _{in} = 0)	- ""					- non-in-				
Quiescent Current (AL Device)	Ipp	5.0	-	5.0		0.005	5.0	DEIGEN !	150	μAdc
(Per Package)	.00	10	_	10	_	0.010	10	_	300	
		15	-	20	. ¬	0.015	20	-	600	
Quiescent Current (CL/CP Device)	IDD	5.0	-	20		0.005	20		150	μAdc
(Per Package)	.00	10		40		0.010	40		300	имас
11 01 2010301		15	_	80	_ 18	0.015	80	GS (Vol)	600	TUMIX,
Total Supply Current**†	IT	5.0		olsV	110	.58 µA/kHz		phitsB	000	A ala
(Dynamic plus Quiescent,	.1	10	914			1.2 μA/kHz				μAdc
Per Package)		15	-		-	1.2 μΑ/KHZ) 1.7 μΑ/kHz)				
(C ₁ = 50 pF on all outputs, all		1000	00.0		TTA	I.I MAIRIZ	טטי די			erloV 10
buffers switching)			1		1					Current

^{*}T_{Iow} = -55°C for AL Device, -40°C for CL/CP Device. Thigh = +125°C for AL Device, +85°C for CL/CP Device.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that Vin and Vout be constrained to the range VSS < (Vin or Vout) < VDD.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD).

[#]Noise immunity specified for worst-case input combination.

Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc

^{2.0} Vdc min @ VDD = 10 Vdc

^{2.5} Vdc min @ VDD = 10 Vdc

2.5 Vdc min @ VDD = 15 Vdc

†To calculate total supply current at loads other than 50 pF: '

IT(C_L) = IT(50 pF) + 1 x 10⁻³ (C_L -50) VDDf

where: IT is in μA (per package), C_L in pF, VDD in Vdc, and f in kHz is input frequency.

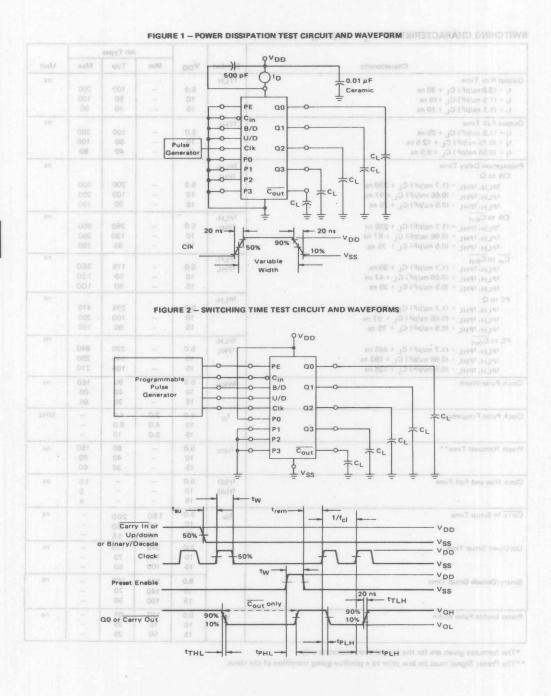
*The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS* (CL = 50 pF, TA = 25°C)

	aavo				All Types		
Characteristic		Symbol	VDD	Min	Тур	Max	Unit
Output Rise Time	0.0	tTLH					ns
t _r = (3.0 ns/pF) C _L + 30 ns			5.0	-	100	200	
t _r = (1.5 ns/pF) C _L +15 ns			10	-	50	100	
t _r = (1.1 ns/pF) C _L + 10 ns		1	15	-	40	80	
Output Fall Time		tTHL					ns
tf = (1.5 ns/pF) CL + 25 ns		1	5.0	-	100	200	
t _f = (0.75 ns/pF) C _L + 12.5 ns	CI ⁿ	1-0-	10	7-	50	100	
t _f = (0.55 ns/pF) C _L + 9.5 ns		0-	15	a -	40	80	
Propagation Delay Time	- 50	tPLH,					ns
Clk to Q		tPHL					
tp_H, tpHL = (1./ ns/pF) CL + 230 ns			5.0	-	200	400	
tpLH, tpHL = (0.66 ns/pF) CL + 97 ns			10	-	100	200	
tpLH, tpHL = (0.5 ns/pF) CL + 75 ns	13		15	-	90	180	
Clk to Cout		tPLH,					ns
tpLH, tpHL = (1.7 ns/pF) CL + 230 ns		tPHL .	5.0	-	250	500	
tpLH, tpHL = (0.66 ns/pF) CL + 97 ns			10	-	130	260	
tpLH, tpHL = (0.5 ns/pF) CL + 75 ns			15	-	85	190	
Cin to Cout		tPLH,	erico-			Head	ns
tpLH, tpHL = (1.7 ns/pF) CL + 95 ns	Answer	TPHL	5.0	-	175	360	
tpLH, tpHL = (0.66 ns/pF) CL + 47 ns			10	-	50	120	
tpLH, tpHL = (0.5 ns/pF) CL + 35 ns			15	-	50	100	
PE to Q		tPLH,					ns
tpLH, tpHL = (1.7 ns/pF) CL + 230 ns / AM CMA TRUCK		TPHL	5.0	UDIT	235	470	
tPLH, tPHL = (0.66 ns/pF) CL + 97 ns			10	-	100	200	
		1					
tpLH, tpHL = (0.5 ns/pF) CL + 75 ns			15	-	80	160	
TPLH, TPHL = (0.5 ns/PF) CL + 75 ns PE to Cout		tPLH,	15	-	80	160	ns
PE to Cout tp_H, tpHL = (1.7 ns/pF) CL + 465 ns	vo	tPLH,	5.0	_	320	640	ns
PE to Cout tp_H, tpHL = (1.7 ns/pF) C _L + 465 ns tp_H, tpHL = (0.66 ns/pF) C _L + 192 ns	1		5.0	-	320 145	640 290	ns
PE to C _{out} tpLH, tpHL = (1.7 ns/pF) C _L + 465 ns	1		5.0	_	320	640	ns
PE to Cout tplH, tpHL = (1.7 ns/pF) CL + 465 ns tplH, tpHL = (0.66 ns/pF) CL + 192 ns tpLH, tpHL = (0.5 ns/pF) CL + 125 ns	39	^t PHL	5.0	-	320 145	640 290	ns
PE to Cout tp_H, tpHL = (1.7 ns/pF) CL + 465 ns tp_H, tpHL = (0.66 ns/pF) CL + 192 ns tp_H, tpHL = (0.5 ns/pF) CL + 125 ns	39		5.0 10 15	-	320 145 105	640 290 210	
PE to Cout tplH, tpHL = (1.7 ns/pF) CL + 465 ns tplH, tpHL = (0.66 ns/pF) CL + 192 ns tplH, tpHL = (0.5 ns/pF) CL + 125 ns	39	^t PHL	5.0 10 15	- Copramolis Pulsa	320 145 105	640 290 210	
PE to Cout tplH. tpHL = (1.7 ns/pF) CL + 465 ns tplH. tpHL = (0.66 ns/pF) CL + 192 ns tplH. tpHL = (0.5 ns/pF) CL + 125 ns Clock Pulse Width	39 - C 0\6 - C 0\0 - C	tPHL tw(ci)	5.0 10 15 5.0 10	ropramoli Pulsa Generala	320 145 105 90 40	640 290 210 180 80	
PE to Cout tp_H, tp_H = (1.7 ns/pF) C_L + 465 ns tp_H, tp_H = (0.66 ns/pF) C_L + 192 ns tp_H, tp_H = (0.5 ns/pF) C_L + 125 ns Clock Pulse Width	39	^t PHL	5.0 10 15 5.0 10	Fulse Sulse Cemeratu	320 145 105 90 40 30	640 290 210 180 80 60	ns
PE to Cout tplH, tpHL = (1.7 ns/pF) CL + 465 ns tplH, tpHL = (0.66 ns/pF) CL + 192 ns tpLH, tpHL = (0.5 ns/pF) CL + 125 ns Clock Pulse Width	39	tPHL tw(ci)	5.0 10 15 5.0 10 15		320 145 105 90 40 30 4.0	640 290 210 180 80 60	ns
PE to Cout tpLH, tpHL = (1.7 ns/pF) CL + 465 ns tpLH, tpHL = (0.66 ns/pF) CL + 192 ns tpLH, tpHL = (0.5 ns/pF) CL + 125 ns Clock Pulse Width	34 <	tPHL tw(cl)	5.0 10 15 5.0 10 15 5.0 10	2.0	320 145 105 90 40 30 4.0 8.0	640 290 210 180 80 60	ns
PE to Cout tpLH, tpHL = (1.7 ns/pF) CL + 465 ns tpLH, tpHL = (0.66 ns/pF) CL + 192 ns tpLH, tpHL = (0.5 ns/pF) CL + 125 ns Clock Pulse Width Clock Pulse Frequency Preset Removal Time**	34 <	tPHL tw(ci)	5.0 10 15 5.0 10 15 5.0 10 15	 2.0 4.0 5.0	320 145 105 90 40 30 4.0 8.0	640 290 210 180 80 60	ns MHz
PE to Cout tpLH, tpHL = (1.7 ns/pF) CL + 465 ns tpLH, tpHL = (0.66 ns/pF) CL + 192 ns tpLH, tpHL = (0.5 ns/pF) CL + 125 ns Clock Pulse Width	34 <	tPHL tw(cl)	5.0 10 15 5.0 10 15 5.0 10 15 5.0	 2.0 4.0 5.0	320 145 105 90 40 30 4.0 8.0 10	640 290 210 180 80 60	ns MHz
PE to Cout tplH, tpHL = (1.7 ns/pF) CL + 465 ns tplH, tpHL = (0.66 ns/pF) CL + 192 ns tpLH, tpHL = (0.5 ns/pF) CL + 125 ns Clock Pulse Width Clock Pulse Frequency Preset Removal Time**	34 <	tPHL tW(cl) fcl trem	5.0 10 15 5.0 10 15 5.0 10 15 5.0 10 15	2.0 4.0 5.0	320 145 105 90 40 30 4.0 8.0 10 80 40 30	640 290 210 180 80 60 	ns MH2
PE to Cout tplH, tpHL = (1.7 ns/pF) CL + 465 ns tplH, tpHL = (0.66 ns/pF) CL + 192 ns tpLH, tpHL = (0.5 ns/pF) CL + 125 ns Clock Pulse Width Clock Pulse Frequency Preset Removal Time**	34 <	tpHL tw(cl) fcl trem tr(cl)	5.0 10 15 5.0 10 15 5.0 10 15 5.0 10	2.0 4.0 5.0	320 145 105 90 40 30 4.0 8.0 10	640 290 210 180 80 60 	ns MHz
PE to Cout tplH, tpHL = (1.7 ns/pF) CL + 465 ns tplH, tpHL = (0.66 ns/pF) CL + 192 ns tpLH, tpHL = (0.5 ns/pF) CL + 125 ns Clock Pulse Width	34 <	tPHL tW(cl) fcl trem	5.0 10 15 5.0 10 15 5.0 10 15 5.0 10 15 5.0 10 15	2.0 4.0 5.0	320 145 105 90 40 30 4.0 8.0 10 80 40 30	640 290 210 180 80 60 	ns MH2
PE to Cout IPLH. IPHL = (1.7 ns/pF) CL + 465 ns IPLH. IPHL = (0.66 ns/pF) CL + 192 ns IPLH. IPHL = (0.5 ns/pF) CL + 125 ns Clock Pulse Width Clock Pulse Frequency Preset Removal Time**	39 - C	tPHL tw(ci) fcl trem tr(ci) tf(ci)	5.0 10 15 5.0 10 15 5.0 10 15 5.0 10 15 5.0 10 15	2.0 4.0 5.0	320 145 105 90 40 30 4.0 8.0 10 80 40 30	640 290 210 180 80 60 	ns MH2
PE to Cout 1PLH. 1PHL = (1.7 ns/pF) CL + 465 ns 1PLH. 1PHL = (0.66 ns/pF) CL + 192 ns 1PLH. 1PHL = (0.5 ns/pF) CL + 125 ns Clock Pulse Width Clock Pulse Frequency Preset Removal Time Clock Rise and Fall Time	39 - C	tpHL tw(cl) fcl trem tr(cl)	5.0 10 15 5.0 10 15 5.0 10 15 5.0 10 15 5.0 10 15 5.0 10 15	2.0 4.0 5.0	320 145 105 90 40 30 4.0 8.0 10 80 40 30	640 290 210 180 80 60 	ns MH2 ns
PE to Cout IPLH. IPHL = (1.7 ns/pF) CL + 465 ns IPLH. IPHL = (0.66 ns/pF) CL + 192 ns IPLH. IPHL = (0.5 ns/pF) CL + 125 ns Clock Pulse Width Clock Pulse Frequency Preset Removal Time**	39 - C	tPHL tw(ci) fcl trem tr(ci) tf(ci)	5.0 10 15 5.0 10 15 5.0 10 15 5.0 10 15 5.0 10 15	2.0 4.0 5.0	320 145 105 90 40 30 4.0 8.0 10 80 40 30 	640 290 210 180 80 60 160 80 60 15 5	ns MH2 ns
PE to Cout tplH, tpHL = (1.7 ns/pF) CL + 465 ns tplH, tpHL = (0.66 ns/pF) CL + 192 ns tpLH, tpHL = (0.5 ns/pF) CL + 125 ns Clock Pulse Width Clock Pulse Frequency Preset Removal Time** Clock Rise and Fall Time	39 - C	tPHL tw(ci) fcl trem tr(ci) tf(ci)	5.0 10 15 5.0 10 15 5.0 10 15 5.0 10 15 5.0 10 15 5.0 10 15 5.0 10 15 15 15 10 10 10 10 10 10 10 10 10 10 10 10 10	2.0 4.0 5.0	320 145 105 90 40 30 4.0 8.0 10 80 40 30 	640 290 210 180 80 60 160 80 60 15 5 4	ns MHz
PE to Cout tpLH, tpHL = (1.7 ns/pF) CL + 465 ns tpLH, tpHL = (0.66 ns/pF) CL + 192 ns tpLH, tpHL = (0.5 ns/pF) CL + 125 ns Clock Pulse Width Clock Pulse Frequency Preset Removal Time Clock Rise and Fall Time	39 - C	tPHL tw(ci) fcl trem tr(ci) tf(ci)	5.0 10 15 5.0 10 15 5.0 10 15 5.0 10 15 5.0 10 15 5.0 10 15 5.0 10 15 5.0 10 15 5.0 10 15 15 15 15 15 15 15 15 15 15 15 15 15	2.0 4.0 5.0 	320 145 105 90 40 30 4.0 8.0 10 80 40 30 	640 290 210 180 80 60 	ns MH2 ns
PE to Cout tpLH, tpHL = (1.7 ns/pF) CL + 465 ns tpLH, tpHL = (0.66 ns/pF) CL + 192 ns tpLH, tpHL = (0.5 ns/pF) CL + 125 ns Clock Pulse Width Clock Pulse Frequency Preset Removal Time Clock Rise and Fall Time	39 000 000 000 000 000 000 000 000 000 0	tPHL tw(ci) fcl trem tr(ci) tf(ci)	5.0 10 15 5.0 10 15 5.0 10 15 5.0 10 15 5.0 10 15 5.0 10 15 5.0 10 15 5.0 10 15 15 15 15 15 16 16 16 16 16 16 16 16 16 16 16 16 16	2.0 4.0 5.0 	320 145 105 90 40 30 4.0 8.0 10 80 40 30 	640 290 210 180 80 60 160 80 60 15 5 4	ns MHz
PE to Cout tpLH, tpHL = (1.7 ns/pF) CL + 465 ns tpLH, tpHL = (0.66 ns/pF) CL + 192 ns tpLH, tpHL = (0.5 ns/pF) CL + 125 ns Clock Pulse Width Clock Pulse Frequency Preset Removal Time Clock Rise and Fall Time	39 000 000 000 000 000 000 000 000 000 0	tPHL tw(ci) fcl trem tr(ci) tf(ci)	5.0 10 15 5.0 10 15 5.0 10 15 5.0 10 15 5.0 10 15 5.0 10 15 5.0 10 15 5.0 10 15 5.0 10 15 15 15 15 15 15 15 15 15 15 15 15 15	2.0 4.0 5.0 	320 145 105 90 40 30 4.0 8.0 10 80 40 30 	640 290 210 180 80 60 	ns MHz
PE to Cout tpLH, tpHL = (1.7 ns/pF) CL + 465 ns tpLH, tpHL = (0.66 ns/pF) CL + 192 ns tpLH, tpHL = (0.5 ns/pF) CL + 125 ns Clock Pulse Width Clock Pulse Frequency Preset Removal Time Clock Rise and Fall Time Clock Rise and Fall Time	39 000 000 000 000 000 000 000 000 000 0	tPHL tw(ci) fcl trem tr(ci) tf(ci)	5.0 10 15 5.0 10 15 5.0 10 15 5.0 10 15 5.0 10 15 5.0 10 15 5.0 10 15 5.0 10 15 15 10 10 15 10 10 10 10 10 10 10 10 10 10 10 10 10	2.0 4.0 5.0 	320 145 105 90 40 30 4.0 8.0 10 80 40 30 	640 290 210 180 80 60 	ns MHz
PE to Cout IPLH. IPHL = (1.7 ns/pF) CL + 465 ns IPLH. IPHL = (0.66 ns/pF) CL + 192 ns IPLH. IPHL = (0.5 ns/pF) CL + 125 ns Clock Pulse Width Clock Pulse Frequency Preset Removal Time Clock Rise and Fall Time Carry In Setup Time Binary/Decade Setup Time	39 000 000 000 000 000 000 000 000 000 0	tPHL tw(ci) fcl trem tr(ci) tf(ci)	5.0 10 15 5.0 10 15 5.0 10 15 5.0 10 15 5.0 10 15 5.0 10 15 5.0 10 15 5.0 10 15 5.0 10 15 5.0 10 10 10 10 10 10 10 10 10 10 10 10 10	2.0 4.0 5.0 5.0 150 60 40 340 140 100 320	320 145 105 90 40 30 4.0 8.0 10 80 40 30 	640 290 210 180 80 60 	ns MH2 ns ns ns
PE to Cout tpLH. tpHL = (1.7 ns/pF) CL + 465 ns tpLH. tpHL = (0.66 ns/pF) CL + 192 ns tpLH. tpHL = (0.5 ns/pF) CL + 125 ns Clock Pulse Width Clock Pulse Frequency Preset Removal Time Clock Rise and Fall Time Dp/Down Setup Time	39 000 000 000 000 000 000 000 000 000 0	tPHL tw(ci) fcl trem tr(ci) tf(ci)	5.0 10 15 5.0 10 15 5.0 10 15 5.0 10 15 5.0 10 15 5.0 10 15 5.0 10 15 5.0 10 15 15 10 10 15 10 10 10 10 10 10 10 10 10 10 10 10 10	2.0 4.0 5.0 	320 145 105 90 40 30 4.0 8.0 10 80 40 30 	640 290 210 180 80 60 160 80 60 15 5 4	ns MH2 ns ns ns
PE to Cout IPLH. IPHL = (1.7 ns/pF) CL + 465 ns IPLH. IPHL = (0.66 ns/pF) CL + 192 ns IPLH. IPHL = (0.5 ns/pF) CL + 125 ns Clock Pulse Width Clock Pulse Frequency Preset Removal Time Clock Rise and Fall Time Dp/Down Setup Time Binary/Decade Setup Time	39 000 000 000 000 000 000 000 000 000 0	tPHL tW(ci) fcl trem tr(ci) tf(ci)	5.0 10 15 5.0 10 15 5.0 10 15 5.0 10 15 5.0 10 15 5.0 10 15 5.0 10 15 5.0 10 15 5.0 10 15 5.0 10 10 10 10 10 10 10 10 10 10 10 10 10	2.0 4.0 5.0 5.0 150 60 40 340 140 100 320	320 145 105 90 40 30 4.0 8.0 10 80 40 30 	640 290 210 180 80 60 160 80 60 15 5 4	ns MH2 ns ns ns
PE to Cout IPLH. IPHL = (1.7 ns/pF) CL + 465 ns IPLH. IPHL = (0.66 ns/pF) CL + 192 ns IPLH. IPHL = (0.5 ns/pF) CL + 125 ns Clock Pulse Width Clock Pulse Frequency Preset Removal Time Carry In Setup Time Up/Down Setup Time Binary/Decade Setup Time	39 000 000 000 000 000 000 000 000 000 0	tPHL tw(ci) fcl trem tr(ci) tf(ci)	5.0 10 15 5.0 10 15 5.0 10 15 5.0 10 15 5.0 10 15 5.0 10 15 5.0 10 15 5.0 10 15 5.0 10 10 15 10 10 10 10 10 10 10 10 10 10 10 10 10	2.0 4.0 5.0 5.0 150 60 40 340 140 100	320 145 105 90 40 30 4.0 8.0 10 80 40 30 	640 290 210 180 80 60 	ns MHz

^{*}The formulae given are for the typical characteristics only.

**The Preset Signal must be low prior to a positive-going transition of the clock.





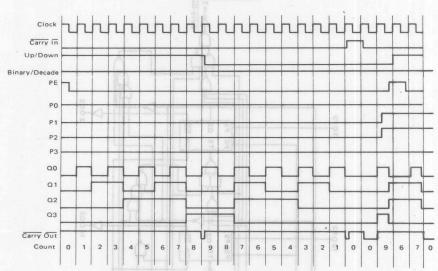
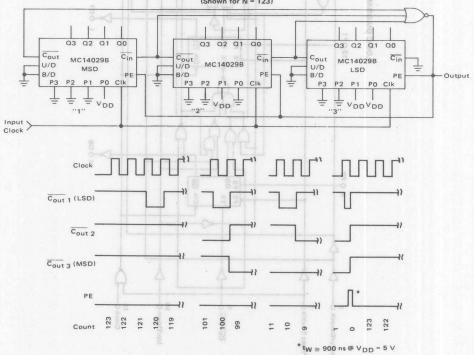
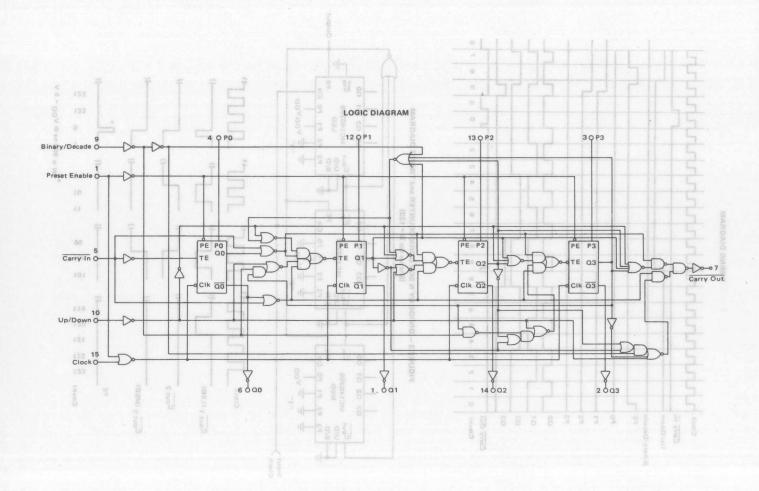


FIGURE 3 — DIVIDE BY N BCD DOWN COUNTER and TIMING DIAGRAM (Shown for N = 123)





3-96

MC1405ag

TRIPLE SERIAL ADDERS

The MC14032B and MC14038B triple serial adders have the clock and carry reset inputs common to all three adders. The carry is added on the positive-going clock transition for the MC14032B, and on the negative-going clock transition for the MC14038B. Typical applications include serial arithmetic units, digital correlators, digital servo control systems, datalink computers, and flight control computers.

- Static Operation from dc to 5.0 MHz
- Buffered Outputs
- Single-Phase Clocking
- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range.
- Pin-for-Pin Replacement for CD4032B and CD4038B

MAXIMUM RATINGS (Voltages referenced to VSS)

Rating		ac c.	Symbol	Value	Unit
DC Supply Voltage	-	8.8-	VDD	-0.5 to +18	Vdc
Input Voltage, All Inputs	-	88.0	Vin.0	-0.5 to V _{DD} + 0.5	Vdc
DC Current Drain per Pin	-	2.25	11.1	10	mAdo
Operating Temperature Range AL CL/CP			TA	-55 to +125 -40 to +85	°C
Storage Temperature Range	0 =	10000	T _{stg}	-65 to +150	оС

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that Vin and Vout be constrained to the range VSS < (Vin or Vout) < VDD.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD).

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

TRIPLE SERIAL ADDERS

Positive Logic - MC14032B Negative Logic - MC14038B

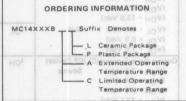


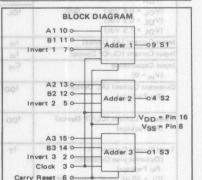
L SUFFIX

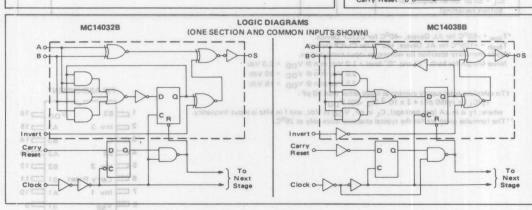
P SUFFIX CERAMIC PACKAGE PLASTIC PACKAGE

CASE 620

CASE 648







ELECTRICAL CHARACTERISTICS

1214 20143		VDD	Tio	w*		25°C		Th	igh *	
Characteristic	Symbol	Vdc	Min	Max	Min	Тур	Max	Min	Max	Unit
Output Voltage "0" Level	VOL	5.0	-	0.05	-	0	0.05		0.05	Vdc
V _{in} = V _{DD} or 0		10	-	0.05	-	0	0.05	-	0.05	-
		15	-	0.05	DODER	0	0.05	RT-	0.05	
SCEOLEDM - New "1" Level	VOH	5.0	4.95	riers -i nau	4.95	5.0	MGH40	4.95	e thiche	Vdc
V _{in} = 0 or V _{DD}	011	10	9.95	IT mobile	9.95	10	COTTON I	9.95	est Vites	bris
		15	14.95	10 O to 10 o al	14.95	15	de Feire	14.95	mele Tron la	plalae
nput Voltage# "0" Level	VIL		pigyT .8	REDITOR	A edit w	k mislejami	at Manda	enion-sy	itanah as	Vdc
(VO = 4.5 or 0.5 Vdc)		5.0	ors, Chaire	1.5	eriolis a	2.25	1.5	e spolas	1.5	1
(VO = 9.0 or 1.0 Vdc)	S700	10		3.0		4.50	3.0	-	3.0	logs
(V _O = 13.5 or 1.5 Vdc)	1000 F	15	dutugo 11	4.0	,enstu	6.75	4.0	eveter	4.0	5.A.185
"1" Level	VIH									moo
(VO = 0.5 or 4.5 Vdc)	100	5.0	3.5		3.5	2.75	or ab re	35	atic Dps	Vdc
(V _O = 1.0 or 9.0 Vdc)		10	7.0	_	7.0	5.50	_	7.0		
(V _O = 1.5 or 13.5 Vdc)		15	11.0	_	11.0	8.25	_	11.0	O benefit.	43 W
Output Drive Current (AL Device)	A.D. 22		11.0		11.0	0.20	121	Madia d	Bert 9-Mari	mAdc
(V _{OH} = 2.5 Vdc) Source	ОН	5.0	-3.0	5 V de	-2.4	-4.2	5.0-nA.	-1.7	triondelli	IIIAGC
(VOH = 4.6 Vdc)		5.0	-0.64	100	-0.51	-0.88		-0.36		
(V _{OH} = 9.5 Vdc)		10	-1.6		-1.3	-2.25	ge = 3.0	-0.36	oV ylagu	8 8
(VOH = 13.5 Vdc)		15	-4.2	sniD at	-3.4	-8.8	Two_Lo	-2.4	to alduos	0 8
0				10/12/10/10		-	0W_ 10	-	LANGE OF THE PARTY	
(V _{OL} = 0.4 Vdc) Sink	IOL	5.0	0.64		0.51	0.88	0312 10	0.36	re Range	mAdc
(V _{OL} = 0.5 Vdc)		10	1.6	. T	1.3	2.25	-	0.9		
(V _{OL} = 1.5 Vdc)		15	4.2	.65604	3.4	8.8	nent los	2.4	nifqTetin	9.0
Output Drive Current (CL/CP Device)	ІОН		-				-			mAdc
(V _{OH} = 2.5 Vdc) Source		5.0	-2.5	-	-2.1	-4.2	nelen zepe	-1.7	MITARIA	UMIX
(V _{OH} = 4.6 Vdc)		5.0	-0.52	11432	-0.44	-0.88	-	-0.36	-	-
(V _{OH} = 9.5 Vdc)		10	-1.3	HEN TO THE REAL PROPERTY.	-1.1	-2.25	-	-0.9	-	-
(V _{OH} = 13.5 Vdc)		15	-3.6	01 (240)-	-3.0	-8.8	-	-2.4	6 - 10(0)	yluqui
(VOL = 0.4 Vdc) Sink	IOL	5.0	0.52	3V # 8.0	0.44	0.88	-	0.36	gnF-4A , s	mAdc
(VOL = 0.5 Vdc)		10	1.3	01 -	1.1	2.25	-	0.9	rest TrianC	Current
(VOL = 1.5 Vdc)		15	3.6	nt 28-	3.0	8.8	NIGHT LA	2.4	SUITE SOPRE	- noise
nput Current (AL Device)	lin	15	- 284	± 0.1	-	±0.00001	±0.1	10 -	±1.0	μAdc
nput Current (CL/CP Device)	lin	15	-087	± 0.3	1 - 1	±0.00001	±0.3	-	±1.0	μAdc
nput Capacitance	Cin	-	001	OT DU	- QTa	5.0	7.5		5 8 FU119 UU	pF
(Vin = 0)	cin			_		5.0	7.5			pr
Quiescent Current (AL Device)		F.0	-	5.0		0.005	F.0			0.4
(Per Package)	IDD	5.0	-	5.0	-	0.005	5.0	-	150	μAdc
(Fer Fackage)	10	15	due to fil	10	legs etus	0.010	10 20	ins circu	300	This d
		- 01	innitions or	N. Latinitism 1	ariz Early	10. 35. 31. 310.H		It aistaelu	600	Links
Quiescent Current (CL/CP Device)	IDD	5.0	egazitov br	20	am n oris	0.005	20	nol re ella	150	μAdc
(Per Package)		10	ni V-hartr	40	point 4 11 1	0.010	40	Blubels 65	300	this his
A2 15 0		15	-	80	- HUD!	0.015	80	ed to the	600	d moV
Total Supply Current**†	I _T	5.0	al level or	periov sigo	IT = (0	.96 μA/kHz	f + Ipp			μAdc
(Dynamic plus Quiescent,	12	10			IT = (1	.93 μA/kHz	f+ IDD			narizia
Per Package)		15				.8 μA/kHz)				100
(C _L = 50 pF on all outputs, all	Carry		-							LUBS.
buffers switching)	personal language								to the class and a second	

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.

T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Noise immunity specified for worst-case input combination. Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc 2.0 Vdc min @ VDD = 10 Vdc 2.5 Vdc min @ VDD = 15 Vdc To calculate total supply current at loads other than 50 pF:

I_T(C_L) = I_T(50 pF) + 3 x 10⁻³ (C_L -50) V_{DD}

where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.

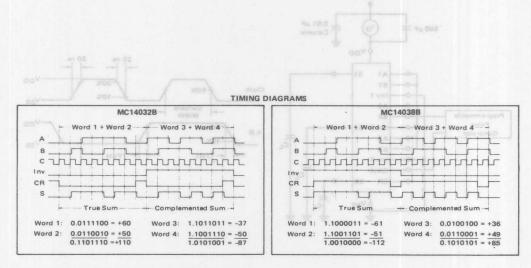
*The formulas given are for the typical characteristics only at 25°C.

PIN ASSIGNMENT 1 ____ S3 VDD 16 2 - Inv 3 A3 15 3 C B3 14 4 S2 A2 13 Inv 2 B2 ___12 B1 -11 Carry Reset 7 = A1 10 Inv 1 8 T VSS SI **□**9

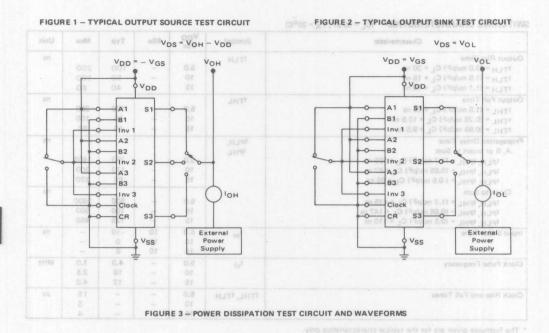
SWITCHING CHARACTERISTICS* (CL = 50 pF, TA = 25°C)

JOV = SOV Characteristic	Symbol	V _{DD} Vdc	Min	Тур	Max	Unit		
Output Rise Time	tTLH		aav -	Vene		ns		
tTLH = (3.0 ns/pF) CL + 30 ns	HU HU	5.0	957	100	200			
tTLH = (1.5 ns/pF) CL + 15 ns		10	-	50	100			
t _{TLH} = (1.1 ns/pF) C _L + 10 ns		15	eoW)	40	80			
Output Fall Time	tTHL		1			ns		
t _{THL} = (1.5 ns/pF) C _L + 25 ns		5.0	43	100	200	-		
t _{THL} = (0.75 ns/pF) C _L + 12.5 ns		10	-	50	100			
t _{THL} = (0.55 ns/pF) C _L + 9.5 ns		15	+	40	80			
Propagation Delay Time	tPLH,			84	0-1-1	ns		
A, B or Invert to Sum	tPHL			58	0-4			
tplH, tpHL = (1.7 ns/pF) CL + 195 ns	1	5.0		280	1400	-		
tplH, tpHL = (0.66 ns/pF) CL + 87 ns		10	-	120	300	9		
tpLH, tpHL = (0.5 ns/pF) CL + 65 ns		15	+	90	230			
Clock to Sum	HO!			t was		ns		
tpLH, tpHL = (1.7 ns/pF) CL + 415 ns		5.0	-	500	2400			
tpLH, tpHL = (0.66 ns/pF) CL + 147 ns		10	1	180	600			
tpLH, tpHL = (0.5 ns/pF) CL + 110 ns		15	108	135	450			
nput Setup Time	t _{su} lesses	5.0	10	-10	_	ns		
O Vess	18WO	10	10	0	-			
	hjdun	15	10	0	-			
Clock Pulse Frequency	fcl	5.0	-	4.0	1.0	MHz		
		10	-	10	2.5			
		15	-	12	4.0			
Clock Rise and Fall Times	tTHL, tTLH	5.0	-	-	15	μs		
		10	-	-	5			
N TEST CIRCUIT AND WAVEFORMS	NER DISSIPATIO	15	PLEURI	-	4			

^{*} The formulae given are for the typical characteristics only.



Note: Unused input pins must be connected to either $V_{\mbox{DD}}$ or $V_{\mbox{SS}}$.



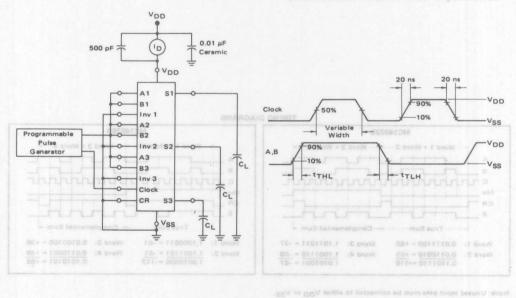
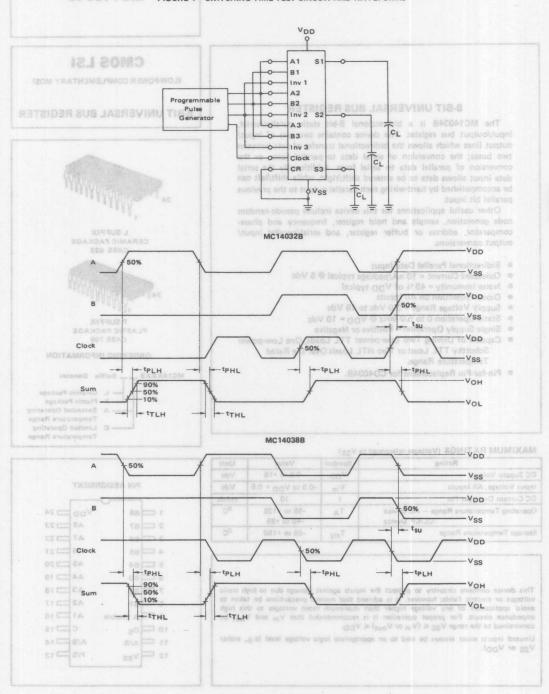


FIGURE 4 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS





MC14034B

HOTAUEZ BANNUT 4038B

CMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

8-BIT UNIVERSAL BUS REGISTER

8-BIT UNIVERSAL BUS REGISTER

The MC14034B is a bidirectional 8-bit static parallel/serial, input/output bus register. The device contains two sets of input/output lines which allows the bidirectional transfer of data between two buses; the conversion of serial data to parallel form, or the conversion of parallel data to serial form. Additionally the serial data input allows data to be entered shift/right, while shift/left can be accompolished by hard-wiring each parallel output to the previous parallel bit input.

Other useful applications for this device include pseudo-random code generation, sample and hold register, frequency and phase-comparator, address or buffer register, and serial/parallel input/output conversions.

- Bidirectional Parallel Data Input
- Quiescent Current = 10 nA/package typical @ 5 Vdc
- Noise Immunity = 45 % of VDD typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Static Operation 0 to 5.0 MHz @ VDD = 10 Vdc
- Single Supply Operation = Positive or Negative
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range.
- Pin-for-Pin Replacement for CD4034B.

L SUFFIX
CERAMIC PACKAGE
CASE 623

P SUFFIX
PLASTIC PACKAGE
CASE 709
ORDERING INFORMATION

MC14XXXB
Suffix Denotes

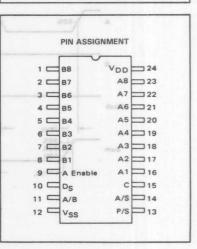
L Ceramic Package
P Plastic Package
P Plastic Package
C Limited Operating
Temperature Range
C Limited Operating
Temperature Range
C Limited Operating

MAXIMUM RATINGS (Voltages referenced to VSS)

Rating	Symbol	Value	Unit
DC Supply Voltage	V _{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	Vin	-0.5 to V _{DD} + 0.5	Vdc
DC Current Drain per Pin	1	10	mAdo
Operating Temperature Range AL Device CL/CP Device	TA	-55 to +125 -40 to +85	°C
Storage Temperature Range	T _{stg}	-65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedence circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).



ELECTRICAL CHARACTERISTICS

	weld		6886	ogV	VDD	T	ow*		25°C	suranudii	Th	igh*	
	Character	ristic	1000	Symbol	Vdc	Min	Max	Min	Тур	Max	Min	Max	Unit
Output Vo	oltage)" Level	VOL	5.0	-	0.05	-	0	0.05	<u>0</u> 10 A	0.05	Vdd
Vin =	VDD or 0			0.0	10	-	0.05	-	0	0.05	+ 75 (34	0.05	ILLI I
				01	15	-	0.05	-	0	0.05	1 75 (40	0.05	NAT?
	130	68 ,,,	l" Level	VOH	5.0	4.95	_	4.95	5.0	20.01	4.95		Vdd
Vin =	0 or VDD				10	9.95	-	9.95	10	-	9.95	all Time	India
		100		0.8	15	14.95	-	14.95	15	25 ns	14.95	= (1.5 ns	HYT
Input Volt	tage#	0.5	"0" Level	VIL						no 8 10	raff) Ci	23 M	Vdd
(Vo =	4.5 or 0.5 Vo	dc)	-	- 01	5.0		1.5	-	2.25	1.5	-	1.5	HIP
	9.0 or 1.0 Vo				10	-	3.0	-	4.50	3.0	BMILL	3.0	181 A
(V _O =	13.5 or 1.5 \	(dc)			15	-	4.0	-	6.75	4.0	Sus Foreil	4.0	ar C
	20801	aca.	"1" Level	VIH	2110				26	10 + 100	Bolon C.	l = THat	Los
	0.5 or 4.5 Vo			01	5.0	3.5	-	3.5	2.75	11 - 10 0	3.5	= THat	Vdc
-	1.0 or 9.0 Vo		1 2 1	ar	10	7.0	-	7.0	5.50	191 T 19	7.0	1 ° 19197	191
	1.5 or 13.5 \				15	11.0	-	11.0	8.25	-	11.0		
	rive Current (100000	IOH	54.10				3000	I ntsG let	nnos Fara	Asynchro	mAd
	= 2.5 Vdc)	So	urce		5.0	-1.2	-	-1.0	-1.7	-	-0.7	Parallel D	1 A 1 B
	= 4.6 Vdc)	808	1 - 1	6.0	5.0	-0.25	-	-0.2	-0.36	C) + 420	-0.14	1 4 11492	1_103
	= 9.5 Vdc)		-	10	10 15	-0.62	-	-0.5	-0.9 -3.5	11+101	-0.35 -1.1	1 = 11492	Total .
	= 13.5 Vdc)	130	- 1	- 09		-1.8	-	-1.5	-	101 - 10	The state of the state of	2019	-
	= 0.4 Vdc)	Sin	OSE	OL	5.0	0.64	-	0.51	0.88	-	0.36	right Wildth	mAd
	= 0.5 Vdc)		140	10	10	1.6	-	1.3	2.25	-	0.9	-	
	= 1.5 Vdc)	21.100	Ditt	ar I	15	4.2	-	3.4	8.8	-	2.4		-
	rive Current (10Н	14						Voit	tupun Freque	mAd
	= 2.5 Vdc)	0.0	ource	01	5.0	-1.0	-	-0.8	-1.7	-	-0.6	-	
	= 4.6 Vdc)			15	5.0	-0.2 -0.5	-	-0.16	-0.36 -0.9	-	-0.12 -0.3	_	
	= 9.5 Vdc) = 13.5 Vdc)			0.a	15	-1.4		-1.2	-3.5	_	-1.0	100 Files	F. Nacel
		Sir	1	,01	5.0	0.52	-	0.44	0.88		0.36	-	- 0.1
	= 0.4 Vdc) = 0.5 Vdc)	211	nk	IOL	10	1.3	-	1.1	2.25	-	0.36		mAd
	= 1.5 Vdc)		100	6.0	15	3.6		3.0	8.8	-	2.4	f gots8 h	ani 8
	rent (AL Dev	lasi	- 69	12	15	-	±0.1		±0.00001	'±0.1	-	±1.0	μAdo
		-	35	lin		-		-			-		-
-	rent (CL/CP)	Device	008	lin	15	-	± 0.3	-	±0.00001	± 0.3	A 18 Buts	±1.0	μAdd
Input Capa (V _{in} =		90	270	Cin			-	-	5.0	7.5	-	-	pF
	Current (AL	Device	9)	IDD	5.0	- "	5.0	no editori	0.010	5.0	sol are n	150	μAde
(Per Pa	ickage)				10	-	10	no solitar	0.020	10		300	DI BIL
					15		20	-	0.030	20	-	600	
Quiescent	Current (CL.	CP De	vice)	IDD	5.0	-	50	-	0.010	50	-	375	μAd
(Per Pa	ackage)			17.77	10	-	100	-	0.020	100	-	750	
					15	-	200	-	0.030	200	-	1500	
Total Supp	ply Current*	*†		IT	5.0	5.1867	HTURT	IT =	(2.2 µA/kHz) f + Ipp			μAd
	mic plus Quie	scent,	-		10				4.4 µA/kH2				1
	ackage)			THOITA	15			1T = 1	6.6 µA/kHz	f + IDD	A/B S/		A
	50 pF on all (rs switching)	output	s, all	erab foliave	A and B p	svoni aze	es Serial da	nehrener nehrener	Serial Sy	1 1	0 0	0	
3-State O	utput Leakag evice)	e Curre	ent [†] etugtug eb etugtug	TTE lella	15	ni <u>s</u> tab la lai d <u>u</u> a l	±0.1	Synunio Asynghia	±0.0001	±0.1	0_ 1	±3.0	μAdc
3-State O	utput Leakag	e Curr	ent	ITL	15	,bardssn	±1.0	instanting to	±0.0001	±1.0		±7.5	μAdc
(CL/C	P Device)				Tellerock A	Eugeni un	in labour su	constant	S Jaivo S	1 x	0 0	1	1

^{*}Tlow = -55°C for AL Device, -40°C for CL/CP Device.

Thigh = +125°C for AL Device, +85°C for CL/CP Device.

#Noise immunity specified for worst-case input combination.

Noise Margin for both "1" and "0" level =

1.0 Vdc min @ VDD = 5.0 Vdc

2.0 Vdc min @ VDD = 10 Vdc

^{2.5} Vdc min @ VDD = 15 Vdc and allowed in the serial mode and when the A/S input is how in the PD standard into the provence of the provence o

SWITCHING	CHARACTERISTICS*	$(C_1 = 50 p)$	F, TA = 25°C)

		aracteri	istic		Tions	Symbol	VDD	Min	Тур	Max	Unit
tick) tubil	nith	zuM	BUT	niM	No.DE	ANN I SHA	SUCCESSION OF STREET		311211971	0.1901/	
Output Rise Time A						tTLH a	5.0	Level .	180	360	N. 18 district
tTLH = (3.0 ns/pl						- 01	10		90	180	
tTLH = (1.5 ns/pl						- ar	15		65	130	
tTLH = (1.1 ns/pl		ns	0.2	30.8		NA 1 08	15	love 1 "	00		
Output Fall Time A						THL			400	200	ns
tTHL = (1.5 ns/pl						en land	5.0	-	100		
tTHL = (0.75 ns/)							10	level "0"	50	100	
tTHL = (0.55 ns/	oF) CL +9	.5 ns	20.00		3.5	0.0	15	-	40	80	
Propagation Delay Ti	me	0.5	08.6			101	-		tabV	9.0 or 1.0	
A (B) Synchronoi	us Paralles	Data In	put,			tPLH,				13.5 or 1	ns
B (A) Parallel Dat	ta Output					tPHL	MAN	level "I"			= 0V) = 0V)
tPLH, tPHL = (1.	7 ns/pF) C	L + 440) ns			5.0 3.6	5.0 -	-	525	1050	
tpHI tpHI = (0.	66 ns/pF)	CL + 17	72 ns			10 7.0		10		205	
tPLH, tPHL = (0.	5 ns/pF) C	L + 120) ns			1 31	15	-	145	290	
Propagation Delay T								(no)	esci Lali	ive Curren	G tuentio
A (B) Asynchron	ous Paralle	Data I	nput			tPLH,	HO	1001		= 2.5 Vdc	ns HO
B (A) Parallel Dat	ta Output					tPHL		1		abV B.b.s	
tPLH, tPHL = (1.	7 ns/pF) C	+ 420	0 ns			10 -0.82	5.0	-	505	1010	HOA!
tpLH, tpHL = (0.	66 ns/pF)	Ci + 14	47 ns			15 -1.8	10		180	360	
tPLH tPHL = (0.	5 ns/pF) C	+ 10	5 ns			100	15	-	130	260	140,540
Clock Pulse Width	26.0	-		18.0		Danis.	5.0	340	170	0.5 VdcI	ns
				1.3			10	140	70	- 1.5 Vdc	10.A1
			8.8	3.6		15 4.2	15	110	- 55	30 V 0.1	TOAL
Clock Pulse Esecuen	ov.					f.,	5.0	(BOLVAC	2.5	1.2	MHz
Clock Pulse Frequen				8.0-	- 1	fcl 0.8	10	631	6.0	3.0	HON
						5.0 -0.2	15	-	8.0	4.0	HO VI
Clock Pulse Rise	-0.3		8.6-	-1.2		tTLH, THL	5.0	1 -	- /	15	μs
							10	-	-	5	100000
						5.0 0.52	15	- 1	Sid	4	10/A
A, B Input Setup Tir	0.0		2.98		-	-	5.0	100	35	inbarra 1	ns
A, B input setup ili	2.011					t _{su} at	10	45	15		1000
						- 81	15	35	12	3 JAI tre	pus Cui
High Level SE, P/S,	A /C Dules I	Nidth	100000.01	-	0.04	twH	5.0	600	200	PETO) Ind	ns
riigii Level SE, P/S,	A/3 ruise v	WIGHT.				WH	10	270	90	scitance	pur Cap
							15	200	80	_ 10	- niVi
						The state of the second second	10	200		_	

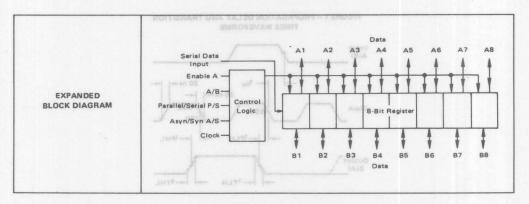
*The formulae given are for the typical characteristics only.

TRUTH TABLE

	OPERATION	(y = y)	MODE	A/S	A/B	P/S	"A" Enable
utputs disabled.	nput, A and B parallel data outp	Synchronous Serial data	Serial	×	0	0	0
	nput, B-Parallel data output.	Synchronous Serial data	Serial	X	1	0	0
puts disabled.	ita inputs, A-Parallel data outpu	B Synchronous Parallel	Parallel	0	0	1	0
tputs disabled.	lata inputs, A-Parallel data outp	B Asynchronous Parallel	Parallel	1	0	1	0
ramon'S angulas I turntu	oled, B-Parallel data outputs.	A-Parallel data inputs dis	Parallel	0	1	1	0
P Chaulen)	oled, B-Parallel data outputs.	A-Parallel data inputs dis	Parallel	1	1	1	0
	put, A-Parallel data output.	Synchronous serial data	Serial	×	0	0	1
	put, B-Parallel data output.	Synchronous serial data	Serial	X	1	0	1
out.	ita input, A-Parallel data output	B-Synchronous Parallel	Parallel	0	0	1	-1
tput.	data input, A-Parallel data outpu	B-Asynchronous Paralle	Parallel	1	0	1	1
outen her "I" standard nor	ata input, B-Parallel data output	A-Synchronous Parallel	Parallel	0	001	1	1
tputay 0.8 = naV 9 nim s	data input, B-Parallel data outpu	A-Asynchronous Paralle	Parallel	.1	. 1	1	1

X = Don't Care

†Outputs change at positive transition of clock in the serial mode and when the A/S input is low in the parallel mode. V and the serial mode and when the A/S input is low in the parallel mode. During transfer from parallel to serial operation, A/S should remain low in order to prevent D_S transfer into flip-flops.



OPERATING CHARACTERISTICS

The MC14034B is composed of eight register cells connected in cascade with additional control logic. Each register cell is composed of one "D" master-slave flip-flop with separate internal clocks, and two data transfer gates allowing the data to be transferred bidirectionally from bus A to bus B and from bus B to bus A, and to be memorized. Besides the single phase clock and the serial data inputs, the control logic provides four other features:

A Enable Input — When high, this input enables the bus A data lines.

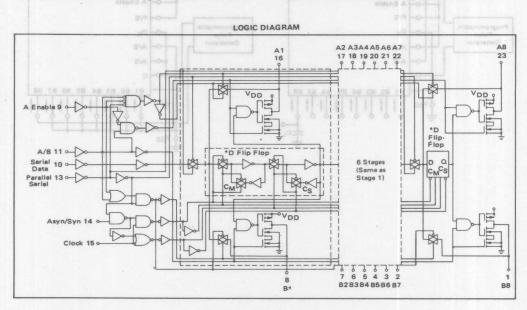
A/B Input (Data A or B) - This input controls the direction of data flow: when high, the data flows from

bus A to bus B; when low, the data flows from bus B to bus A.

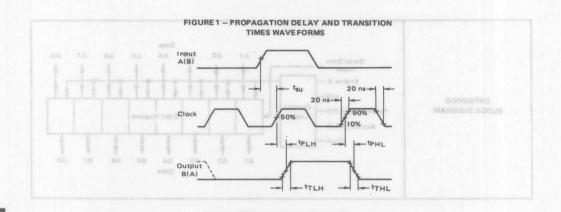
P/S Input (Parallel/Serial) — This input controls the data input mode (parallel or serial). When high, the data is transferred to the register in a parallel asynchronous mode or a parallel synchronous mode (positive clock transition). When low, the data is entered into the register in a serial synchronous mode (positive clock transition).

A/S Input (Asynchronous/Synchronous to the Clock)

When this input is high, the data is transferred independently from the clock rate; when low, the clock is enabled and the data is transferred synchronously.







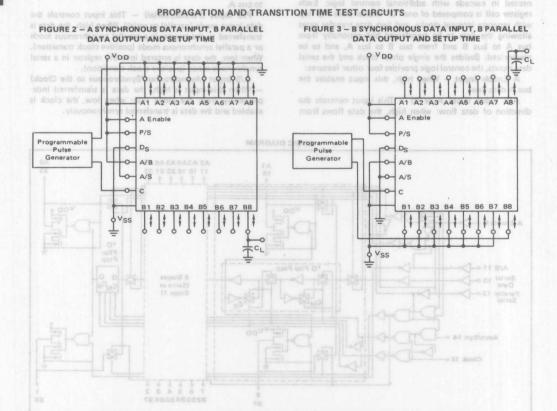


FIGURE 4 - POWER DISSIPATION TEST CIRCUIT AND WAVEFORMS

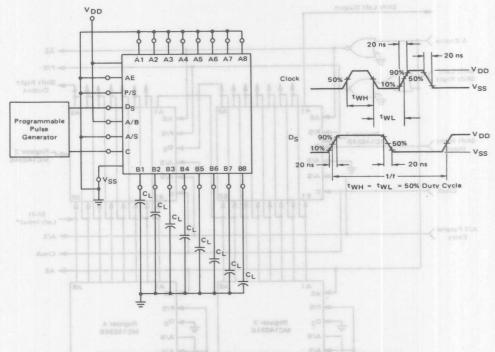
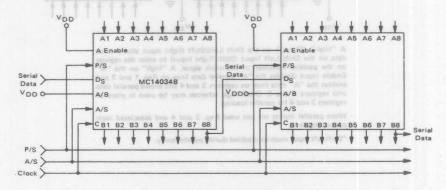
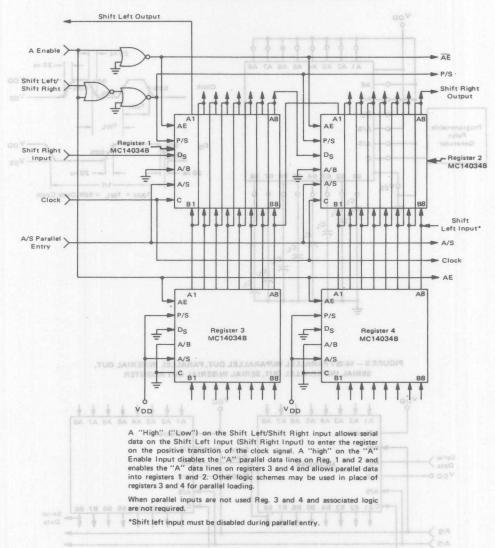


FIGURE 5 – 16-BIT PARALLEL IN/PARALLEL OUT, PARALLEL IN/SERIAL OUT, SERIAL IN/PARALLEL OUT, SERIAL IN/SERIAL OUT REGISTER







4-BIT PARALLEL-IN/PARALLEL-OUT SHIFT REGISTER

The MC14035B 4-bit shift register is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. It consists of a 4-stage clocked serial-shift register with synchronous parallel inputs and buffered parallel outputs. The Parallel/Serial (P/S) input allows serial-right shifting of data or synchronous parallel loading via inputs Dp0 thru Dp3. The True/Complement (T/C) input determines whether the outputs display the Q or Q outputs of the flip-flop stages. J-K logic forms the serial input to the first stage. With the J and K inputs connected together they operate as a serial "D" input.

This device may be effectively used for shift-right/shift-left registers, parallel-to-serial/serial-to-parallel conversion, sequence generation, up/down Johnson or ring counters, pseudo-random code generation, frequency and phase comparators, sample and hold registers, etc.

- 4-Stage Clocked Serial-Shift Operation
- Synchronous Parallel Loading of all Four Stages
- J-K Serial Inputs on First Stage
- Asynchronous True/Complement Control of all Outputs
- Fully Static Operation
- Asynchronous Master Reset
- Data Transfer Occurs on the Positive-Going Clock Transition
- No Limit on Clock Rise and Fall Times
- All Inputs are Buffered
- 6.0 MHz Operation @ VDD = 10 Vdc
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range

MAXIMUM RATINGS (Voltages referenced to VSS)

Rating	Symbol	Value	Unit
DC Supply Voltage	VDD	-0.5 to +18	Vdc
Input Voltage, All Inputs	Vin	-0.5 to V _{DD} + 0.5	Vdc
DC Current Drain per Pin	1	10	mAdc
Operating Temperature Range - AL Device CL/CP Device	TA	-55 to +125 -40 to +85	°C
Storage Temperature Range	T _{stg}	-65 to +150	°C

TRUTH TABLE

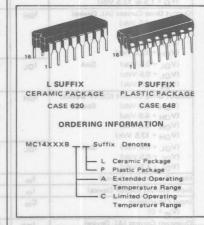
	INP	UTS		tn OUTPUT
С	J	K	R	QO
	0	0	0	oil pin Ole no s
1	0	d alkis d	0	Q0 (n - 1)
_	111	10 0 V	0	Q0 (n - 1)
	1	1	0	1
7	×	×	0	Q0:(n-1)
×	×	×	1	0

x = Don't Care
P/S = 0 = Serial Mode
T/C = 1 = True Outputs

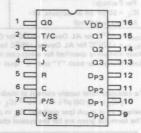
CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

4-BIT
PARALLEL-IN/PARALLEL-OUT
SHIFT REGISTER



PIN ASSIGNMENT



ELECTRICAL CHARACTERISTICS

		VDD	Tic	w*		25°C		Thi		
Characteristic	Symbol	Vdc	Min	Max	Min	Тур	Max	Min	Max	Unit
Output Voltage "0" Level	VOL	5.0	-	0.05	-	0	0.05	-	0.05	Vdc
V _{in} = V _{DD} or 0		10	-	0.05	-	0	0.05	-	0.05	
		15	-	0.05	BULLAR	A 0	0.05	HATTH	0.05	
"1" Level	VOH	5.0	4.95	-	4:95	5.0	SHAPT	4.95	-	Vdc
V _{in} = 0 or V _{DD}		10	9.95	-	9.95	10	-	9.95	-	
THE RESERVE AND A PROPERTY OF THE PARTY OF T		15	14.95	cted- wit	14.95	1015 001	this ti	14.95	e MC14	T
nput Voltage# "0" Level	VIL		gle mon	s in a sir	de device	om Insmi	enhano	ennaile-l	I bes les	Vdc
(V _O = 4.5 or 0.5 Vdc)		5.0	daigen 11	1.5	basholo	2.25	1.5	8. It cos	1.5	einbil.
(V _O = 9.0 or 1.0 Vdc)	100	10	IT Sug	3.0	io beref	4.50	3.0	nso suo	3.0	ditiw
(V _O = 13.5 or 1.5 Vdc)	3A9	15	tio Third	4.0	Hids to	6.75	4.0	(P/S) in	4.0	Paras
garaga ga "1" Level	VIH		nua/Com	a. The	ebru Ün	souts Door	rig via ir	bsol lell	neo suo	chro
(V _O = 0.5 or 4.5 Vdc)		5.0	3.5	naib atuc	3.5	2.75	etermina	3.5	2027	Vdc
(V _O = 1.0 or 9.0 Vdc)		10	7.0		7.0	5.50	p-flop st	7.0	stuntue	D to
(V _O = 1.5 or 13.5 Vdc)		15	11.0	ms the s	11.0	8.25	e dou-d	11.0	STRUTTUO	3 10
Output Drive Current (AL Device)	ГОН		10/11	Cos paso	PH 100 H	paper 21 be	0.000	21111 1081	30 SCH1 5	mAd
(VOH = 2.5 Vdc) Source	·On	5.0	-3.0	-	-2.4	-4.2	Jugni	-1.7	02 5 20 57	pago
(V _{OH} = 4.6 Vdc)	50 m	5.0	-0.64	Sur/Eurita	-0.51	-0.88	effe <u>c</u> tive	-0.36	esiveb en	T
(VOH = 9.5 Vdc)		10	-1.6	NOUDSE.	-1.3	-2.25	1-Ot-Isins	-0.9	parallet-t	ters,
(V _{OH} = 13.5 Vdc)	97111	15	-4.2	a mobris	-3.4	-8.8	enis to i	-2.4	nwap/qu	nois
(VOI = 0.4 Vdc) Sink	IOL	5.0	0.64	plor bas	0.51	0.88	hast_col	0.36	YENGOTT.	mAd
(VOL = 0.5 Vdc)	'OL	10	1.6	_	1.3	2.25	_	0.9	_	.ore
(VOL = 1.5 Vdc)		15	4.2	_	3.4	8.8	shi+2.4s	2.4	n17-nes5	5.0
Output Drive Current (CL/CP Device)	ТОН		1.2			-ourself o			DIO DESIGNA	mAd
(VOH = 2.5 Vdc) Source	НО	5.0	-2.5	_	-2.1	-4.2	nlbso.J 1	-1.7	onerden	MAG
(V _{OH} = 4.6 Vdc)		5.0	-0.52		-0.44	-0.88	First St.	-0.36	Serial	46 0
(V _{OH} = 9.5 Vdc)		10	-1.3	Output	-1.1	-2.25	Consile	-0.9	mondany	0 0
(V _{OH} = 13.5 Vdc)		15	-3.6	_	-3.0	-8.8	- 100	-2.4	dites# vill	7 6
the second second second second	A1756		-		-	-				-
OL .	OL	5.0	0.52	-	0.44	0.88	Jam R v	0.36	уветеоп	mAde
(Vol. = 0.5 Vdc)		10 15	1.3	ck Trans	3.0	2.25 8.8	ed) no a	0.9	tarter Trains	0 0
(V _{OL} = 1.5 Vdc)			-	-	-	1707 14	1000	2.4	- timber	10.0
nput Current (AL Device)	lin	15	-	± 0.1	-	±0.00001	±0.1	-	± 1.0	μAdd
nput Current (CL/CP Device)	lin	15	-	± 0.3	-	±0.00001	± 0.3	DITTED ST	±1.0	μAdd
nput Capacitance	Cin	-			-	5.0	7.5	NOLISTED	O STIME	pF
(V _{in} = 0)					Vdc	Vide to 18	0.E = ag	tage Ran	loV yigg	S @
Quiescent Current (AL Device)	IDD	5.0	W OT W B	5.0	sout JT	0.005	5.0	pnising	150	μAdd
(Per Package)	00	10	eome T l	10	ds Gver	0.010	10	TL tose	300	8
		15	-	20	-	0.015	20	-	600	235
Quiescent Current (CL/CP Device)	IDD	5.0	-	20	-	0.005	20	_	150	μAdo
(Per Package)	00	10	-	40	-	0.010	40	_	300	-
		15	-	80	-	0.015	80		600	
Total Supply Current**†	IT	5.0			1= 11	.0 μA/kHz)	f + les	210 Y 2 00		μAdo
(Dynamic plus Quiescent,		10				.0 μA/kHz)				MAG
Per Package)		15	819			.0 μA/kHz)				y ylaqq
(C ₁ = 50 pF on all outputs, all		shV	Teas			.U MM/KHZ)	00			szloV
buffers switching)			-							-

^{*}T_{Iow} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in} \text{ or } V_{out})$ < VDD.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD).

Noise Margin for both "1" and "0" level = 1.0 Vdc min @ VDD = 5.0 Vdc

^{2.0} Vdc min @ V_{DD} = 10 Vdc 2.5 Vdc min @ V_{DD} = 15 Vdc

[†]To calculate total supply current at loads other than 50 pF: $I_T(C_L) = I_T(50 \text{ pF}) + 1 \times 10^{-3} (C_L - 50) \text{ VDDf}$

where: T is in A (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency. *The formulas given are for the typical characteristics only at $25^{\circ}C$.

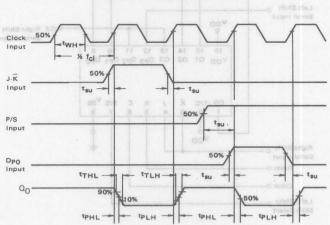
SWITCHING CHARACTERISTICS* (C1 = 50 pF, TA = 25°C)

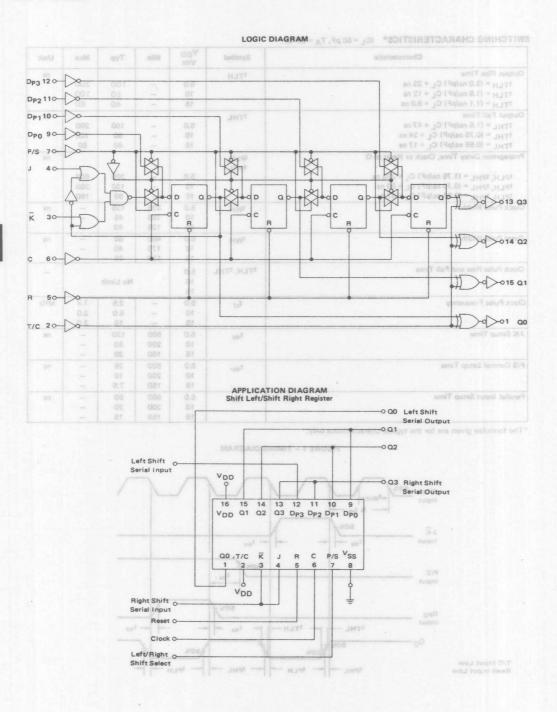
Characteristic	Symbol	V _{DD} Vdc	Min	Тур	Max	Unit
Output Rise Time	tTLH					ns
tTLH = (3.0 ns/pF) CL + 25 ns		5.0	,-	100	200	93 12 O-
t _{TLH} = (1.5 ns/pF) C _L + 12 ns		10	-	50	100	orreg
t _{TLH} = (1.1 ns/pF) C _L + 8.0 ns		15	-	40	80	1 24
Output Fall Time	THL			-		ns
t _{THL} = (1.5 ns/pF) C _L + 47 ns		5.0	-	100	200	
t _{THL} = (0.75 ns/pF) C _L + 24 ns		10	- 1	50	100	-00 pg
t _{THL} = (0.55 ns/pF) C _L + 17 ns		15	-	40	80	Lan
Propagation Delay Time, Clock or Reset to Q	tPLH,		1504	1		ns
	tPHL		HOH	1 V	1	-0.6
tpLH, tpHL = (1.75 ns/pF) CL + 223 ns		5.0	12	300	600	
tpLH, tpHL = (0.70 ns/pF) CL + 89 ns	T INV	10	1500	130	260	
tpLH, tpHL = (0.53 ns/pF) CL + 67 ns	a policy leto	0 15		95	190	
Clock Pulse Width	tWH	5.0	335	135	-	ns
30-1 30-1	30	10	165	45	-	-0E
8 8		15	125	40	-	
Reset Pulse Width	twH	5.0	400	80	-	ns
		10	175	40	-	
		15	130	35		-0.9
Clock Pulse Rise and Fall Time	TLH, THL	5.0				_
		10		No Limit		
		15				
Clock Pulse Frequency	fcl	5.0	-	2.5	1.2	MHz
		10	-	6.0	2.0	
10 10< 0< . [[]		- 15	-	10	3.0	-0E 30
J-K Setup Time	t _{su}	- 5.0	500	120	-	ns
	30	10	200	50	-	
		15	150	30	-	
P/S Control Setup Time	tsu	5.0	500	25	-	ns
	-su	10	200	10	_	
		15	150	7.5	_	
Parallel Input Setup Time		5.0	500	90	† -	ns
	-su	10	200	20	_	1.00
		1	150	15		1

^{*}The formulae given are for the typical characteristics only.

T/C Input Low Reset Input Low

FIGURE 1 - TIMING DIAGRAM







TRIPLE SERIAL ADDERS

The MC14032B and MC14038B triple serial adders have the clock and carry reset inputs common to all three adders. The carry is added on the positive-going clock transition for the MC14032B, and on the negative-going clock transition for the MC14038B. Typical applications include serial arithmetic units, digital correlators, digital servo control systems, datalink computers, and flight control computers.

- Static Operation from dc to 5.0 MHz
- Buffered Outputs
- Single-Phase Clocking
- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range.
- Pin-for-Pin Replacement for CD4032B and CD4038B.

MAXIMUM RATINGS (Voltages referenced to VSS)

Rating	Symbol	Value	Unit
DC Supply Voltage	V _{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	Vin	-0.5 to V _{DD} + 0.5	Vdc
DC Current Drain per Pin	1	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	TA	-55 to +125 -40 to +85	°C
Storage Temperature Range	T _{stg}	-65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leqslant (V_{in} \text{ or } V_{out}) \leqslant V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

MC14038B

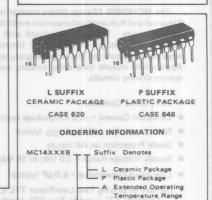
FOR COMPLETE DATA SEE MC14032B

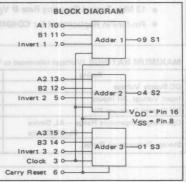
CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

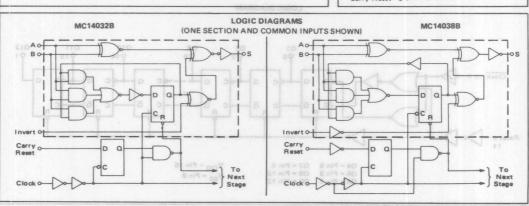
TRIPLE SERIAL ADDERS

Positive Logic - MC14032B Negative Logic - MC14038B





Limited Operating
Temperature Range



3

12-BIT BINARY COUNTER

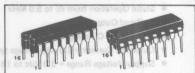
The MC14040B 12-stage binary counter is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. This part is designed with an input wave shaping circuit and 12 stages of ripple-carry binary counter. The device advances the count on the negative-going edge of the clock pulse. Applications include time delay circuits, counter controls, and frequency-driving circuits.

- Fully Static Operation
- Quiescent Current = | 5.0 nA/package typical @ 5 Vdc
- Noise Immunity = 45% of VDD typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Low Input Capacitance = 5.0 pF typical
- Capable of Driving Two Low-Power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range.
- Common Reset Line
- 13 MHz Typical Counting Rate @ VDD = 15 V
- Pin-for-Pin Replacement for CD4040B

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

12-BIT BINARY COUNTER



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

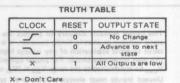
ORDERING INFORMATION

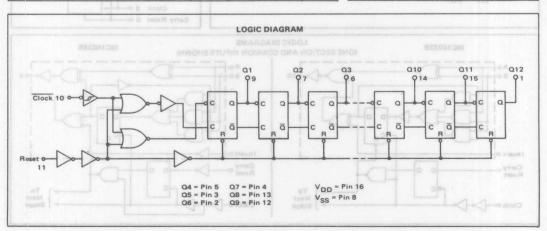
MC14XXXB Suffix Denotes

L Ceramic Package
P Plastic Package
A Extended Operating
Temperature Range
C Limited Operating
Temperature Range

MAXIMUM RATINGS (Voltages referenced to VSS)

Rating	Symbol	Value	Unit
DC Supply Voltage	VDD	-0.5 to +18	Vdc
Input Voltage, All Inputs	Vin	-0.5 to V _{DD} + 0.5	Vdc
DC Current Drain per Pin	- (10	mAdc
Operating Temperature Range — AL Device CL/CP Device	TA	-55 to +125 -40 to +85	°C
Storage Temperature Range	T _{stg}	-65 to +150	°C





ELECTRICAL CHARACTERISTICS

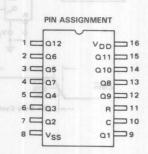
		10000	QGA I	VDD	Tio	w*		25°C	Series of C	Thi	gh*	
	teristic		Symbol	Vdc	Min	Max	Min	Тур	Max	Min	Max	Unit
Output Voltage	"()" Level	VOL	5.0	-	0.05	-	0	0.05		0.05	Vdc
Vin = VDD or 0		-	24/20	10	_	0.05	-	0	0.05	+ 75 140	0.05	171.15
		-	01	15	-	0.05	-	0	0.05	+ JO (3d	0.05	4.172
	00	I" Level	VOH	5.0	4.95		4.95	5.0	100	4.95	-	Vdc
Vin = 0 or VDD				10	9.95	-	9.95	10	-	9.95	emil lis	Tuqtu
200		- CH4	6.0	15	14.95		14.95	15	am Bi	14.95	ian 8. () =	HT
Input Voltage#	00	"O" Level	VIL						-En-0/9 P	29 1 111	W 07.01	Vdc
(Vo = 4.5 or 0.5	Vdc)		6.5	5.0		1.5		2.25	1.5	IDF CL.	1.5	THEFT
(VO = 9.0 or 1.0				10	_	3.0	-	4.50	3.0	Time	3.0	Segrego:
(VO = 13.5 or 1.5	Vdc)	1		15	-	4.0	-	6.75	4.0	-	4.0	Close
		"1" Level	VIH					15 ns	+ 101	1.7 ms/p	F H393	(pug)
$(V_0 = 0.5 \text{ or } 4.5)$	Vdc)	-	0.00	5.0	3.5	-	3.5	2.75	+ 5 9	3.5	= +0.107	Vdc
(VO = 1.0 or 9.0	Vdc)		10	10	7.0	_	7.0	5.50	4-10-1	7.0	- FLIST	11192
(VO = 1.5 or 13.5	Vdc)	1 3	15	15	11.0	-	11.0	8.25	-	11.0	0.00	2177
Output Drive Curren	t (AL De	vice)	Іон							and the state of	1 - 12 - 12	mAdo
(VOH = 2.5 Vdc)		urce	0.00	5.0	-3.0	_	-2.4	-4.2	-1	-1.7	= Funi	75536
(VOH = 4.6 Vdc)		1	10	5.0	-0.64	_	-0.51	-0.88	30,17	-0.36	# Telef	DH97
(VOH = 9.5 Vdc)			15	10	-1.6	_	-1.3	-2.25	T Just	-0.9	_	11481
(VOH = 13.5 Vdc				15	-4.2	-	-3.4	-8.8	_	-2.4	on Delay	a spede
(VOL = 0.4 Vdc)	Sir	nk	IOL	5.0	0.64	-	0.51	0.88	n 705 m	0.36	700	mAdd
(VOL = 0.5 Vdc)			100,10	10	1.6	_	1.3	2.25		0.9	1,11 - 19	1
(VOL = 1.5 Vdc)		-	OT .	15	4.2	-	3.4	8.8	in \$87 + j	2.4	8.00 = JH	12
Output Drive Curren	t (CL /CP	Device)	ГОН						20.1586.4	O Thina	10.3/1	mAdo
(VOH = 2.5 Vdc)		086	000	5.0	-2.5	_	-2.1	-4.2	_	-1.7	strbill so	IIIAGC
(VOH = 4.6 Vdc)		MOL	01.	5.0	-0.52		-0.44	-0.88	-	-0.36		
(VOH = 9.5 Vdc)		811	16	10	-1.3	_	-1.1	-2.25	_	-0.9		
(VOH = 13.5 Vdc) 1.5	-	8.8	15	-3.6	_	-3.0	-8.8	_	-2.4	superfl.or	took Pull
(VOL = 0.4 Vdc)	Sir	nk	lot	5.0	0.52	-	0.44	0.88	_	0.36	-	mAdo
(VOL = 0.5 Vdc)	0.01	1		10	1.3	_	1.1	2.25	_	0.9		
(VOL = 1.5 Vdc)			5.0	15	3.6	_	3.0	8.8	_	2.4	la il bnc s	I Hook
Input Current (AL D	evice)		lin	15	-	± 0.1	-	±0.00001	±0.1	-	± 1.0	μAdc
Input Current (CL/C	P Device	080	lin	15	-	± 0.3	-	±0.00001	± 0.3	-	±1.0	μAdo
Input Capacitance	120	380	Cin	-	-	-	-	5.0	7.5	-	-	pF
(V _{in} = 0)		270	Vin					3.0	7.5			Pi
Quiescent Current (A			IDD	5.0	-	5.0	no amitain	0.005	5.0	rot Tra m	150	'µAdc
(Per Package)			.00	10	_	10	nsitios of	0.010	10	101 918 (11	300	01.911
				15	_	20		0.015	20	-	600	
Quiescent Current (C	L/CP De	vice)	IDD	5.0	_	20	-	0.005	20	-	150	μAdo
(Per Package)			.00	10	_	40	-	0.010	40	1 -	300	mr.de
	T DMIHS	2 - SHIT	FIGURE	15	_	80	1231	0.015	80	04-131	600	
Total Supply Current	PAYAN	GMA THUS	TICIA	5.0			I== 10	42 μA/kHz		THUS MIS	000	μAdo
(Dynamic plus Qu				10				.85 μA/kHz				MAGC.
Per Package)	0	av I		15				43 µA/kHz				
(C ₁ = 50 pF on a	Il output	s. all					1 (1.		JU			
buffers switching		0										

2.0 Vdc min @ V_{DD} = 10 Vdc

2.5 Vdc min @ V_{DD} = 15 Vdc

1To calculate total supply current at loads other than 50 pF: $|T_{\parallel}| = |T_{\parallel}| = |$

input frequency.
**The formulas given are for the typical characteristics only at 25°C.



 $^{^*}T_{low} = -55^{\circ}C$ for AL Device, $-40^{\circ}C$ for CL/CP Device. $T_{high} = +125^{\circ}C$ for AL Device, $+85^{\circ}C$ for CL/CP Device. \pm Noise immunity specified for worst-case input combination.

Noise Margin for both "1" and "0" level = 1.0 Vdc min @ VDD = 5.0 Vdc

SWITCHING CHARACTERISTICS* (CL = 50	0 pF, TA = 25°C)
Characteristic	*wo
Two May Min May Unit	Maga, d., 600gs
O D' T'	

Charac	teristic		"wol	Symbol	V _{DD} Vdc	Min	Тур	Max	Unit
Output Rise Time tTLH = (3.0 ns/pF) CL + 30 ns tTLH = (1.5 ns/pF) CL + 15 ns tTLH = (1.1 ns/pF) CL + 10 ns	0 0		80.0 80.0 80.0	_ trug д	5.0 10 15	leve.1	100 50 40	200 100 80	V Institut
Output Fall Time t _{THL} = (1.5 ns/pF) C _L + 25 ns t _{THL} = (0.75 ns/pF) C _L + 12.5 r t _{THL} = (0.55 ns/pF) C _L + 9.5 ns	Of at	9.95	-	age THL	5.0 10 15	0" Lavel	100 50 40	200 100 80	lo V ruig
Propagation Delay Time Clock to Q1	4,50		3.0	tPLH,			(obV i	9.0 or 1.0	ns
tpHL, tpLH = (1.7 ns/pF) C _L - tpHL, tpLH = (0.66 ns/pF) C _L - tpHL, tpLH = (0.5 ns/pF) C _L - Clock to Q12	+ 137 ns			tPHL a	5.0 10 15	I" Level	400 170 120	800 340 240	- 0VI - 0VI - 0VI
t_{PHL} , $t_{PLH} = (1.7 \text{ ns/pF}) \text{ C}_L \cdot t_{PHL}$, $t_{PLH} = (0.66 \text{ ns/pF}) \text{ C}_L \cdot t_{PHL}$, $t_{PLH} = (0.5 \text{ ns/pF}) \text{ C}_L \cdot t_{PLH}$	+ 867 ns	-2.4 -0.51		5.5 - 3.5 5.0 - 0.6 6.0 - 0.7	5.0 10 15	_ (90 _ 90	2.5 0.9 0.5	5.0 1.8 1.4	HOV)
Propagation Delay Time Reset to Q _n tpHL = (1.7 ns/pF) C _L + 485 tpHL = (0.66 ns/pF) C _L + 18: tpHL = (0.5 ns/pF) C _L + 145	2 ns	-3.4 0.51 1.3 3.4	-	15 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4	5.0 10 15	-	570 215 170	1620 600 450	10A1 10A1 10A1 10A1
Clock Pulse Width	-4.2 -0.88	1.5-		5.0 HW [†] -2.5	5.0 10 15	385 150 115	140 55 38	2.5 Videl	ns HOV
Clock Pulse Frequency	8.8-	-3.0 0.44		a.s. fcl ar	5.0 10 15	-	2.1 7.0 10.0	1.5 3.5 4.5	MHz
Clock Rise and Fall Time	8.8 ± 10000.0±	0.8	1.0±	TLH, THL	5.0 10 15		No Limit	1.5 Vdc) 001 (AL D	ns ns
Reset Pulse Width		-	5.0:	t₩H	5.0 10 15	960 360 270	320 120 80	DAJ <u>O</u>) Ine collected 0)	ns que o tue = m V)
		-		A		1			

^{*} The formulae given are for the typical characteristics only.

FIGURE 1 - POWER DISSIPATION TEST CIRCUIT AND WAVEFORM PVDD ALERT 0.01 μF (1D) Pulse 0 0 C Q1 Generator 02 a_n - 20 ns AT CONTO - 20 ns Clock -V_{DD} -50% -10% -Vss

50% Duty Cycle

sav = s

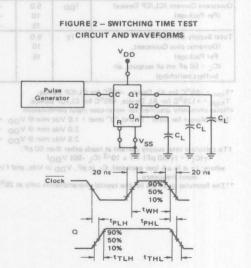
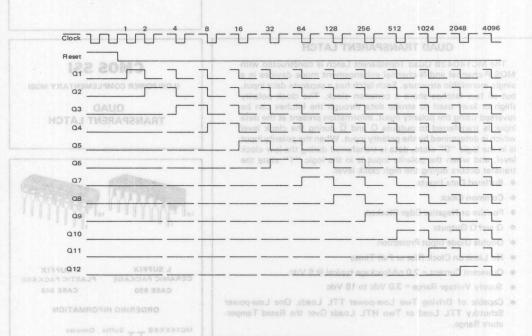


FIGURE 3 - TIMING DIAGRAM

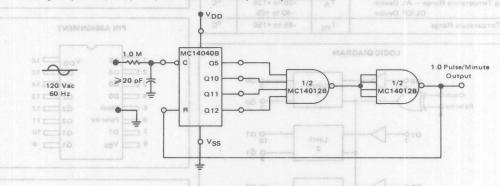


APPLICATIONS INFORMATION

TIME-BASE GENERATOR

A 60 Hz sinewave obtained through a 1.0 Megohm resistor connected directly to a standard 120 Vac power line is applied to the clock input of the MC14040B. By selecting outputs Q5, Q10, Q11, and Q12 division by

3600 is accomplished. The MC14012B decodes the counter outputs, produces a single output pulse, and resets the binary counter. The resulting output frequency is 1.0 pulse/minute.



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leqslant (V_{in} \text{ or } V_{out}) \leqslant V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g. either VSS or VDD).

MC14042B

MC14040B

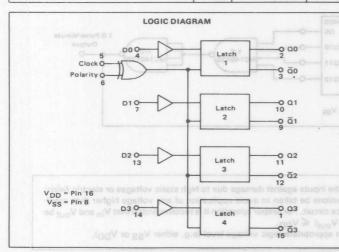
QUAD TRANSPARENT LATCH

The MC14042B Quad Transparent Latch is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. Each latch has a separate data input, but all four latches share a common clock. The clock polarity (high or low) used to strobe data through the latches can be reversed using the polarity input. Information present at the data input is transferred to outputs Q and $\overline{\mathbb{Q}}$ during the clock level which is determined by the polarity input. When the polarity input is in the logic "O" state, data is transferred during the low clock level, and when the polarity input is in the logic "1" state the transfer occurs during the high clock level.

- Buffered Data Inputs
- Common Clock
- Positive or Negative Edge Clocked
- Q and Q Outputs
- Double Diode Input Protection
- No Limit on Clock Rise or Fall Times
- Quiescent Current = 2.0 nA/package typical @ 5 Vdc
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range.

MAXIMUM RATINGS (Voltages referenced to VSS)

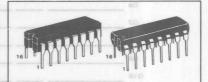
Symbol	Value	Unit
V _{DD}	-0.5 to +18	Vdc
Vin	-0.5 to V _{DD} + 0.5	Vdc
1 . (2) 100	10	mAdo
TA	-55 to +125 -40 to +85	°C
T _{stg}	-65 to +150	°C
	V _{DD} V _{in} I T _A	V _{DD} -0.5 to +18 V _{in} -0.5 to V _{DD} + 0.5 I 10 T _A -55 to +125 -40 to +85



CMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

QUAD
TRANSPARENT LATCH



L SUFFIX
CERAMIC PACKAGE
CASE 620

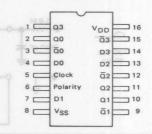
P SUFFIX
PLASTIC PACKAGE

ORDERING INFORMATION

Suffix Denotes

L Ceramic Package
P Plastic Package
A Extended Operating
Temperature Range
C Limited Operating
Temperature Range

PIN ASSIGNMENT



TRUTH TABLE

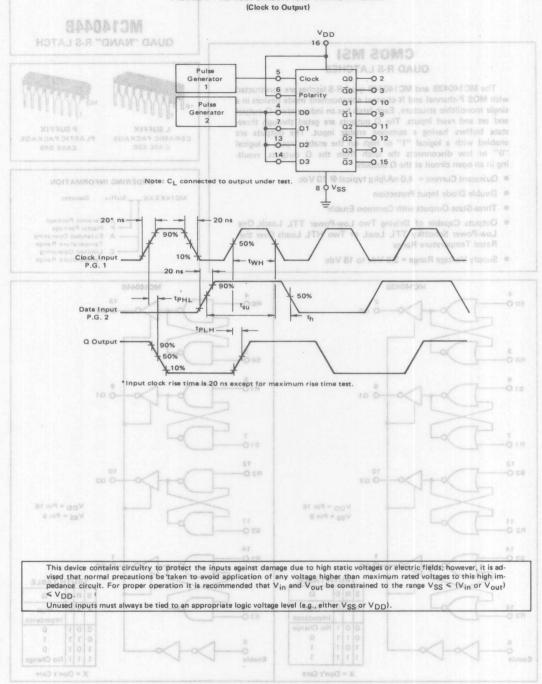
CLOCK	POLARITY	Q
0	0	Data
JRIT-DS	081	Latch
Hally 03	sed vortages	Data
A Jour	sent for pan	Latch

FLECTRICAL CHARACTERISTICS

Vdc 5.0 10 15 5.0 10 15 5.0 10 15 5.0 10 15 5.0 10 15 5.0 10 15 5.0 10 15	Min 4.95 9.95 14.95 3.5 7.0 11.0	Max 0.05 0.05 0.05 1.5 3.0 4.0	Min	Typ 0 0 0 5.0 10 15 2.25 4.50 6.75 2.75 5.50	0.05 0.05 0.05 0.05 	4.95 9.95 14.95	Max 0.05 0.05 0.05 	Vdc Vdc Vdc
10 15 5.0 10 15 5.0 10 15 5.0 10 15 5.0 10 15 5.0 10 15	4.95 9.95 14.95 3.5 7.0	0.05 0.05 - - - 1.5 3.0 4.0	4.95 9.95 14.95	0 0 5.0 10 15 2.25 4.50 6.75	0.05 0.05 - - - 1.5 3.0 4.0	4.95 9.95 14.95	0.05 0.05 - - - - 1.5 3.0 4.0	Vdd
15 5.0 10 15 5.0 10 15 5.0 10 15 5.0 10 15 5.0 10 15 5.0 10 15 5.0 10 15 5.0 10 15 5.0 10 15 5.0 10 10 10 10 10 10 10 10 10 1	4.95 9.95 14.95 - - - 3.5 7.0 11.0	0.05 - - - 1.5 3.0 4.0	4.95 9.95 14.95 ————————————————————————————————————	0 5.0 10 15 2.25 4.50 6.75	0.05 - - 1.5 3.0 4.0	4.95 9.95 14.95	0.05 - - - 1.5 3.0 4.0	Vdd
5.0 10 15 5.0 10 15 5.0 10 15 5.0 10 15 5.0 10 15 5.0 10 15	4.95 9.95 14.95 - - - 3.5 7.0 11.0	1.5 3.0 4.0	9.95 14.95 — — — 3.5 7.0	5.0 10 15 2.25 4.50 6.75	0.05 - - 1.5 3.0 4.0	4.95 9.95 14.95	1.5 3.0 4.0	Vd
10 15 5.0 10 15 5.0 10 15 5.0 10 15 5.0 10	9.95 14.95 - - - 3.5 7.0 11.0	1.5 3.0 4.0	9.95 14.95 — — — 3.5 7.0	5.0 10 15 2.25 4.50 6.75	1.5 3.0 4.0	9.95 14.95 	1.5 3.0 4.0	Vd
10 15 5.0 10 15 5.0 10 15 5.0 10 15 5.0 10	9.95 14.95 - - - 3.5 7.0 11.0	1.5 3.0 4.0	9.95 14.95 — — — 3.5 7.0	10 15 2.25 4.50 6.75	1.5 3.0 4.0	9.95 14.95 	1.5 3.0 4.0	Vd
5.0 10 15 5.0 10 15 5.0 10 15 5.0 10 15	14.95 - - - 3.5 7.0 11.0	1.5 3.0 4.0	14.95 - - - - 3.5 7.0	2.25 4.50 6.75	1.5 3.0 4.0	14.95	1.5 3.0 4.0	Vd
5.0 10 15 5.0 10 15 5.0 10 15 5.0 10 15	- - - 3.5 7.0 11.0	1.5 3.0 4.0	- - - 3.5 7.0	2.25 4.50 6.75	1.5 3.0 4.0	or Demili Aqlan C Aqlan B. U Aqlan B. U	1.5 3.0 4.0	Vde
5.0 10 15 5.0 10 15 5.0	3.5 7.0 11.0	3.0 4.0	3.5 7.0	4.50 6.75 2.75	3.0	7 (<u>s</u>) (p) (p) (p) (p) (p) (p) (p) (p) (p) (p	3.0 4.0	HTId1 ubsdu
5.0 10 15 5.0 10 15 5.0	3.5 7.0 11.0	3.0 4.0	3.5 7.0	4.50 6.75 2.75	3.0	7 (<u>s</u>) (p) (p) (p) (p) (p) (p) (p) (p) (p) (p	3.0 4.0	
5.0 10 15 5.0 10 15 5.0 10 15	3.5 7.0 11.0	4.0	3.5 7.0	6.75 2.75	4.0	1.588_01P	4.0	
5.0 10 15 5.0 10 15	7.0 11.0	-	7.0	2.75	CL + JS ck to D, C	JQVsn d,U		11197
10 15 5.0 10 15	7.0 11.0	-	7.0	100000000000000000000000000000000000000		advsu gv		
10 15 5.0 10 15	7.0 11.0	-	7.0	100000000000000000000000000000000000000				1731
5.0 10 15	11.0	_	100000	5.50		3.5	yaled no	Vdc
5.0 10 15	-		11.0		1617 (0.1	7.0	* HIGT	H:197
10 15 5.0		1.5		8.25	18 4-JU (9	11.0	H197.	1191
10 15 5.0		1 5		81	64 + 10	mighter al. ()	JH91	Vdd
10 15 5.0			_	2.25	1.5	_	1.5	9 sloo
5.0		3.0	-	4.50	3.0	_	3.0	
5.0		3.75		6.75	3.75		3.75	
		0.70		0.75	0.70		0.70	-
	2.5		2 -	0.75		0.5		
10	3.5		3.5	2.75	-	3.5	aren i no	Vdc
45	7.0	-	7.0	5.50	-	7.0	-	
15	11.25	_	11.25	8.25	-	11.25		
								mAd
5.0	-3.0	-	-2.4	-4.2	-	-1.7	- 97	old The
5.0	-0.64	-	-0.51	-0.88	-	-0.36	-	
10	-1.6	-	-1.3	-2.25	-	-0.9	-	
15	-4.2	A -	-3.4	-8.8	-	-2.4	_	
5.0	0.64	-	0.51	0.88		0.36	- 300	mAd
1909.0								1
10	4.2		3.4	0.0		2.4		-
-				-				mAd
				LOST OF BRANDAZION A	the typics		svig helun	ticl or
		-			-		-	
10		_			-		-	
15	-4.2	_	-3.0	-8.8	-	-2.4	-	
5.0	0.52	-	0.44	0.88	-	0.36	-	mAd
10	1.3		1.1	2.25	-	0.9	_	
15	3.6	_	3.0	8.8	_		_	
15		+01			+0.1		+10	μAdo
							_	-
	RIG-7891	± 0.3	REPURSE.	A CONTRACTOR OF THE PARTY OF TH	± 0.3	RIGUR	±1.0	μAdd
-	(FegtuO	or n i s(0)	-	5.0	7.5	-	-	pF
5.0	-	1.0	-	0.002	1.0	-	30	μAdo
10	_	2.0	-	(C) (S) (F)		- 1		
	_		_	2000		7-		
2000					1000			μAde
manufacture of the second	1 678G		170	11.000000000000000000000000000000000000				
			170	-			120	-
							Bella T	μAdd
15	0.0		IT = (3	1.0 µA/kHz)	f + IDD			
		21.0	0.2	90	-			
	15 5.0 10 15 5.0 10 15 5.0 10 15 15 15 15 15 15 15 15 15 15	15	15	15	15	15	15	15

	Totals	Chara	cteristic		1	Ttov	Symbol	VDD	Min	Тур	Max	Unit
Output Rise Tim	e niM	- XeM	gyT	niff	NgN	ni%	tTLH	Symbol		olimino	Chareen	ns
tTLH = (3.0							5.0	5.0	leve J	100	200	oV nuon
tTLH = (1.5	ns/pF) CL +	15 ns					01	10	-	50	100	Vinv
tTLH = (1.1	ns/pF) CL +	10 ns					15	15	-	40	80	Sufe.
Output Fall Tim	e 30 h		6.0	4.95		4.95	tTHL	um V	Level	give		ns
tTHL = (1.5	ns/pF) Cr +	25 ns					Of	5.0	1949.3	100	200	V _{in} <0
tTHL (0.75 m						14.95	ar I	10	-	50	100	ui.
tTHL (0.55 n			4					15	_	40	80	
Propagation Dela			2.25		1	1	tPLH,	21 V	Lieva I Tis	4711	10 700	ns
tPLH, tPHL			5 ns				tPHL	5.0	_	220	440	0.5-90.7
tPLH, tPHL							ar Is	10	_	90	180	B- OV)
tPLH, tPHL	= (0.5 ns/pF) C1 + 35	ns				61	15	100-11-11	60	120	IVO -
Propagation Dela					+	-	*****	HILY	16V9.3 1	1.00	5 or 4.5	ns
tPLH. tPHL							tPLH,	5.0		220		- 100
tPLH, tPHL							tPHL	10	_	90	180	(Vo
tPLH, tPHL	= (0.00 fis/p	10 + 25	7 115				18	25		60	120	(- OV)
		_						23	Jeve J. "O"	00	B1 N. U. 101	ntoV tuo
Clock Pulse Wid							tWH	F.0	000	(ab)	1,5 or 0.5	TO THE PARTY OF
		3.0					10	5.0	300	150	0.1 70 0.1	200
		2.75	6.75				ar	10	100	50	3.5 or 1.5	(VO-
		-						15	80	40	1 -	
Clock Rise Time	3,5						TLH	100			1.5 or 4.5 /	
							10	5.0				400
							ar	10		Limit	5 or 13.5	t = oVI
obAm-								15	fasi	IAL Day	ve Current	O Ivan
Hold Time			-4.2			-3.0	th		8311	Sot	2,5 Vdc	ns
		-					0.8	5.0	100	50	4,644dc	HOVE
							10	10	50	25	9.5-Vdc	HOV)
	-2.6		8.8-				15	15	40	20	13.6 Vd:	HOV)
Setup Time	0.36	-	88.0	0.51		0.64	t _{su}	JO!		Sin	O,4 Vdc)	ns
			2.25				07	5.0	50	0	0.5-Vdc	-JOV)
	2.4		8.8	3.4		4.2	81	10	30	0	1.54/do	110V)
bbAm .								15	25	0	harry Day	O luga
The formulae gi	ven are for	the typic	al character	stics on	lv -		5.0					
9.			88.0-	bb.0-	-						4.8 Vdc)	
											9.5 Vdcl	
	-2.4		8.8-			-4.2					13.5 Vde	
	35.0											
	0.9											
						3.6						
		1.0±							-	Lanna		
	-											
	FIGUR		AND POWE	R DISS			CUIT AND	TIMING	DIAGRA	Nacimed .		
3q -			0:0		(Data to	Output)						
	-		VDD							1		(Vin =1
			16 0		0.1			001		OF VOID A	At Install	11933911
		2.0	1000		2.0		20 ns	-1 -			- 20 ns	(Per Rac
		0.9	0.00.0		4.0		20113				20 115	
30 µAdd	-	5	- see.d		9.0			1	90	0%		1
	-	10	Clock	00	0 20.8	Data I	nput	+	5	10)% feemle	A 1971
		6	Polarity	āo	0 3		TPLH			-	tPHL	
Pulse		004	INDIANA O	01	O 10		5.0	71 1	90%	*	dy Current	
Generate	or	90	DO A 0	<u>ā</u> 1	-09			*	30%	feent,	50%	
1		107+1	SHINAU D.S	1	-	000	tput-	10%		1		
		0	D1	02	O 11			-	tTLH	Duge	*THL	
		13	D2	Q2	O 12						switching	
		14		03	-O 1	-		- 1	TPHL			
		L-0-	D3	Q3	O 15	Q	Output -	90%		To Device	125°C 6	
								1	10%	50%	a viinumi	

To calculate total supply current at loads other than 80 pF: ${\rm Ty}(C_L) = {\rm Ty}(60~{\rm pF}) + 4\times 10^{-3}~(C_L - 50)~{\rm Vpp} t$ where ${\rm Ty}$ is in $\mu{\rm A}$ (per package), C_L in pF, Vpp in Vác, and t in with is input frequency. The formulas given are for the typical characteristics only at $25^{\rm G}{\rm C}$.





CMOS MSI QUAD R-S LATCHES

The MC14043B and MC14044B quad R-S latches are constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. Each latch has an independent Q output and set and reset inputs. The Q outputs are gated through threestate buffers having a common enable input. The outputs are enabled with a logical "1" or high on the enable input; a logical "O" or low disconnects the latch from the Q outputs, resulting in an open circuit at the Q outputs.

- Quiescent Current = 4.0 nA/pkg typical @ 10 Vdc
- Double Diode Input Protection
- Three-State Outputs with Common Enable
- Outputs Capable of Driving Two Low-Power TTL Loads, One Low-Power Schottky TTL Load, or Two HTL Loads Over the Rated Temperature Range
- Supply Voltage Range = 3.0 Vdc to 18 Vdc

MC14043B

QUAD "NOR" R-S LATCH

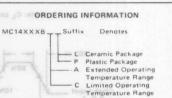
MC14044B

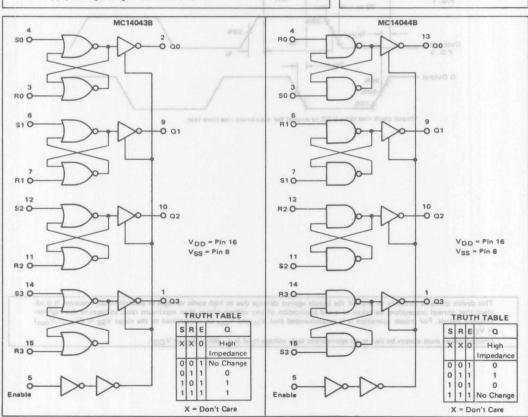
QUAD "NAND" R-S LATCH











ELECTRICAL CHARACTERISTICS

layers against training that to migh static	inv —	VDD	Tic	ow*	166	25°C		Thi	igh *	
Characteristic	Symbol	Vdc	Min	Max	Min	Тур	Max	Min	Max	Unit
Output Voltage "0" Level	VOL	5.0	(911-0)	0.05	00.	0	0.05	_	0.05	Vdc
V _{in} = V _{DD} or 0	0.052	10	O + agV	0.05	Vin	0	0.05	\$114dq	0.05	eV zugr
adance circuit. For proper operation is	prof [15	- 01	0.05	1-	0	0.05	milt vo	0.05	Philip
bo wo bus niv sads bebonnings	VOH	5.0	4.95	88 1	4.95	5.0	0 34 - 1	4.95	erecent i	Vdc
V _{in} = 0 or V _{DD}	MOS. OH	10	9.95	01	9.95	10	O 10/10	9.95	_	
and inputs must always be tied to en	0 × 500	15	14.95	22	14.95	15	-	14.95	100-	-
Input Voltage# "0" Level	VII		0244 0							Vdc
$(V_O = 4.5 \text{ or } 0.5 \text{ Vdc})$		5.0		1.5	-	2.25	1.5		1.5	1
$(V_0 = 9.0 \text{ or } 1.0 \text{ Vdc})$		10	_	3.0	-	4.50	3.0		3.0	
$(V_0 = 13.5 \text{ or } 1.5 \text{ Vdc})$		15	_	4.0	_	6.75	4.0	_	4.0	
"1" Level	VIH	15	-	10082 =	aT Au 0	= 13) *	RISTRES	RACTE	NG CHI	нэти
(V _O = 0.5 or 4.5 Vdc)		5.0	3.5	10.07 -	3.5	2.75	1000	3.5	SERV SPER	Vdc
(V _O = 1.0 or 9.0 Vdc)	aav	10	7.0		7.0	5.50	Chora	7.0		100
(V _O = 1.5 or 13.5 Vdc)	obV.	15	11.0	_	11.0	8.25		11.0		
		15	11.0	-	11.0	0.25		11.0	sent Y and	- 0 -
Output Drive Current (AL Device)	ЮН	5.0	-3:0	_	-2.4	-4.2	# 32.5 ns	-1.7	n 86.1) ×	mAdd
(V _{OH} = 25 Vdc) Source	07		-0.64	-	-0.51	-0.88	all 05 4	-0.36	n 08.01 =	UT1
(V _{OH} = 4.6 Vdc)	1.5	5.0	-1.6	-	-1.3	-2.25	120 (18)	-0.9	n (0,40 n	UTT
(V _{OH} = 9.5 Vdc)		15	-4.2	_	-3.4	-8.8	_	-2.4	amil' Na	Sugge
(V _{OH} = 13.5 Vdc)	2.2		-	-	-	-	an 3.00 a		× 20.33 ×	1111
(V _{OL} = 0.4 Vdc) Sink	OL	5.0	0.64	-	0.51	0.88	20 fts	0.36	n (((T)) =	mAde
(V _{OL} = 0.5 Vdc)		10	1.6	-	1.3	2.25	# 20 ms	0.9	= (0.40 o	HTI
(V _{OL} = 1.5 Vdc)		15	4.2	-	3.4	8.8	-	2.4	on Dalay	100000
Output Drive Current (CL/CP Device)	ЮН							JD (Rely	n 00.00 =	mAde
(V _{OH} = 2.5 Vdc) Source	10	5.0	-2.5	-	-2.1	-4.2	87 m	-1.7	o 80.00) =	192.19
(V _{OH} = 4.6 Vdc)	15	5.0	-0.52	-	-0.44	-0.88	m (4)	-0.36	= (0726 n	11/41
(V _{OH} = 9.5 Vdc)	6,0	10	-1.3	-	-1.1	-2.25	in 061 4	-0.9	n 09.0) =	Held
(V _{OH} = 13.5 Vdc)	nr.	15	-3.6	-	-3.0	-8.8	57.53	-2.4	a 0(710 a	Lares
(VOL = 0.4 Vdc) Sink	IOL	5.0	0.52	-	0.44	0.88	47 m	0.36	n 83:-01 =	mAde
(V _{OL} = 0.5 Vdc)	6,0	10	1.3	-	1.1	2.25	-	0.9	Width	et Pulse
(V _{OL} = 1.5 Vdc)	Dr.	15	3.6	-	3.0	8.8	-	2.4	-	
Input Current (Al. Device)	lin	15	-	± 0.1	-	±0.00001	± 0.1	-	±1.0	μAdd
Input Current (CL/CP Device)	lin	15	-	± 0.3	-	±0.00001	± 0.3	_	±1.0	μAdd
Input Capacitance	Cin	-	-	-	-	5.0	7.5	-	-	pF
(V _{in} = 0) - 05 07	oin					3.0	7.5			
Quiescent Current (AL Device)	Ipp	5.0	-	1.0	-	0.002	1.0	i street (I)	30	μAdo
(Per Package) 08 -	10	10	-	2.0	-	0.004	2.0	-	60	
- 85 110	15	15	-	4.0	-	0.006	4.0	-	120	
Quiescent Current (CL/CP Device)	¹DD	5.0	-	4.0	ing astiair	0.002	4.0	not wis no	30	μAd
(Per Package)	00	10		8.0	- COURT	0.004	8.0		60	1
		15	-	16	-	0.006	16	_	120	
Total Supply Current**†	IT	5.0			1- = 10	.58 µA/kHz	1 6 + 1			μAdd
(Dynamic plus Quiescent, Per Package)		10	VEFORMS		1- = (1	.15 µA/kHz) f + los	,		1
(C _L = 50 pF on all outputs, all outputs switching)	4	15				.73 μA/kHz				
Three-State Output Leakage Current (AL Device)	ITL	15	-	±0.1	zn-90	±0.0001	±0.1	-	±3.0	μAdd
Three-State Output Leakage Current (CL/CP Device)	ITL	15	762	±1.0	_8:01	±0.0001	±1.0	-	±7.5	μAdo

^{*}Tlow = -55°C for AL Device, -40°C for CL/CP Device.

Thigh = +125°C for AL Device, +85°C for CL/CP Device.

#Noise immunity specified for worst-case input combination.

Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc

2.0 Vdc min @ V_{DD} = 10 Vdc

2.5 Vdc min @ V_{DD} = 15 Vdc

1To calculate total supply current at loads other than 50 pF.

IT(CL) = IT(50 pF) + 4 x 10-3 (CL -50) V_{DD} if Vdc, and f in kHz is input frequents.

where: I_T is in µA (per package), C_L in pF. V_{DD} in Vdc, and f in KHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

MAXIMUM RATINGS (Voltages referenced to VSS)

Hall water Rating	Symbol	Value	Unit
DC Supply Voltage	VDD	-0.5 to +18	Vdc
Input Voltage, All Inputs	Vin	-0.5 to V _{DD} + 0.5	Vdc
DC Current Drain per Pin	-1	ag 10	mAdc
Operating Temperature Range — AL Device CL/CP Device	TA	-55 to +125 -40 to +85	O.ºC
Storage Temperature Range	T _{stg}	-65 to +150	°C

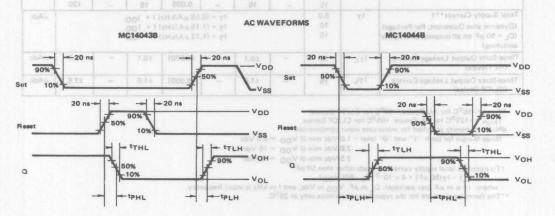
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD).

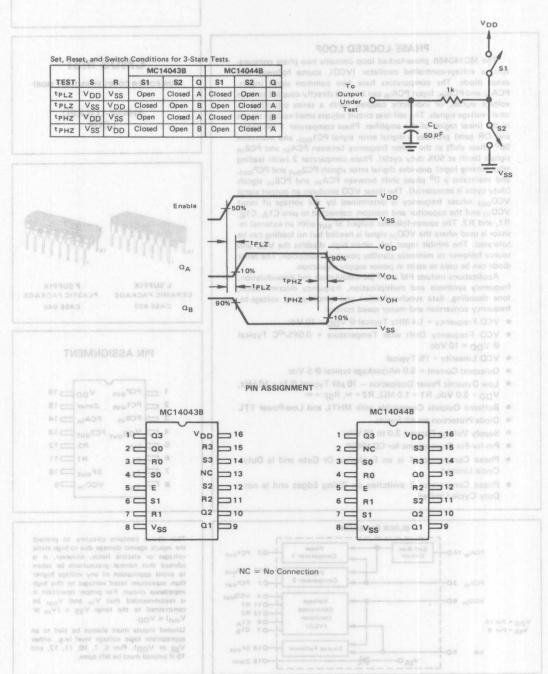
SWITCHING CHARACTERISTICS* (CL = 50 pF, TA = 25°C)

- 0.5 Chara	cteristic				Symbol	VDD	Min	Тур	Max :	Unit
Output Rise Time	68.0	THE STATE OF		9.11	tTLH			(2077	C1 10 C.1	ns
tTLH = (1.35 ns/pF) CL + 32.5 ns						5.0	_ (85)	100	200	a train
tTLH = (0.60 ns/pF) CL + 20 ns					5.0	10	_ 9011	50	100	HOV!
tTLH = (0.40 ns/pF) CL + 20 ns				NB.0-	5.0	15	-	40	80	HOV)
Output Fall Time	2,25	4.6-		5.4-	†THL				OUR PORT	ns
tTHL = (1.35 ns/pF) CL + 32.5 ns					61	5.0	-	100	200	HOAL
tTHL = (0.60 ns/pF) CL + 20 ns	88.0				0.5	10	- 1	50	100	TOAL
tTHL = (0.40 ns/pF) CL + 20 ns					01	15	-	40	80	10.A)
Propagation Delay Time	0.0	P. G.		200	tPLH				30 V G 1 =	ns
tpLH = (0.90 ns/pF) CL + 130 ns						5.0	(enlye)	175	350	G tugtus
tpLH = (0.36 ns/pF) CL + 57 ns	4.2				6.0	10	_ 9918	≥ 75	175	HOVI
tpLH = (0.26 ns/pF) CL + 47 ns					0.8	15	-	60	120	HOVI
tpHI = (0.90 ns/pF) C1 + 130 ns					tPHL	5.0	_	175	350	ns
tpHL = (0.90 ns/pF) CL + 57 ns					1910	10	-	75	175	HOV)
tpHL = (0.26 ns/pF) CL + 47 ns					6.8	15	- 9	60	120	TOAL
Set Pulse Width	25.5	13		T. L.I	tWH	5.0	200	80	DDV_CUV	ns
- 1 24 - 1	8.8				93.	10	100	40	= 1,5_Vdg	TOAL
					15	15	70	30	1 1/8/1 toes	aput Cur
Reset Pulse Width	10000.0±		E.0 E		twH	5.0	200	80	1/1/2 <u>1</u> tress	ns
					- 1	10	100	40	es m utice	rput Cas
						15	70	30	- (0	= niVl
Three-State Enable/Disable Delay	0.002	774	0.1	- 1	tPLZ,	5.0	-	150	300	ns
					tPHZ	10	-	80	160	(Pet P
					et	15	-	55	110	
	1		-		parada and a second				Name of the last o	

*The formulae given are for the typical characteristics only.









MC14046B

PHASE-LOCKED LOOP

The MC14046B phase-locked loop contains two phase comparators, a voltage-controlled oscillator (VCO), source follower, and zener diode. The comparators have two common signal inputs. PCAin and PCBin. Input PCAin can be used directly coupled to large voltage signals, or indirectly coupled (with a series capacitor) to small voltage signals. The self-bias circuit adjusts small voltage signals in the linear region of the amplifier. Phase comparator 1 (an exclusive OR gate) provides a digital error signal PC1_{out}, and maintains 900 phase shift at the center frequency between PCAin and PCBin signals (both at 50% duty cycle). Phase comparator 2 (with leading edge sensing logic) provides digital error signals PC2out and PCPout, and maintains a 00 phase shift between PCAin and PCBin signals (duty cycle is immaterial). The linear VCO produces an output signal VCO_{out} whose frequency is determined by the voltage of input VCOin and the capacitor and resistors connected to pins C1A, C1B, R1, and R2. The source-follower output SFout with an external resistor is used where the VCO_{in} signal is needed but no loading can be tolerated. The inhibit input Inh, when high, disables the VCO and source follower to minimize standby power consumption. The zener diode can be used to assist in power supply regulation.

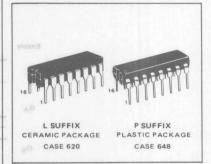
Applications include FM and FSK modulation and demodulation, frequency synthesis and multiplication, frequency discrimination, tone decoding, data synchronization and conditioning, voltage-to-frequency conversion and motor speed control.

- VCO Frequency = 1.4 MHz Typical @ VDD = 10 Vdc
- VCO Frequency Drift with Temperature = 0.04%/OC Typical
 VDD = 10 Vdc
- VCO Linearity = 1% Typical
- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- Low Dynamic Power Dissipation $-70~\mu W$ Typical @ f₀ = 10 kHz, V_{DD} = 5.0 Vdc, R1 = 1.0 M Ω , R2 = ∞ , RSF = ∞
- Buffered Outputs Compatible with MHTL and Low-Power TTL
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 to 18 Vdc
- Pin-for-Pin Replacement for CD4046B
- Phase Comparator 1 is an Exclusive Or Gate and is Duty Cycle Limited
- Phase Comparator 2 switches on Rising Edges and is not Duty Cycle Limited

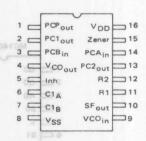
CMOS MSI

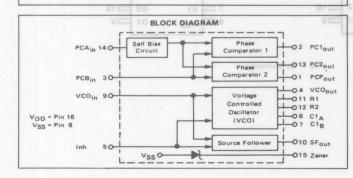
(LOW-POWER COMPLEMENTARY MOS)

PHASE-LOCKED LOOP



PIN ASSIGNMENT





This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leqslant (V_{in} \text{ or } V_{out}) \leqslant V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD). Pins 6, 7, 10, 11, 12, and 15 if unused must be left open.

Rating	Symbol	Value	Unit
DC Supply Voltage	V _{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	Vin	-0.5 to V _{DD} + 0.5	Vdc
DC Current Drain per Pin	1	10	mAdd
Operating Temperature Range AL Device CL/CP Device	TA	-55 to +125 -40 to +85	°C
Storage Temperature Range	T _{stg}	-65 to +150	оС

ELECTRICAL CHARACTERISTICS

	Innunu7	900 IN	V _{DD}	Ti	ow*		25°C		Thi	gh °	
Characteristic	Typical	Symbol	Vdc	Min	Max	Min	Тур	Max	Min	Max	Unit
Output Voltage	"O" Level	VOL	5.0	-	0.05	-	0	0.05	-	0.05	Vdo
Vin = VDD or 0		0.0	10	3.0	0.05	_	0	0.05	+ 318	0.05	HUTT
150 200		7.1	15	0.0	0.05	-	0	0.05	1 10 11	0.05	H217
	"1" Level	VOH	5.0	4.95	-	4.95	5.0	-an-0	4.95	Nan T 11	Vde
Vin = 0 or Vnn	00	On	10	9.95	-	9.95	10	an U	9.95	_	1027
80 111			15	14.95	THE	14.95	15	_	14.95	ami T H	1007
Input Voltage#	"0" Level	VIL		0.0		1		815-10	2011	pletti di Tri	Vdo
(V _O = 4.5 or 0.5 Vdc)		112	5.0	91	1.5	_	2.25	1.5	+ 10 (9q)	1.5	THE
(V _O = 9.0 or 1.0 Vdc)	37		10	15	3.0		4.50	3.0	+ J5 (3g)	3.0	JHT
$(V_O = 13.5 \text{ or } 1.5 \text{ Vdc})$			15	_	4.0	_	6.75	4.0	0 1 2RO1	4.0	KSE O
10.0 01 1.0 4007	"1" Level	VIH	0.1	0.8 1	m.A.	-	0.70		mAD*	- sonate	es Res
(Vo = 0.5 or 4.5 Vdc)	2.0	0.2	5.0	3.5	Albert	3.5	2.75	_	3.5	2311012	Vdc
(Vo = 1.0 or 9.0 Vdc)		1.0	10	7.0			5.50		7.0		Vuc
(Vo = 1.5 or 13.5 Vdc)		and the same of	15		-	7.0					
7	1500	16	0910	11.0	a.H	11.0	8.25		11.0		-
Output Drive Current (AL I		ОН		6.0	mV I				yhyiha		mAd
(V _{OH} = 2.5 Vdc)	Source		5.0	-1.2	-	-1.0	-1.7	-	-0.7	R - Terrigo	AC CO
(V _{OH} = 4.6 Vdc)			5.0	-0.25	-	-0.2	-0.36	idda -	-0.14	0001 = 1	C tori
(V _{OH} = 9.5 Vdc)			10	-0.62	-	-0.5	-0.9	-	-0.35	-	0 30
(V _{OH} = 13.5 Vdc)	C SELON SHO	-	15	-1.8		-1.5	-3.5	- 00	-1.1	2100	12 210
(VOL = 0.4 Vdc)	Sink	IOL	5.0	0.64	-	0.51	0.88	SOUTH	0.36	RTMD3	mAd
(VOL = 0.5 Vdc)		0.35	0810	1.6	vorm!	1.3	2.25		0.9	Frequenc	numio
(VOL = 1.5 Vdc)		0.7	0 15	4.2	-	3.4	8.8	- 3	2.4	act F	1000/
Output Drive Current (CL/0	CP Device)	ІОН	9.1	15					(2 = 4)	bins Jak	mAd
	Source	011	5.0	-1.0	-	-0.8	-1.7	Violet	-0.6	80 7- 60	6150/1
(VOH = 4.6 Vdc)			5.0	-0.2	-	-0.16	-0.36	-	-0.12	- 6	- CAI
(VOH = 9.5 Vdc)		- 1	10	-0.5	_	-0.4	-0.9	-	-0.3	-	1
(VOH = 13.5 Vdc)		-	15	-1.4	-	-1.2	-3.5	_	-1.0	Car T Car	
0	Sink	la.	5.0	0.52		0.44	0.88	81-10	0.36		mAd
(V _{OL} = 0.5 Vdc)	Sink	IOL	10	1.3		1.1	2.25		0.30	V 0350 ×	even.
			15	3.6		3.0	8.8	30 - FR.	2.4	00.0	(03V)
(V _{OL} = 1.5 Vdc)			11.5	-			10000	DI # 18	2.4	1007 1	gov i
Input Current (AL Device)	98	lin	15	5 00 1	± 0.1	-	±0.00001	±0.1	-	±1.0	μAd
nput Current (CL/CP Device	ce) (mail	1 lin	0815	er-	± 0.3		±0.00001	± 0.3	1E00%	±1.0	μAd
Input Capacitance		Cin	-	-	-	-	5.0	7.5	- 83	WeJJos	pF
(V _{in} = 0)	1		-	To T		-	-		-		-
Quiescent Current (AL Dev	ice)	IDD	5.0	or -	5.0	-	0.005	5.0	-	150	μAd
(Per Package)		.00	10	91	10	-	0.010	10	SH Jun'	300	0201
(Inh = "1" and PCA = "1"	9 68.1	3	15	91	20		0.015	20		600	
Quiescent Current (CL/CP I		lan	5.0		-	-	0:005	20			
(Per Package)	Jevice)	IDD	10	0.0	20		0.005	11 45 TRONGS	/ 00.00 : S	150	μAd
(Inh = "1" and PCA = "1"	ao 1	100		07	40	-	0.010	40	7.08.5 + 1	300	ODVI
	90	-	15	35	80			80	V-00-2	600	-
Total Supply Current †		IT.	5.0	-		IT = (1	.46 μA/kHz	f+ IDD			μAd
(Inh = "0", fo = 10 kHz, 0			10	-		IT = (2	2.91 μA/kHz	f + IDD			
R1 = 1 MΩ, R2 = ∞, RSF	= oo, and	6.3	15			1T = (4	1.37 μA/kHz	f + IDD			DV 18/
50% Duty Cycle)	1.00	-	-	1					m (= -1)		Simen

^{*}T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

*Noise immunity specified for worst-case input combination.

[†]To Calculate Total Current in General:

$$\begin{split} &I_{T}\approx 2.2\times V_{DD} - \left(\frac{VCO_{in}-1.65}{R1} + \frac{V_{DD}-1.35}{R2}\right)^{3/4} \\ &+ 1.6\times \left(\frac{VCO_{in}-1.65}{RSF}\right)^{3/4} + 1\times 10^{-3} \, (C_{L}+9) \, V_{DD} \, \, f + \\ &1\times 10^{-1} \, V_{DD}^{2} \left(\frac{100 \cdot \% \, \text{Duty Cycle of PCA}_{in}}{100}\right) + I_{Q} \\ &+ 1.6\times \left(\frac{VCO_{in}-1.65}{RSF}\right)^{3/4} + 1\times 10^{-3} \, (C_{L}+9) \, V_{DD} \, \, f + \\ &1\times 10^{-1} \, V_{DD}^{2} \left(\frac{100 \cdot \% \, \text{Duty Cycle of PCA}_{in}}{100}\right) + I_{Q} \\ &+ 1.6\times \left(\frac{VCO_{in}-1.65}{RSF}\right)^{3/4} + 1\times 10^{-3} \, (C_{L}+9) \, V_{DD} \, \, f + \\ &1\times 10^{-1} \, V_{DD}^{2} \left(\frac{100 \cdot \% \, \text{Duty Cycle of PCA}_{in}}{100}\right) + I_{Q} \\ &+ 1.6\times \left(\frac{VCO_{in}-1.65}{RSF}\right)^{3/4} + 1\times 10^{-3} \, (C_{L}+9) \, V_{DD} \, \, f + \\ &1\times 10^{-2} \, V_{DD}^{2} \left(\frac{100 \cdot \% \, \text{Duty Cycle of PCA}_{in}}{100}\right) + I_{Q} \\ &+ 1.6\times \left(\frac{VCO_{in}-1.65}{RSF}\right)^{3/4} + 1\times 10^{-3} \, (C_{L}+9) \, V_{DD} \, \, f + \\ &1\times 10^{-2} \, V_{DD}^{2} \left(\frac{100 \cdot \% \, \text{Duty Cycle of PCA}_{in}}{100}\right) + I_{Q} \\ &+ 1.6\times \left(\frac{VCO_{in}-1.65}{RSF}\right)^{3/4} + 1\times 10^{-3} \, (C_{L}+9) \, V_{DD} \, \, f + \\ &1\times 10^{-2} \, V_{DD}^{2} \left(\frac{100 \cdot \% \, \text{Duty Cycle of PCA}_{in}}{100}\right) + I_{Q} \\ &+ 1.6\times \left(\frac{VCO_{in}-1.65}{RSF}\right)^{3/4} + 1\times 10^{-3} \, (C_{L}+9) \, V_{DD} \, \, f + \\ &1\times 10^{-2} \, V_{DD}^{2} \left(\frac{100 \cdot \% \, \text{Duty Cycle of PCA}_{in}}{100}\right) + I_{Q} \\ &+ 1.6\times \left(\frac{VCO_{in}-1.65}{RSF}\right)^{3/4} + 1\times 10^{-3} \, (C_{L}+9) \, V_{DD}^{2} \, \, f + \\ &1\times 10^{-2} \, V_{DD}^{2} \, (C_{L}+9) \, V_{DD}^{2} \, \, f + \\ &1\times 10^{-2} \, V_{DD}^{2} \, \, f + \\ &1\times 10^{-2} \, V_{DD}^{2} \, \, f + \\ &1\times 10^{-2} \, V_{DD}^{2} \, \, f + \\ &1\times 10^{-2} \, V_{DD}^{2} \, \, f + \\ &1\times 10^{-2} \, V_{DD}^{2} \, \, f + \\ &1\times 10^{-2} \, V_{DD}^{2} \, \, f + \\ &1\times 10^{-2} \, V_{DD}^{2} \, \, f + \\ &1\times 10^{-2} \, V_{DD}^{2} \, \, f + \\ &1\times 10^{-2} \, V_{DD}^{2} \, \, f + \\ &1\times 10^{-2} \, V_{DD}^{2} \, \, f + \\ &1\times 10^{-2} \, V_{DD}^{2} \, \, f + \\ &1\times 10^{-2} \, V_{DD}^{2} \, \, f + \\ &1\times 10^{-2} \, V_{DD}^{2} \, \, f + \\ &1\times 10^{-2} \, V_{DD}^{2} \, \, f + \\ &1\times 10^{-2} \, V_{DD}^{2} \, \, f + \\ &1\times 10^{-2} \, V_{DD}^{2} \, \, f + \\ &1\times 10^{-2} \, V_{DD}^{2} \, \, f + \\ &1\times 10^{-2} \, V_{DD}^{2} \, \, f + \\ &1\times 10^{-2} \, V_{DD$$

Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc 2.0 Vdc min @ V_{DD} = 10 Vdc 2.5 Vdc min @ V_{DD} = 15 Vdc

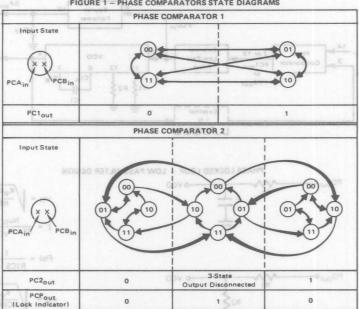
		MAXIMUM RATINGS (Voltages referenced
		Pating
		Input Voltage, All Inputs
-40 to +85	AT	
-65 to +150		

FLECTRICAL	CHARACTERISTICS* (C)	$= 50 \text{ pF} \cdot \text{TA} = 25^{\circ}\text{C}$

5 5 6 6	5.0 10 15 5.0 10 15.	AL Device	CL/CP Device	Typical All Types 180 90 65	AL Device 350 150 110	400 200 160	Units
5	10 15 5.0 10 15.	0.8 61 61 61	HOY.	90 65	150 110	200	ns
5	10 15 5.0 10 15.	25.0 30.0 31.0 5.0		90 65	150 110	200	u.V
5	10 15 5.0 10 15.	5.0		90 65	150 110	200	
50 6	5.0 10 15.	16 15 5.0		100	110		
5	10 15.	5.0	_va_		475		
5	10 15.	5.0	w.		475	100	ns
5	10 15.	01	- Ntr	50	175	200	
6	5.0	01	-	30	75	100	input.
0.1	200	ar		37	55	80	DAN.
0.1	200	201			Islat 2 I	20 3 C C	0.00
0.1		1.0	1.0	2.0	1307 6.1		ΙΜΩ
0.1		0.2	0.2	0.4	5 Vdcl	A 10 2.0 =	(V)
0.4	15	0.1	0.1	0.2	(abV 0)		100 I
5	15	150	15	1500	G.5 V _d ci	= 1.5 or 1	MΩ
		130	HOL				
1	5.0	5.0	HULL	200	300	400	mV p-t
1.25	10			400	600	800 1400	145
1		ai l		700	1050	1400	127
5 t	o 15	21		See Noise	mmunity	Pattan	10
64	0	5.0	ant	Sail	(9)	W 8.0 s	OVI
35	5.0	0.50	0.35	0.70		N 99 = 7	MHz
	10	1.0	0.7	1.4	- (5	N. 91 7	(NO
	15	1.4	1.0	1.9	0\J5) ms	Drive Curr	Output
0.5	5.0	0.6	-	0.12.00		N SE . H	%/°C
	10	5.0	- 1	0.04		V 84 - H	(V)
5.0	15	01-	-	0.015	- (2)	A 8-8 - H	OV)
P.1		15			(36)	H - 13.2	%
	5.0	0.8-	107	1.856		W 140 = 1	030
	10	-10		1	- (3		010
8.8	15	35.	-	1	- (:s	W 6.7 + J	039
	to 15	517	ni-	50	Davion)	A) Munu	96
1	15	150	50	1500	/CP Devic	Uragina (Cil	MSS
		-	113			constitution	InputC
1 5	5.0			1.65	2.2	2.5	Vdc
	10	5.0	201	1.65	2.2	2'5	Chieso
1	15	10	-	1.65	2.2	2.5	(20)
	-				1 - B A-8		0%
5	5.0		ool.	0.1	1 43/TO)	merug 2 in	
	10		- 1	0.6		Packagel	
4	15	61	-	0.8	"I" = AD	Lona T	doll
		00	7	20000	0.000.00	A STATE OF THE PERSON NAMED IN	10107
T	- 1	6.7	6.3	7.0	7.3	7.7	Vdc
	- 1	~		-	_	alov2 vsui	0
		aniver f	1900 10	1000	aivell 1A	AV) JAN 18	1
	1		10 1 15 1 - 6.7	- 6.7 6.3	- 6.7 6.3 7.0 100	- 6.7 6.3 7.0 7.3 - 100	10 - 0.6 - 0

^{*} The formulae given are for the typical characteristics only.

 $\begin{array}{c} + 1.6 \times \left(\frac{\text{VOO}_{10} - 1.66}{\text{RSp}}\right)^{3/4} + 1 \times 10^{-3} \, (\text{CL} + 8) \, \text{VOO} \, \text{ f.} + \\ \text{where: IT in JA, CL, in pF, VCO}_{10}, \, \text{VQQ in Vec, f. in KHz, and} \\ \text{Q1, K2, RSp} \, \text{in M0, CL, on VCO}_{out}. \end{array}$

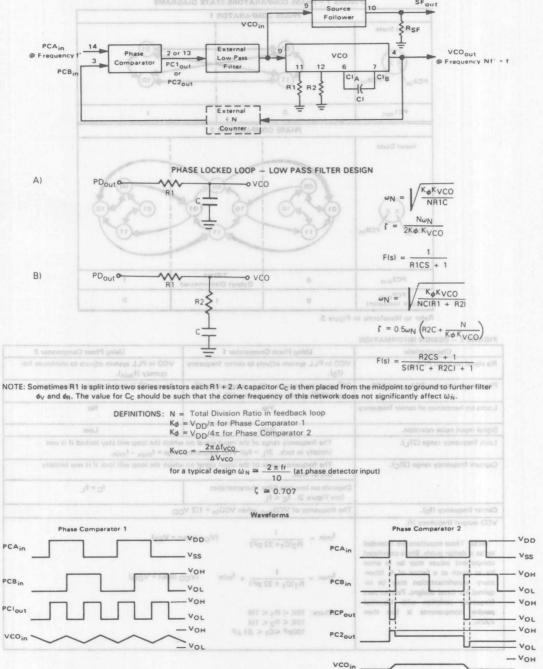


Refer to Waveforms in Figure 3.

FIGURE 2 - DESIGN INFORMATION

Characteristic	Using Phase Comparator 1	Using Phase Comparator 2				
No signal on input PCAin.	VCO in PLL system adjusts to center frequency (f ₀).	VCO in PLL system adjusts to minimum frequency (f _{min}).				
Phase angle between PCA _{in} and PCB _{in} .	90° at center frequency (f ₀), approaching 0° and 180° at ends of lock range (2f _L).					
Locks on harmonics of center frequency.	Total Division Ratio in feedback loop	No DEFINITIONS: N				
Signal input noise rejection.	C totalan High and and a Manute	Low				
Lock frequency range (2f _L).	The frequency range of the input signal on which the loop will stay locked if it was initially in lock. 2f _L = full VCO frequency range = f _{max} - f _{min} .					
Capture frequency range (2f _C).	The frequency range of the input signal on which the loop will lock if it was initially out of lock.					
	Depends on low-pass filter characteristics (see Figure 3). fc < fL	f _C = f _L				
Center frequency (f ₀).	The frequency of VCOout, when VCOin = 1/2 V	'DD				
VCO output frequency (f). Note: These equations are intended to be a design guide. Since calculated component values may be in error by as much as a factor of 4, laboratory experimentation may be re-	$f_{min} = \frac{I}{R_2(C_1 + 32 pF)}$ (V _{CO} inpotential inputs of the contraction of the c	ut = V _{SS}) O input = V _{DD})				
quired for fixed designs. Part to part frequency variation with identical pessive components is less than ±20%.	Where: 10K < R ₁ < 1M 10K < R ₂ < 1M	100/3				
	100pF <c<sub>1 < .01 μF</c<sub>					

- VOL



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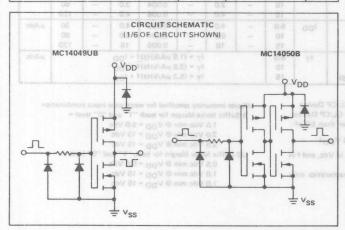
HEX BUFFERS

The MC14049UB hex inverter/buffer and MC14050B non-inverting hex buffer are constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These complementary MOS devices find primary use where low power dissipation and/or high noise immunity is desired. These devices provide logic-level conversion using only one supply voltage, VDD. The input-signal high level (VIH) can exceed the VDD supply voltage for logic-level conversions. Two TTL/DTL Loads can be driven when the devices are used as CMOS-to-TTL/DTL converters (VDD = 5.0 V, VOL \leqslant 0.4 V, IOL \geqslant 3.2 mA). Note that pins 13 and 16 are not connected internally on these devices; consequently connections to these terminals will not affect circuit operation.

- High Source and Sink Currents
- High-to-Low Level Converter
- Quiescent Current = 2.0 nA/package typical @ 5 Vdc
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Meets JEDEC UB Specifications—MC14049UB
 Meets JEDEC B Specification—MC14050B
- V_{IN} can exceed V_{DD}

MAXIMUM RATINGS (Voltages referenced to VSS, Pin 8)

Rating	Symbol	Value	Unit
DC Supply Voltage	, V _{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	Vin	-0.5 to $+30$	Vdc
DC Current Drain per Input Pin	1 70	10	mAdc
DC Current Drain per Output Pin	1 2 5	45	mAdc
Operating Temperature Range · AL Device CL/CP Device	_ TA _	-55 to +125 -40 to +85	,c
Storage Temperature Range	T _{stg}	-65 to +150	°C

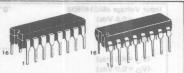


CMOS SSI

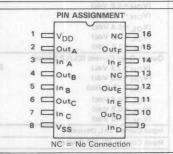
(LOW-POWER COMPLEMENTARY MOS)

HEX BUFFERS

Inverting - MC14049UB Noninverting - MC14050B



L SUFFIX CERAMIC PACKAGE CASE 620 P SUFFIX
PLASTIC PACKAGE
CASE 648



LOGIC DIAGRAMS

MC14049UB	MC14050B
3—2	3—2
	5——4
7—6	7 6
910	
11-0-12	
14 15	14
NC = Pin 13, 16 V _{SS} = Pin 8 V _{DD} = Pin 1	NC = Pin 13, 16 V _{SS} = Pin 8 V _{DD} = Pin 1



ELECTRICAL CHARACTERISTICS

Characteristic			VDD	T _{low} *		25°C			Thigh*		
		Symbol	Vdc	Min	Max	Min	Тур	Max	Min	Max	Unit
Output Voltage "0"	Level	VOL	5.0	-	0.05	-	0	0.05	-	0.05	Vdc
Vin = VDD or 0	10		10	-	0.05	-	0	0.05	-	0.05	
"" CMOS SSI			15	-	0.05	-	0	0.05	-	0.05	
ice cumu "i"	Level	VOH	5.0	4.95	-	4.95	5.0	-	4.95	-	Vdc
(LOW-POWER COMPLEMENTARY MOS)			10	9.95	-	9.95	10	-	9.95	-	11/18
		-500	15	14.95	han y	14.95	. 15	H BU	14.95	Mod	-
	Level	VIL	leans	6-9 B	intr-Ivit	cted v	untengo i	de rei	ud xa	1.0	Vdc
(V _O = 4.5 Vdc)		pirts	5.0	single	1.0	spiveb	2.25	1.0	enhar		-1/1
$(V_0 = 9.0 \text{ Vdc})$	111	981/	10	a bailt i	2.0	SOM	4.50	2.0	These	2.0	Str
(V _O = 13.5 Vdc)			15	N. 10-11-1	2.5	701071	6.75	2.5	WOO Y	2.5	
(V _O = 0.5 Vdc) minsyninov "1"	Level	VIH	THE INCHES	n cons	and to		d okinessi	2 5 2 1		T heni	Vdc
(VO = 1.0 Vdc)		Anic	5.0	4.0	102 9 1 151	4.0	2.75	Nicas	4.0		teb
(V _O = 1.5 Vdc)	- -	nso	10	8.0 12.5	id tord	8.0	5.50 8.25	gV-,eg	12.5	ds b ees	no
	7	OW.	1032016		loxar	100000	C OF MARKET	ylgans	-		
	Level	VIL	5.0	is sepin	1.5	merly	2.25	1.5	abso.	JTQ\	Vdc
(V _O = 0.5 Vdc) (V _O = 1.0 Vdc)		.V	10	104 V	3.0	= 00	4.50	3.0	COMMI	3.0	CIV
(V _O = 1.5 Vdc)		-ni t	15	ios Jon	4.0	S and	6.75	4.0	(Am	4.0	101
	Level	VIH	13 03 0	noiner	100 Y	House	0000 (80	OI WOO	reoria -	O VIIO	Vdc
(VO = 4.5 Vdc)	Level	VIH	5.0	3.5	0	3.5	2.75	affect	3.5	elsoin	797
(VO = 9.0 Vdc)	111		10	7.0		7.0	5.50	nd-Sid	7.0	High S	0
(VO = 13.5 Vdc) X199U2 J			15	11	_	11	8.25	O levo	111	st-r le siH	0
Output Drive Current (AL Device)		ГОН	Vdc	B on less	igyt ei	nacket	2.0 nA	= Siver	U3 200	Oujesc	mAd
	ource	-OH	5.0	-1.6	V ST	-1.25	-2.5	ni d a	-0.9	vla g u2	8
(V _{OH} = 9.5 Vdc)	-	- 1	10	-1.6	NOETC	-1.3	-2.6	UBS	-0.9	Maets	0
(VOH = 13.5 Vdc) 2A M9			15	-4.7	MOSTAN	-3.75	-10	200	-2.7	61261/1	-
(VOL = 0.4 Vdc)	Sink	loL	5.0	3.75	-	3.2	6.0	-	2.1		mAd
(VOL = 0.5 Vdc)		0.	10	10	-	8.0	16	IQ√ be	5.6	V _{IN} ca	0
(VOL = 1.5 Vdc)			15	30	-	24	40	-	16.8	-	
Output Drive Current (CL/CP Device)		ГОН									mAd
(V _{OH} = 2.5 Vdc) S	ource	0	5.0	-1.5	-	-1.25	-2.5	-	-1.0		
(VOH = 9.5 Vdc)			10	-1.5	18 mg	-1.3	-2.6	tgsttoV)	-1.0	MBAT	MAIN
(V _{OH} = 13.5 Vdc)	1 12	u l	15	-4.5	-100	-3.75	-10	-	-3.0	-	
(VOL = 0.4 Vdc)	Sink	IOL	5.0	3.6	-	3.2	6.0	-	2.6	vol/ToV	mAd
(VOL = 0.5 Vdc)	1	V	10	9.6	-	8.0	16	-	6.6	HA or	tinV n
(VOL - 1.5 Vdc)			15	28	-	24	40	-	19	_	
Input Current (AL Device)		lin	15	-	± 0.1	-	±0.00001	± 0.1	noctor in	± 1.0	μAd
Input Current (CL/CP Device)	1	lin	15	25.75	± 0.3	-	± 0.00001	± 0.3	nging o	± 1.0	μAdd
Input Capacitance (Vin = 0)		Cin	8+ o	1-09-	1-	-	10 Dayage	20		- In-	pF
Quiescent Current (AL Device)	111	IDD	5.0	0.00	1.0	2 -	0.002	1.0	senelt e	30	μAd
(Per Package)	1	00	10	-	2.0	-	0.004	2.0	-	60	
MC14049UB MC14060B	Lot		15	-	4.0	-	0.006	4.0	-	120	-
Quiescent Current (CL/CP Device)		IDD	5.0	-	4.0	HEMAT	0.002	4.0	-	30	μAd
(Per Package)		00	10	-	8.0	OH2 TH	0.004	8.0	-	60	
Man Man			15	-	16	-	0.006	16	-	120	
Total Supply Current**†		IT	5.0	10		IT = (1.	8 μA/kHz)	f + IDD	soe	PORT DISC	μAd
(Dynamic plus Quiescent, Per Package)	FI		10				5 μA/kHz)				
(CL 50 pF on all outputs, all buffers switchi	ing)		15				3 μA/kHz)				

 $^{^*}T_{low} = -55\,^\circ\text{C}$ for AL Device, $-40\,^\circ\text{C}$ for CL/CP Device. Thigh = $+125\,^\circ\text{C}$ for AL Device, $+85\,^\circ\text{C}$ for CL/CP Device. †To Calculate total supply current at loads other than 50 pF:

IT (CL) = IT (50 pF) + 6 x 10-3 (CL - 50) VDDf

where: IT is in μA (per package), CL in pF, VDD in Vdc, and f in kHz is input frequency.

#Noise immunity specified for worst-case input combination

B Suffix Noise Margin for both "1" and "0" level =

1.0 Vdc min @ V_{DD} = 5.0 Vdc 2.0 Vdc min @ V_{DD} = 10 Vdc

2.5 Vdc min @ V_{DD} = 15 Vdc
UB Suffix Noise Margin for both "1" and "0" level =

0.5 Vdc min @ V_{DD} = 5.0 Vdc 1.0 Vdc min @ V_{DD} = 10 Vdc 1.0 Vdc min @ V_{DD} = 15 Vdc

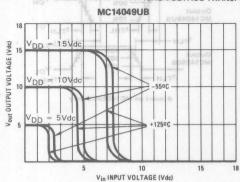
^{**}The formulas given are for the typical characteristics only

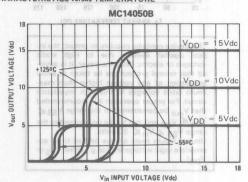
SWITCHING CHARACTERISTICS* (CL = 50 pF, TA = 25°C) 2017218370ARAHO 30AUGS TUSTUO JADISYT - S BRUDIS

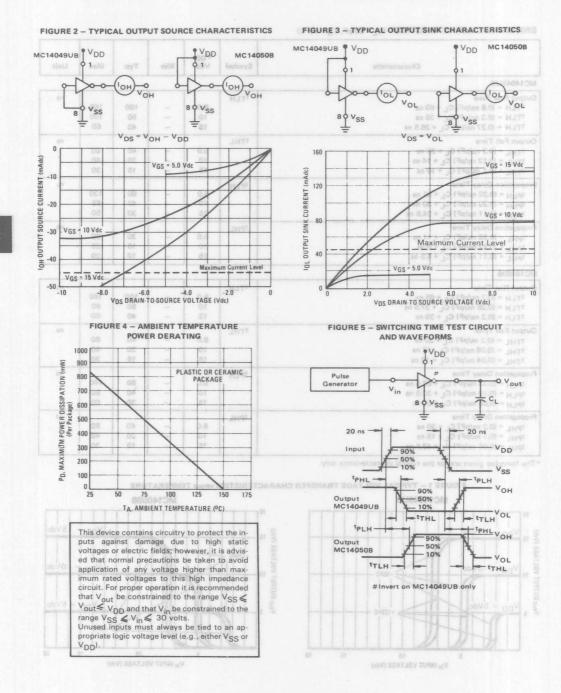
Characteristic	Symbol	V _{DD} Vdc	Min	Тур	Max 9	euesos: Unit
MC14049UB	o-(unt)	01		0-(40)	-0-0	1-0
Output Rise Time tTLH = (0.8 ns/pF) C _L + 60 ns tTLH = (0.3 ns/pF) C _L + 35 ns tTLH = (0.27 ns/pF) C _L + 26.5 ns	t _{TLH}	5.0 10 15	=	100 50 40	160 100 60	ns
Output Fall Time tTHL = (0.3 ns/pF) C _L + 25 ns tTHL = (0.12 ns/pF) C _L + 14 ns tTHL = (0.1 ns/pF) C _L + 10 ns	tTHL	5.0 10 15	0.8 = 5.0 V	40 20 15	60 40 30	ns
Propagation Delay Time tp_H = (0.38 ns/pF) C_ + 61 ns tp_H = (0.20 ns/pF) C_ + 30 ns tp_H = (0.11 ns/pF) C_ + 24.5 ns	tPLH	5.0 10 15		80 40 30	120 65 50	ns 85-
Propagation Delay Time tpHL = (0.38 ns/pF) C _L + 11 ns tpHL = (0.12 ns/pF) C _L + 9 ns tpHL = (0.11 ns/pF) C _L + 4.5 ns	^t PHL	5.0 10 15	1	30 15 10	60 30 20	28 V ^{ns} 08-
MC14050B	THE PROPERTY OF	introduction of		>	aby at	
Output Rise Time tTLH = (0.7 ns/pF) CL + 65 ns tTLH = (0.25 ns/pF) CL + 37.5 ns tTLH = (0.2 ns/pF) CL + 30 ns	tTLH ₂	5.0 10 15	3380080	100 50 40	160 80 60	ns 0ā-
Output Fall Time t _{THL} = (0.2 ns/pF) C _L + 30 ns t _{THL} = (0.06 ns/pF) C _L +17 ns t _{THL} = (0.04 ns/pF) C _L + 13 ns	tTHL	5.0 10 15	FARBOR	40 20 15	60 40 30	ns
Propagation Delay Time tp_H = (0.33 ns/pF) C_ + 63.5 ns tp_H = (0.19 ns/pF) C_ + 30.5 ns tp_H = (0.06 ns/pF) C_ + 27 ns	^t PLH	5.0 10 15	19 - -	80 40 30	140 80 60	ns
Propagation Delay Time tpHL = (0.2 ns/pF) CL + 30 ns tpHL = (0.1 ns/pF) CL + 15 ns tpHL = (0.05 ns/pF) CL + 12.5 ns	tPHL	5.0 10 15	1	40 20 15	80 40 30	OR SWOR IND

^{*}The formulae given are for the typical characteristics only.

FIGURE 1 - TYPICAL VOLTAGE TRANSFER CHARACTERISTICS Versus TEMPERATURE









MC14051B MC14052B MC14053B

ANALOG MULTIPLEXERS/DEMULTIPLEXERS

The MC14051B, MC14052B, and MC14053B, analog multiplexers are digitally controlled analog switches. The MC14051B effectively implements an 8PST electronic switch, the MC14052B a 4PDT or 2P4T, and the MC14053B a DP3T or 3P2T. All three devices feature low ON impedance and very low OFF leakage current. Control of analog signals up to the complete supply voltage range can be achieved.

- High On/Off Output Voltage Ratio 65 dB typical
- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- Low Crosstalk Between Switches 80 dB typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Analog Voltage Range (V_{DD}-V_{EE}) = 3 to 18 V
 Note: V_{EE} must be

 ✓ V_{SS}
- Transmits Frequencies Up to 65 MHz
- Linearized Transfer Characteristics, $\triangle R_{ON}$ <60 Ω for V_{in} = V_{DD} to V_{EE} @ 15 V_{dc}
- Low Noise 12 nV/√ Cycle, f ≥ 1 kHz typical
- Pin-for-Pin Replacement for CD4051, CD4052, and CD4053

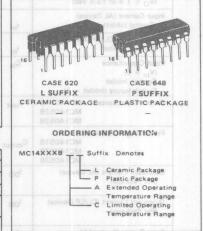
MAXIMUM BATINGS

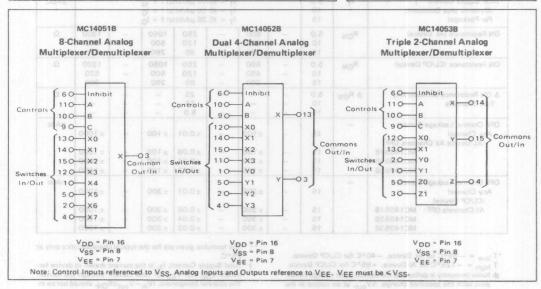
Rating	Symbol	Value	Unit
DC Supply Voltage	VDD.VEE	-0.5 to +18	Vdc
Input Voltage, All Inputs	Vin	-0.5 to VDD + 0.5	Vdc
Through Current 008 - 00	- 1 o.c.s	02 25 -	mAdo
Operating Temperature Range - AL Device CL/CP Device	- AT 0.008	-55 to +125 -40 to +85	°°C
Storage Temperature Range	Tstg	-65 to +150	оС

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

ANALOG MULTIPLEXERS/ DEMULTIPLEXERS





MOTOROLA

ELECTRICAL CHARACTERISTICS

	GCCOAL ASS		V _{DD} -	T _{low} *		25°C			Thi		
	Characteristic	Symbol	Vdc	Min	Max	Min	Тур	Max	Min	Max	Unit
	Output Voltage "0" Level	VOL	5.0	-	0.005	_	0	0.05	-	0.05	Vdc
	Vin = VDD or VSS	OL .	10	-	0.05	-	0	0.05	-	0.05	
	V _{SS} = V _{EE}	11	15	-	0.05	-	0	0.05	-	0.05	
	"1" Level	Vон	5.0	4.95	187	4.95	5.0	LEXE	4.95	MEDICAL	Vdc
	V _{in} = 0 or V _{DD}	On	10	9.95	_	9.95	10	_	9.95	_	
	OW POWER COMPLEMENTARY M	1.1	15	14.95	m pelso	14.95	15	152B, at	14.95	C149511	
	Input Voltage (Control) # "O" Level	VIL	vi	autactius	40518	COM and	C sociati	we pole	ns hello	tingo yli	Vdc
	$(V_O = 4.5 \text{ or } 0.5 \text{ Vdc})$	- IF	5.0	TORNE	1.5	rold a	2.25	1.5	-1-TO	1.5	nemalor
	$(V_0 = 9.0 \text{ or } 1.0 \text{ Vdc})$		10	127.16.1	3.0	a second	4.50	3.0	hata 10	3.0	de constitue
	(V _O = 13.5 or 1.5 Vdc)		15	1881 189 1881 189	4.0	ris ITA.	6.75	4.0	BEGORI	4.0	na Ta
	"1" Level	V	10	100800	JOSTIL	в врали	11 770	MOL VIB	v bna e	mpedan	Vdc
	(V _O = 0.5 or 4.5 Vdc)	VIH	5.0	3.5	d ngo sg	3.5	2.75	e atalar	3.5	nalsup to	pis golsi
	$(V_0 = 1.0 \text{ or } 9.0 \text{ Vdc})$		10	7.0		7.0	5.50		7.0		
	$(V_0 = 1.5 \text{ or } 13.5 \text{ Vdc})$		15	11.25	lisaid	11.0	8.25	ltage F	11.0	0 110\n0	High
			15	11.25	obV 3	11.0	0.23	nal An I	11.0	HUD TON	Quico
	Input Current (AL Device)			. 77	tes	in the state of	08 ± 39		anuraS	ollarzzon?	wo.l
	(Control Inhibit)	in	15	-	±0.1	with on	0.00001	±0.1	0.00.00	±1.0	μAdc
į	Input Current (CL/CP Device)	0 11				ob)/	RT ±r of	V 0.5 -	anna S.	y Voltage	Suppl
	(Control, Inhibit)	lin	15		±0.3	304	0.00001	±0.3	egneñ.	±1.0	μAdc
			10		10.0	03.6	0.00001	UELS / S	Bursa er	200000	0.00
	Input Capacitance	C _{in}							> 8d 78	nu 33A	pF
	$(V_{in} = 0)$				n is no		s MM a		uencies	penil stin	lensy1.
	Control, Inhibit		-	-	भारत Ω	08> NO	5.0	7.5	isfer Cha	isser Train	Linear
	Switch Inputs (Inhibit = 1)			-	-	-	10	21.0	aaV ol	aaV =	Vie
	Output Capacitance MC14051B	Cout	10	-	-	Isaidvi	96	1 - STSV C	NA Vn S	-Train	pf
	MC14052B		10	6200	and CD	сапьо	48	IO Tot I	warning!	Pin Rep	Pin-to
	MC14053B		10	-	-	-	24	-	-	-	
	Feedthrough Capacitance										
	MC14051B	C _{in-out}	10	-	-	-	0.18	_	-	TINGS	pf
	MC14052B	OM I	. 10		1117	Trucks	0.12	-	-	nits of	
	MC14053B		10		-	- 3	0.10		-	-	
	Quiescent Current (AL Device)	IDD	5.0		5.0	1997	0.005	5.0	_	150	μAdc
	(Per Package)	00	10	8.0 + 0	10	0-1_:01	0.010	10	_	300	Lage: Al
	Israed balantika A	1.1	15	-	20	_	0.015	20	-	600	Current
Ī	Quiescent Current (CL/CP Device)	IDD	5.0	125-	20	1- 0	0.005	20	1A_ 90	150	μAdc
	(Per Package)	יטטי	10	-28	40	-	0.010	40	9040	300	μΑας
	i di Tadiago,		15	-	80		0.015	80	-	600	
	Total Supply Current **†	-	5.0	003	0,000	1 10	.07 μA/kH			000	ADC
	(Dynamic plus Quiescent,	¹T	10				.20 μA/kH				μADC
	Per Package)		15				.20 μA/kH				
_				-	1000	1 = 10	1	-	1	1	
	ON Resistance (AL Device)	RON	5.0	-	800	-	250	1050	- "	1300	Ω
			10	itonA lo	400	h bueG	120	500	palen	550	3.6
	Nultiplemer/Demultiplexer		15	plqi#lon	220	Suffigia	80	280	cel aithu	320	slqitlul
	ON Resistance (CL/CP Device)	RON	5.0	_	880	_	250	1050	_	1200	Ω
		OIN	10	-	450	_	120	500	_	520	
			15		250	-	80	280	-	300	
	Δ ON Resistance Between Any	Δ R _{ON}	5.0		idida F	-027	25	_		dut-1	οαΩ
	Two Channels		10	_	-0-		10	_	1	-	OTT
		Contri	15				5.0	_	1		213
	OFF Channel Leakage Current						-				nAdc
			15		±100	120-	±0.01	± 100		±1000	HAUC
					1.00	140-	10.01	1100		11000	[130
	Any Channel	750000			±100	-0.81	±0.08	±100		±1000	140
	Any Channel (AL Device All Channels OFF:	zoome d'ile	15						D X		
	Any Channel (AL Device All Channels OFF: MC14051B	amons at/la Switch	15 15			-011	+0.04	+ 100	100	+ 1000	0011
	Any Channel (AL Device All Channels OFF: MC14051B MC14052B		15	-	±100	-041	±0.04 +0.02	± 100 ± 100	ma37	± 1000 + 1000	061
	Any Channel (AL Device All Channels OFF: MC14051B MC14052B MC14053B	Switch		- - -	±100 ±100	-0+	±0.04 ±0.02	± 100 ± 100	Con	±1000	120
	Any Channel (AL Device All Channels OFF: MC14051B MC14052B MC14053B OFF Channel Leakage Current	Switch	15 15		±100 ±100	-0+ -03	±0.02	±100	00	±1000	nAdc
	Any Channel (AL Device All Channels OFF: MC140518 MC140528 MC140538 OFF Channel Leakage Current Any Channel	Switch	15		±100 ±100	-0+			- O.	±1000	120
	Any Channel (AL Device All Channels OFF:	Switch	15 15	- v	±100 ±100	-0+ -03	±0.02	± 100	(Com	±1000	nAdc
	Any Channel (AL Device All Channels OFF: MC140518 MC140528 MC140538 OFF Channel Leakage Current Any Channel	Switch	15 15		±100 ±100	-0+ -03	±0.02	±100	(Com	±1000	nAdc

^{*}T low = −55°C for AL Device, −40°C for CL/CP Device. T high = +125°C for Al Device, +85°C for CL/CP Device. Noise immunity is defined as the control input voltage coincident with the specified change, ΔV_{out}, at an output in the OFF State.

^{••} The formulas given are for the typical characteristics only at 25°C.

⁷ Total Supply Current, I_T, is the current drawn at device terminals V_{DD} and V_{SS} for total current through the device. The channel component, (V_{in}-V_{out})/R_{ON}, should not be included.

MC140518 • MC140528 • MC140538

SWITCHING	CHARACTERISTICS*	(C1 = 50 pF. TA = 25°C)

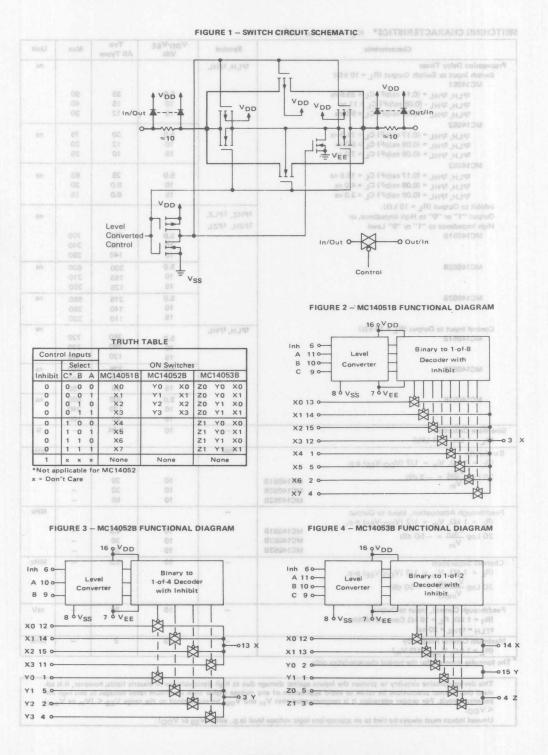
Characteristic	Symbol	VDD-VEE	Typ All Types	Max	Unit
Propagation Delay Times Switch Input to Switch Output (R _L = 10 kΩ) MC14051	tPLH, tPHL				ns
tp: u tpu; = (0.17 ns/pF) C; + 26.5 ns		5.0	35	90	
tpLH, tpHL - (0.08 ns/pF) CL + 11 ns	ogv —	10	15	40	17.7
tpLH, tpHL = (0.06 ns/pF) CL + 9.0 ns MC14052		15	Ohn 12	30	
tpLH, tpHL = (0.17 ns/pF) CL + 21.5 ns		5.0	30	75	ns
tpLH, tpHL = (0.08 ns/pF) CL + 8.0 ns	111	10	12	30	
tpLH, tpHL = (0.06 ns/pF) CL + 7.0 ns MC14053		15	10	25	
tpLH, tpHL = (0.17 ns/pF) CL + 16.5 ns		5.0	25	65	ns
tpLH, tpHL = (0.08 ns/pF) CL + 4.0 ns		10	8.0	20	
tpLH, tpHL = (0.06 ns/pF) CL + 3.0 ns		15	6.0	15	
Inhibit to Output (R _L = 10 kΩ):		H-1004-	 	-	-
Output "1" or "0" to High Impedance, or	tPHZ, tPLZ,	b			ns
High Impedance to "1" or "0" Level	tPZH, tPZL		Level		
MC14051B		5.0	350	700	
ni/out o Out/in	11.13	10	170	340	
경기에 15. 전기하면 이번 50. 하면 되는 그 모으로 보고 있다.	10 10 10 10	15	140	280	
MC14052B	14 - 14 - 11	5.0	300	600	ns
		10	155	310	
		15	125	250	
MC14053B		5.0	275	550	ns
FIGURE 2 - MC140518 FUNCTIONAL DIAGRAM		10	140	280	
		15	110	220	
Control Input to Output (R _L = 10 kΩ)	tPLH, tPHL				ns
MC14051B	,	5.0	360	720	
Stort or years — - 0 a rini	-	10	160	320	
Cities relucional level Level Off A		15	120	240	Cont
MC14052B day		5.0	325	650	ns
	WC14083B	10	130	260	town
Soves 70VE	OX OY O	10	90	180	0
MC14053B	D YD X1	5.0	300	600	ns
	TX TY O		120	240	0
X1 14.00 X1 14.00	lex or r	15	80	160	0
Sine Wave Distortion	IX-07 F	10	0.04	0-1	%
$(R_L = 1 k\Omega, f = 1 kHz)$	1 Y1 X0		9X	1 5 1	0
Bandwidth	BW		NA L		MH
$(R_L = 1 k\Omega, V_{in} = 1/2 (V_{DD} V_{EE}) p-p,$	None	None	None	K H	
30 Lag Vout _ 3 dB)			or NIC 14062	plicable	Not so
$\frac{20 \text{ Log}}{\text{V}_{in}} = -3 \text{ dB}$ MC14051B	THE STATE OF THE S	10	20	- 91 <u>8</u> 0 71	noci =
MC14052B		10	30	-	
MC14053B		10	55		-
Feedthrough Attenuation, Input to Output	7.				МН
$(R_L = 1 \text{ k}\Omega, V_{in} = 1/2 (V_{DD} - V_{EE}) \text{ p-p.}$ 20 Log $\frac{V_{out}}{V_{out}} = -50 \text{ dB}$	MARDAI	LAW TO DAIL	4.5	E BBUO	18
20 Log $\frac{V_{out}}{V_{in}} = -50 \text{ dB}$ MC14052B MC14052B		10	30		
Vin MC14053B		10	55		
Channel Separation		10	3.0		MH
(R ₁ = 1 kQ V ₂ = 1/2 (V ₂ V ₂ V ₂ V ₂ V ₂ V ₃ V ₄		er ytenië	0.0	-	0 8 6
Vout(B)		Popped A to 7	lev tev		001
(R _L = 1 k Ω , V _{in} = 1/2 (V _{DD} V _{EE}) p-p, 20 Log $\frac{V_{out}(B)}{V_{in}(A)}$ = -50 dB)		syigh lobilitie	10770	Com	0 6 8
Feedthrough Control, Input to Output	_	10	30	+	m\
$(R_1 = 1 \text{ k}\Omega, R_L = 10 \text{ k}\Omega \text{ Control/Inhibit}$ $t_{TLH} = t_{THL} = 20 \text{ ns}$			29 A P	88 A P B	0 81
Maximum Control Frequency	C ETO	10	2	-	MH

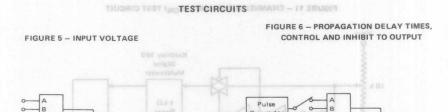
^{*} The formulas given are for the typical characteristics only.

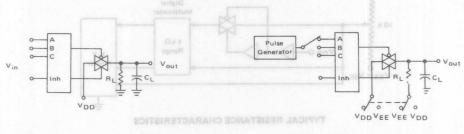
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{EE} \le (V_{in} \text{ or } V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either $V_{\mbox{SS}}$ or $V_{\mbox{DD}}$).









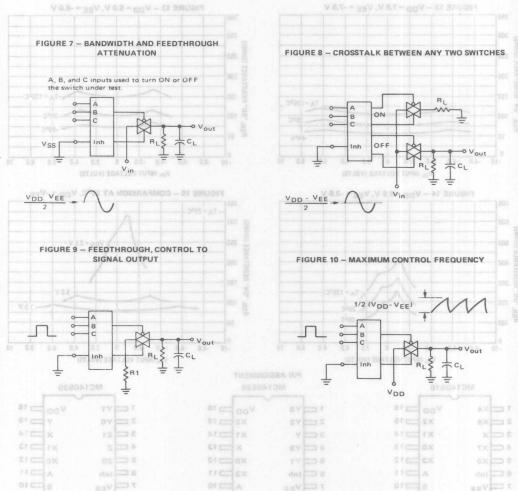
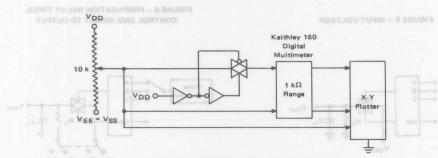
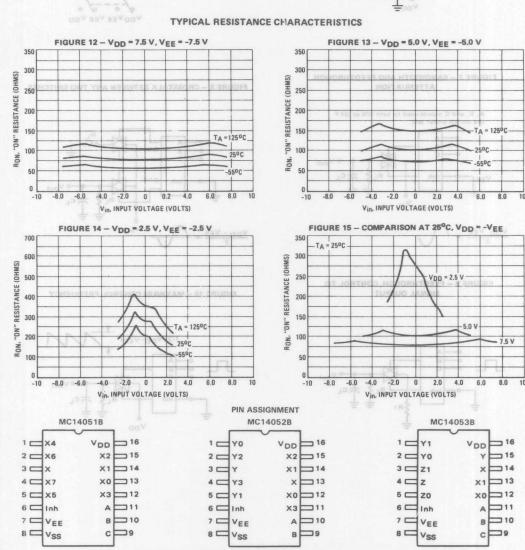


FIGURE 11 - CHANNEL RESISTANCE (RON) TEST CIRCUIT

MC140518°MC140528°MC14053B







MC14060B

Advance Information

14-BIT BINARY COUNTER AND OSCILLATOR

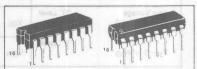
The MC14060B is a 14-stage binary ripple counter with an cn-chip oscillator buffer. The oscillator configuration allows design of either RC or crystal oscillator circuits. Also included on the chip is a reset function which places all outputs into the zero state and disables the oscillator. A negative transition on Clockin will advance the counter to the next state. Schmitt trigger action on the input line permits very slow input rise and fall times. Applications include time delay circuits, counter controls, and frequency dividing circuits.

- Fully Static Operation
- Quiescent Current = 5.0 nA/Package Typical @ 5 V
- Noise Immunity = 45% of VDD Typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 V to 18 V
- Capable of Driving Two Low-Power TTL Loads, One Low-Power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range
- Low Input Capacitance = 5.0 pF Typical
- Buffered Outputs Available from Stages 4 Through 10 and 12 Through 14
- Common Reset Line
- 17 MHz Typical Counting Rate @ VDD = 15 V
- Pin-for-Pin Replacement for CD4060B

CMOS MSI

(LOW POWER COMPLEMENTARY MOS)

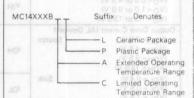
14-BIT BINARY COUNTER
AND OSCILLATOR

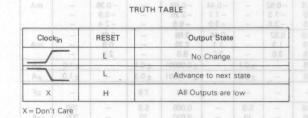


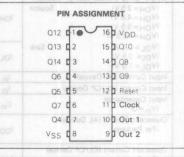
L SUFFIX
CERAMIC PACKAGE
CASE 620

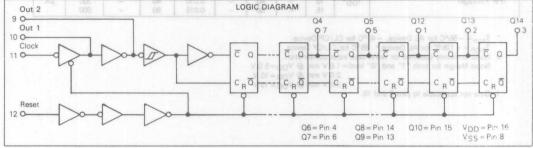
P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION









This is advance information and specifications are subject to change without notice.

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ADI-822

MAXIMUM RATINGS (Voltages referenced to VSS)

Rating	Symbol	Value	Unit
DC Supply Voltage	VDD	-0.5 to +18	V
Input Voltage, All Inputs	Vin	-0.5 to V _{DD} +0.5	٧
DC Current Drain per Pin	1	10	mA
Operating Temperature Range — AL Device CL/CP Device	TA	- 55 to + 125 - 40 to + 85	°C
Storage Temperature Range	T _{stg}	-65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leqslant (V_{in})$ or Vout) ≤ VDD.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD).

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	VDD		w*291 6	chib is	25°C	Also inclu	Thi	Unit	
Characteristic	Symbol	V	Min	Max	Min	Тур	Max	Min	Max	Onit
Output Voltage ''0' Level V _{in} = V _{DD} or 0	VOL	5.0 10 15	ve next w input ter con-	0.05 0.05 0.05	e count sermits y cuous	npu o del	0.05 0.05 0.05	on_clod ger <u>a</u> ctior App#caei	0.05 0.05 0.05	BWIEB BIV S
V _{in} = 0 or V _{DD}	Vон	5.0 10 15	4.95 9.95 14.95		4.95 9.95 14.95	5.0 10 15	BINDED I	4.95 9.95 14.95	State Op	VII.V
Input Voltage # "0" Level (V _O = 4.5 or 0.5 V) (V _O = 9.0 or 1.0 V) (V _O = 13.5 or 1.5 V)	VIL	5.0 10 15		1.5 3.0 4.0		2.25 4.50 6.75	1.5 3.0 4.0	=45% or n on All Range=	1.5 3.0 4.0	Nose Vode
(V _O = 0.5 or 4.5 V) (V _O = 1.0 or 9.0 V) (V _O = 1.5 or 13.5 V)	VIH	5.0 10 15	3.5 7.0 11.0	e Low-F	3.5 7.0 11.0	2,75 5.50 8.25	Low-Poy	3.5 7.0 11.0	ale of Driving TILL	Vano Rang
Output Drive Current (AL Device)† (VOH = 2.5 V) Source (VOH = 4.6 V) (VOH = 9.5 V) (VOH = 13.5 V)	ЮН	5.0 5.0 10	-3.0 -0.64 -1.6 -4.2	10 and -	-2.4 -0.51 -1.3 -3.4	-4.2 -0.88 -2.25 -8.8	ole from	-1.7 -0.36 -0.9 -2.4	vatuD ber PL Aguor PERE non	mA
(V _{OL} = 0.4 V) Sink (V _{OL} = 0.5 V) (V _{OL} = 1.5 V)	lor	5.0 10 15	0.64 1.6 4.2	-	0.51 1.3 3.4	0.88 2.25 8.8	for CD4	0.36 0.9 2.4	r-Pio_Rep	mA
Output Drive Current (CL/CP Device): (VOH = 2.5 V) Source (VOH = 4.6 V) (VOH = 9.5 V) (VOH = 13.5 V)	ЮН	5.0 5.0 10 15	-2.5 -0.52 -1.3 -3.6		- 2.1 - 0.44 - 1.1 - 3.0	-4.2 -0.88 -2.25 -8.8	HTURT	- 1.7 - 0.36 - 0.9 - 2.4	=	mA
(V _{OL} = 0.4 V) Sink (V _{OL} = 0.5 V) (V _{OL} = 1.5 V)	lor	5.0 10 15	0.52 1.3 3.6	-	0.44 1.1 3.0	0.88 2.25 8.8	-	0.36 0.9 2.4		mA
nput Current (AL Device)	lin	15		±0.1		±0.00001	±0.1		±1.0	μΑ
Input Current (CL/CP Device)	lin	15	-	±0.3	txea of	±0.00001	±0.3	. =	±1.0	μА
nput Capacitance (V _{in} = 0)	Cin	-	, -	-wo	916-0100	5.0	7.5	+1	-	pF
Quiescent Current (AL Device) (Per Package)	IDD	5.0 10 15	-	5.0 10 20	Ξ	0.005 0.010 0.015	5.0 10 20	-	150 300 600	μΑ
Quiescent Current (CL/CP Device) (Per Package)	IDD	5.0 10 15	MARG	20 40 80	01	0.005 0.010 0.015	20 40 80	-	150 300 600	μΑ

T_{IOW} = -55°C for AL Device, -40°C for CL/CP Device.
 Thigh = +125°C for AL Device, 85°C for CL/CP Device.
 Noise immunity specified for worst-case input combination.

3-142

Noise Margin for both "1" and "0" level = 1.0 V min @ VDD = 5.0 V 2.0 V min @ V_{DD} = 10 V 2.5 V min @ V_{DD} = 15 V

[†] Data not applicable to pins 9 and 10.

SWITCHING CHARACTERISTICS (C₁ = 50 pF, T_A = 25°C)

Characteristic	Symbol	V _{DD} Vdc	Min	Тур	Max	Unit
Output Rise Time (Counter Outputs)	tTLH	5.0 10 15	Î	40 25 20	200 100 80	ns
Output Fall Time (Counter Outputs)	tTHL	5.0 10 15	0 10 	50 30 20	200 100 80	ns
Propagation Delay Time Clock _{in} to Q4	tPLH tPHL	5.0 10 15	-	415 175 125	740 300 200	ns
CHARACTERISTICS PRODUCT AND OF 10 AN	SCILLATOR	5.0 10 15	TYP	1.5 0.7 0.4	2.7 1.3 - 1.0	μS
Clock Pulse Width	twH	5.0 10 15	100 40 30	65 30 20	-	ns
Clock Pulse Frequency	fφ	5.0 10 15	181-00	5 14 17	3.5 8 12	мна
Clock Rise and Fall Time	tTLH tTHL	5.0 10 15	V 0.1	No Limit		0
Reset Pulse Width	t _W	5.0 10 15	120 60 40	40 15 10	-	ns
Propagation Delay Time Reset to Qn	tPHL	5.0 10 15	17 ,01-ggr 6 or 17 -pgr 8 st 5	170 80 60	360 160 100	ns

FIGURE 1 — POWER DISSIPATION TEST CIRCUIT

AND WAVEFORM

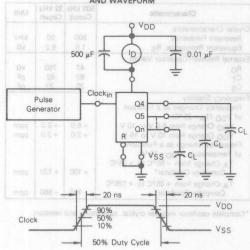
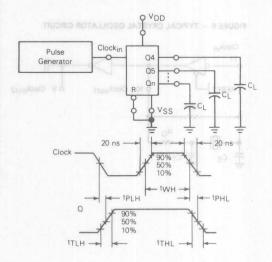


FIGURE 2 — SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



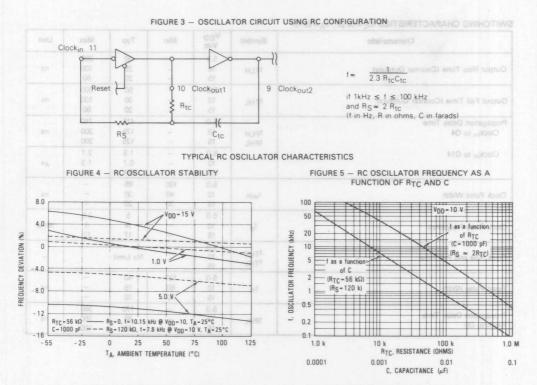


FIGURE 6 - TYPICAL CRYSTAL OSCILLATOR CIRCUIT

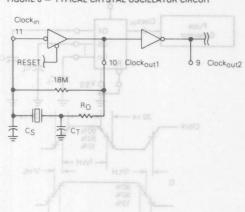


FIGURE 7 - TYPICAL DATA FOR CRYSTAL OSCILLATOR CIRCUIT

Characteristic	500 kHz Circuit	32 kHz Circuit	Unit
Crystal Characteristics Resonant Frequency	500	50	kHz
Equivalent Resistance, RS	1.0	6.2	kΩ
External Resistor/Capacitor Values	- and 000		H
Ro	47	750	kΩ
CT	82	82	pF
CS	20	20	pF
Frequency Stability	100	notris	
Frequency Changes as a Function of V _{DD} (T _A = 25°C)		1018190	
VDD Change from 5.0 V to 10 V	+6.0	+2.0	ppm
V _{DD} Change from 10 V to 15 V Frequency Change as a Function of Temperature (V _{DD} = 10 V) T _A Change from −55°C to +25°C	+2.0	+ 2.0	ppm
Complete Oscillator*	+ 100	+ 120	ppm
TA Change from +25°C to +125°C Complete Oscillator*	- 160	- 560	ppm

^{*}Complete oscillator includes crystal, capacitors, and resistors.



QUAD ANALOG SWITCH/QUAD MULTIPLEXER

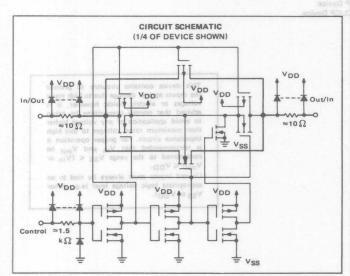
The MC14066B consists of four independent switches capable of controlling either digital or analog signals. This quad bilateral switch is useful in signal gating, chopper, modulator, demodulator and CMOS logic implementation.

The MC14066B is designed to be pin-for-pin compatible with the MC14016B, but has much lower ON resistance. Input voltage swings as large as the full supply voltage can be controlled via each independent control input.

- High On/Off Output Voltage Ratio 65 dB typical
- Quiescent Current = 0.5 nA/package typical @ 5 Vdc
- Low Crosstalk Between Switches -50 dB typical @ 8 MHz
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Transmits Frequencies Up to 65 MHz @ 10 Vdc
- Linearized Transfer Characteristics, △RON <60 Ω for $V_{in} = V_{DD}$ to V_{SS} (at 15V) Low Noise $-12 \text{ nV}/\sqrt{\text{Cycle}}$, $f \ge 1 \text{ kHz typical}$
- Pin-for-Pin Replacement for CD4016, CD4066, MC14016

MAXIMUM RATINGS (Voltages referenced to VSS)

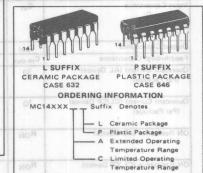
80 Rating 082 08	Symbol	Value	Unit
DC Supply Voltage	VDD	-0.5 to +18	Vdc
Input Voltage, All Inputs	Vin	-0.5 to V _{DD} + 0.5	Vdc
Through Current		25	mAdc
Operating Temperature Range — AL Device CL/CP Device	TA	-55 to +125 -40 to +85	°C
Storage Temperature Range	T _{stg}	-65 to +150	°C

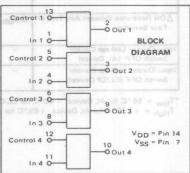


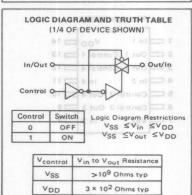


(LOW-POWER COMPLEMENTARY MOS)

QUAD ANALOG SWITCH QUAD MULTIPLEXER





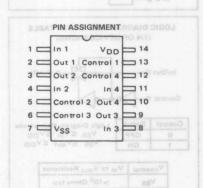


7	7	Г	ч	
	ρ	۰	а	
	ь	w	э	

		VDD	T _{low} *		25°C			This		
Characteristic	Symbol	Vdc	Min	Max	Min	Тур	Max	Min	Max	Unit
Input Voltage (Control) "0" Level	VIL									Vdc
(V _O = 4.5 or 0.5 Vdc)		5.0	-	1.5	-	2.25	1.5	-	1.5	
(VO = 9.0 or 1.0 Vdc)		10	-	3.0	-	4.50	3.0	-	3.0	
(VO = 13.5 or 1.5 Vdc)		15	(Take	3.75	INTO A	6.75	3.75	1.15.000	3.75	
"1" Level	VIH		Trans.	10.16.0	201 102	la min				Vdc
(Vo = 0.5 or 4.5 Vdc)	.0	5.0	3.5	gorlatiwa	3.5	2.75	do Essiau	3.5	HOM WICH	
(VO = 1.0 or 9.0 Vdc)	100	10	7.0	talie bau	7.0	5.50	ne ao lei	7.0	e gailion	noo
(V _O = 1.5 or 13.5 Vdc)		15	11.25	болав	11.25	8.25	do v enim	11.25	ni -lutes	la la
Input Current (AL Device) Control	lin	15	-	± 0.1	-	±0.00001	± 0.1	nen+eiqm	±1.0	μAdc
nput Current (CL/CP Device) Control	lin	15	rit Hiws	±0.3	o rig-10	±0.00001	±0.3	1) 4) 2000	±1.0	μAdc
Input Capacitance	Cin		nga swing	iov Juga	0.83763	8001 1/20 16	ועכוז וטעו	1 3 6 C) THE	- UTUB.	pF
$(V_{in} = 0)$			sach inda	siv ballo	ningo s	tage can b	lov ylag	e full s	1 35 AGN	56
Control Input	330		-	-	-	5.0	7.5	hugei los	trice their	neq
Switch Inputs		10	-	Tealo	or 8th 81	8.0	15 V	gtgO H	XnO rigil	
Output Capacitance	Cout	10	-	5 Vite.	8 lebigs	13.0	- 0.5 nA	เกราะเวิ	meneral	pF
Feedthrough Capacitance	C _{in-out}	10	- 214	A 8-0 hs	dB-typi	0.5	(w8-nsev	talk Bet	teoral wo	pF
Quiescent Current (AL Device)	10	5.0		0.25	-	0.0005	0.25	sctien o	7.5	μAdc
(Per Package)	CERA	10	-	0.50	StoV	0.0010	0.50	aFl-sparl	V 15000	0 .
SAS SEAS SUBSECTION OF SEAS	1	15	-	1.00	NV OF G	0.0015	1.00	nsupper 3	30	0
Quiescent Current (CL/CP Device)	- la	5.0	-	1.0	8>7/10	0.0005	1.0	Transfe	7.5	μAdc
(Per Package)	ATTEC TO	10	-	2.0	-	0.0010	2.0	/ 07 00	15 V	
		15	-	4.0	minion v	0.0015	4.0	/o 51 -	30	10
ON Resistance (AL Device)	RON	5.0	- 80	800	8010	250	1050	Restand	1200	52
A Extended Operating	0	10	-	400	-	120	500	-	520	
Temperature Range		15	-	220	-	80	280		300	-
ON Resistance (CL/CP Device)	RON	5.0	-	880	-	250	1050	-	1300	52
	-	10	-	450	- 18	120	500	IGN TAO	550	HIMBK
		15		250	100mm	80	280	Patien	320	
△ON Resistance Between Any Two of	ARON	5.0	-814	os 8:0-	Tod'	25	-	-	ogsatoly	25
Four Switches	0.0	10	18.0 + 6	0.5 to Vn	- v	10	-	- 870	onl TIA as	wieV z
		15	10.0 7 6	0100	01.0	5.0		-	1000	27 (1906)
Input/Output Leakage Current	- 1	15	1	±100	-	± 0.01	± 100		±1000	nAdc
Switch OFF (AL Device)	Contri	30	125	01 68-	B	3.6.	anversi 22)	and agreem a		20136
Input/Output Leakage Current Switch OFF (CL/CP Device)	-	15	180	±300	073	± 0.01	± 300	agnal	±1000	nAdc

 $^*T_{low} = 55\,^\circ\text{C}$ for AL Device, $-40\,^\circ\text{C}$ for CL/CP Device. $T_{high} = +125\,^\circ\text{C}$ for AL Device, $+85\,^\circ\text{C}$ for CL/CP Device.

-- 0 E n1



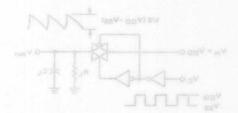
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range V_{SS} < (V_{in} or V_{out}) < V_{DD}. Vout) < VDD.

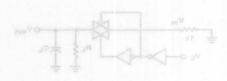
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD).

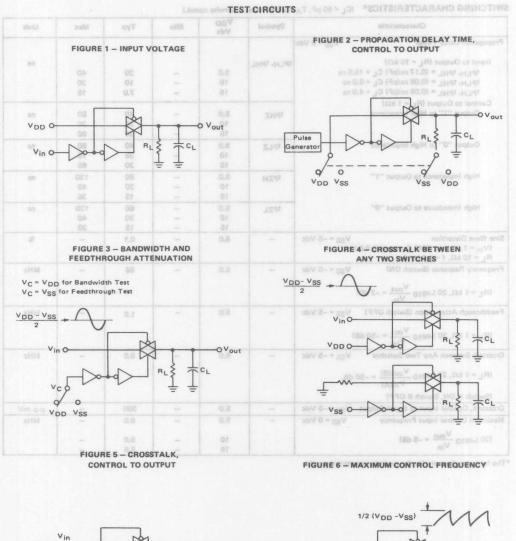
SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C unless otherwise noted.)

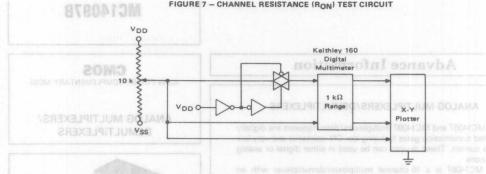
Characteristic	Symbol	V _{DD} Vdc	Min	Тур	Max	Unit
Propagation Delay Times VSS = 0 Vdc			204210	is account to	Note and the	
CONTROL TO OUTPUT			392111	V TURNI — I	3710017	
Input to Output (R _L = 10 kΩ)	tPLH, tPHL					ns
tpLH, tpHL = (0.17 ns/pF) CL + 15.5 ns		5.0	-	20	40	
tpLH, tpHL = (0.08 ns/pF) CL + 6.0 ns		10	-	10	20	
tpLH, tpHL = (0.06 ns/pF) CL + 4.0 ns		15	-	7.0	15	
Control to Output (R _L = 1 kΩ)						
Output "1" to High Impedance	tPHZ	5.0	-	40	80	ns
		10		35	70	OggV
D木 3 N 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1		15	- 1	30	60	
Output "0" to High Impedance	tPLZ	5.0	の本 多	40	80	ns
	and the second	10	- 7	35	70	O MY
	Carlotte Silver	15	* =	30	60	
High Impedance to Output "1"	tPZH	5.0	-	60	120	ns
gay asy gay		10	_	20	40	
		15		15	30	7 16 1
High Impedance to Output "0"	tPZL	5.0	-	60	120	ns
	1.22	10	-	20	40	
		15	-	15	30	
Sine Wave Distortion VSS = -5 Vdc	-	5.0	-	0.1	_	%
(Vin = 1.77 Vdc, RMS Centered @ 0.0 Vdc,			OWA HTO	WIGHAR - E	FIGURE	
$R_L = 10 \text{ k}\Omega$, $f = 1.0 \text{ kHz}$			MOITAUM	FITA POUD	HKTQ333	
requency Response (Switch ON) VSS = -5 Vdc	-	5.0	-	65	-	MHz
	αV				for Bandwid	Ver Voc
$(R_L = 1 k\Omega, 20 Log_{10} \frac{V_{out}}{V_{c}} = -3 dB)$					for Paedthros	
V _{in}						
Feedthrough Attenuation (Switch OFF) VSS = -5 Vdc	_	5.0	_	1.0	(2)	MHz
O Ally				1.0	1-1-	257 007
$(R_L = 1 \text{ k}\Omega, 20 \text{ Log}_{10} \frac{V_{\text{out}}}{V_{\text{in}}} = -50 \text{ dB})$					~	
Vin 30 db/						1.3 %
Crosstalk Between Any Two Switches Vss = -5 Vdc	_	5.0	7 -1 7	8.0		MHz
		0.0	1 1	0.0		101112
$(R_L = 1 \text{ k}\Omega, 20 \text{ Log}_{10} \frac{\text{Vout}(B)}{\text{Vin}(A)} = -50 \text{ dB},$		10	平 美山田			
Vin(A)			1 1	1	V 1.	v
(Switch A ON, Switch B OFF)	F 10.		= =		10	
Crosstalk, Control Input to Signal Output VSS = -5 Vdc	-	5.0	-	300	-0.7	p-p mV
Maximum Control Input Frequency VSS = 0 Vdc	-	5.0	-	6.0	-	MHz
$(20 \text{ Log}_{10} \frac{V_{\text{out}}}{V_{\text{out}}} = -6 \text{ dB})$		10	-	8.0	-	
Vin		15	_	8.5		

^{*}The formulas given are for the typical characteristics only.

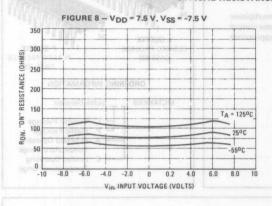


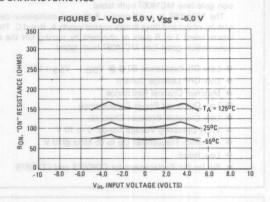


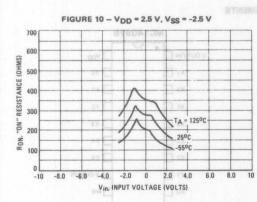


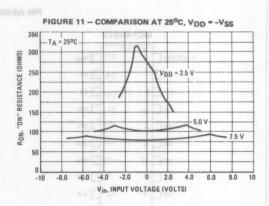


TYPICAL RESISTANCE CHARACTERISTICS









MC14067B MC14097B

MICTAUSES

Advance Information

FIGURE 7 - CHANNEL RESISTANCE (ROM) TEST CIRCUIT

ANALOG MULTIPLEXERS/DEMULTIPLEXERS

The MC14067 and MC14097 multiplexers/demultiplexers are digitally controlled transmission gates featuring low ON resistance and very low leakage current. These devices can be used in either digital or analog applications.

The MC14067 is a 16-channel multiplexer/demultiplexer with an inhibit and four binary control inputs A, B, C and D. These control inputs select 1-of-16 channels by turning ON the appropriate transmission gate (see MC14067 truth table).

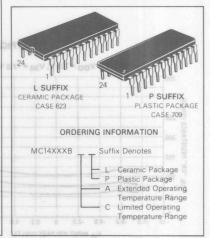
The MC14097 is a differential 8-channel multiplexer/demultiplexer with an inhibit and three binary control inputs A, B and C. These control inputs select 1 of 8 pairs of channels by turning ON the appropriate transmission gates (see MC14097 truth table).

- Low ON Resistance: 80 Ω @ V_{DD} V_{SS} = 15 V
- Low OFF Leakage Current
- Matched Channel Resistance
- Low Quiescent Power Consumption
- Low Crosstalk Between Channels
- Wide Operating Voltage Range: 3 to 18 V
- Transmits Frequencies Up to 65 MHz @10 V
- Low Noise
- Pin for Pin Replacement for CD4067B and CD4097B

CMOS

(LOW-POWER COMPLEMENTARY MOS)

ANALOG MULTIPLEXERS/ DEMULTIPLEXERS



PIN ASSIGNMENTS FIGURE 10 - VOO = 2.5 V, VSS = -2.5 V MC14067B MC14097B X OUT / IN □ V_{DD} 23 X8 YO] Y1 22 X9 X6 Y2 2(X10 X5 LO X11 X4 Y3 19 X12 X3 🗍 74 18 X13 X2 Y5 X1 [YOUT/IN X1 5 10 X15 xo 🗌 7-Y6 IS INHIBIT A Y7 В С 13 0 VSS [VSS [INHIBIT

ADI-919

MAXIMUM RATINGS Symbol Value -0.5 to +18DC Supply Voltage VDD-VSS Input Voltage, All Inputs 0.5 to VDD + 0.5 25 Through Current TA Operating Temperature Range - AL Device -55 to +125 CL/CP Device -40 to +85Tstg Storage Temperature Range -65 to +150°C

Selected Control Inputs Inh Channel None X 0 0 0 XO 0 0 0 X1 0 0 X2 0 0 X3 0 0 X4 X5 X6 X7 0 0 X8 0 0 X9 XO 0 X1 0 0 X2 0 X3 0 0 0 X4 X5

MC14067 TRUTH TABLE

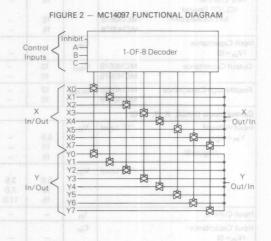
Control Inputs В C Channels A Inh X None 0 0 0 0 XO YO X1 Y1 0 0 0 0 0 0 X2 Y2 1 0 0 X3 Y3 0 X4 Y4 0 0 0 0 X5 Y5 X6 Y6 X7 Y7 0 0 0

MC14097 TRUTH TABLE

X = Don't Care

FIGURE 1 - MC14067 FUNCTIONAL DIAGRAM A-B-Control 1-OF-16 Decoder Inputs X3 X4 X5 -X6 -X X7 -In/Out Out/In X9 X10 X11 -

X12 X13



3-151

	CHARACTERISTICS

ELECTRICAL CHARACT			V	т.	*	168	ATAR M	UIVIDAN	-	4	
Characteries	line Unit	Cumbal	VDD	Min	*w	Rabing	25°C	May	Min	gh*	Unit
Characterist	Y Y 1 01 1 W	Symbol	ZZ V GO	Min	Max	Min	Тур	Max	IVIII	Max	Unit
Channel Inputs (Vin) and C	7 1 2 2 2 3 1 1	-0.5 to	Vin			Strik	1	stloV Jugn			
Output Voltage	"0" Level	VOL	5.0	-	0.05	-	0	0.05	-	0.05	V
V _{in} = 0 V		-55 p	10 15	_ 80	0.05	egngR es	0	0.05		0.05	
	d8+ 0	06		-		-					
N/ N	"1" Level	VOH	5.0	4.95	-	4.95	5.0	Storage Tr	4.95	-	V
$V_{in} = V_{DD}$			10	9.95		9.95 14.95	10 15		9.95	_	
Quiescent Current (AL De	unal .	le e	5.0	-	5.0	14.00	0.005	5.0	-	150	^
(Per Package)	vicei	IDD	10		10		0.005	10		300	μΑ
			15		20	_	0.015	20 7	ME140	600	1488
Quiescent Current (CL/CP	Device)	IDD	5.0	_	20		0.005	20		150	μΑ
(Per Package)			10		40	-	0.010	40	_	300	μΑ
Selected			15	_	80	Supe	0.015	80	Contra	600	
Total Supply Current**†		J IT	5.0		Hon	T = (0.07)	7 μA/kHz)	f + Inn			μА
(Dynamic plus Quiescen	t,	X I	10				μA/kHz)	f + IDD			
Per Package)		15			IT = (0.36	$\mu A/kHz$				HAR	
ON Resistance (AL Device	0 1	RON	5.0		880	- 1	250	1050		1200	Ω
(Figure 9)		7	10	-	400	-	120	500	+	550	
AY AX 0		0	0 15	-	220	+ 1	80	280	-	320	
ON Resistance (CL/CP De	vice)	RON	5.0	-	880	- 1	250	1050	-	1200	Ω
(Figure 9)			0 10	-	450	4	120	500	-	520	
0 X XX Y			15	-	250	1	80	280	1	300	
ON Resistance Between	Any	- RON	5.0	-		1 -	25	- 1	-	-	Ω
Two Channels			10	-	-		10	1 -	-		
			15		7		5.0				
OFF Channel Leakage Cur	rent	-									nA
Any Channel (AL Device) All Chann	and OFF.		25	-	100		± 0.01	100	1 7		- 9
TAL Devicer All Chan	MC14067B		15		100		± 0.08	100			
	MC14097B		15		100		± 0.04	100			
OFF Channel Leakage Cur	rent										nA
Any Channel	rent		15	_	1000		± 0.01	1000	_	_	116
(CL/CP Device)			in.			nanana.		e avaria es	harner	a nauna	
All Channels OFF:	MC14067B		15		1000	MARGA	± 0.08	1000	- MC140	A SUDIE	10.0
	MC14097B		15	-	1000		± 0.04	1000		thetadol >	
Input Capacitance		Cin	lantne							A	pF ₀
$(V_{in}=0)$	1-0F-8 Dec	-8	7 - studio	-	-	-	5.0	1-0 <u>E</u> -18	- [8 - (arugni
Output Capacitance	MC14067B	Cout	10	-	-	-	60	-		0 - 1	pF
	MC14097B		10	-	-		32	+		-	
Feedthrough Capacitance	MC14069B	Cin-out	10	-	- F		0.18	11+11	1,50	- OX	pF
	MC14067B	To a	10	-	- [0.12		do a	- !X	
Control Inputs (Inhibit, A,	B, C, D)				+						
Input Voltage#	"0" Level	VII	T describe					- in the		- BX	V
$V_{in} = V_{DD}$			5.0	-	1.5		2.25	1.5		1.5	×
(Figure 5)		AL AN	10		3.0		4.50	3.0	-	3.0	tu@\ni
ii igai o a		T-W	15	- "	4.0		6.75	4.0	-	4.0	
	"1" Level	VIH			-		10			- 00X	V
		- BY	5.0	3.5	- 1	3.5	2.75	-	3.5	E SEX	May -
		ay	10 15	11.0		11.0	5.50 8.25	-	11.0	- EIX	THE ST
1		-67			-	11.0		-	11.0	部分	- ^
Input Current		lin	-	-	-	-	10	-	-		рА
Input Capacitance		Cin				1					pF
$(V_{in} = 0)$			_	-	_	-	5.0	-	-	-	

^{*} T_{low} = -55°C for AL Device, -40°C for CL/CP Device. T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

*Noise immunity is defined as the control input voltage coincident with the specified change, $\Delta \dot{V}_{OUt}$, at an output in the OFF state.

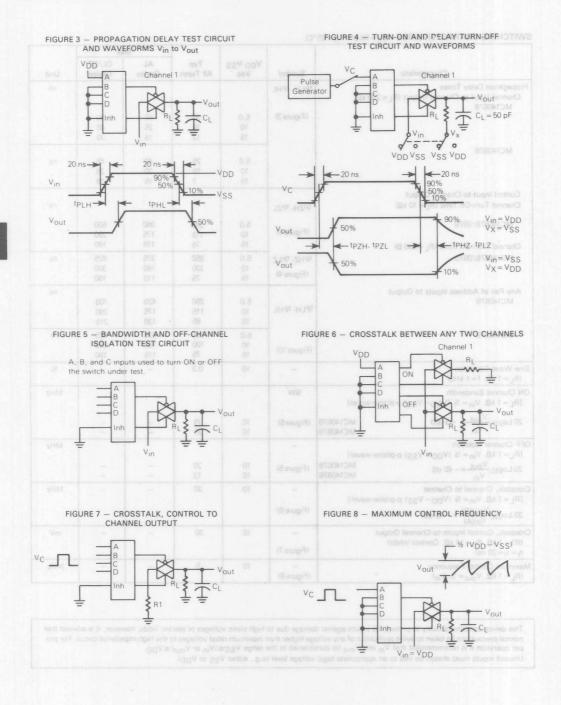
**The formulas given are for the typical characteristics only at 25°C.

[†]Total Supply Current, I_T, is the current drawn at device terminals V_{DD} and V_{SS} for total current through the device. The channel component, (Vin-Vout)/RON, should not be included.

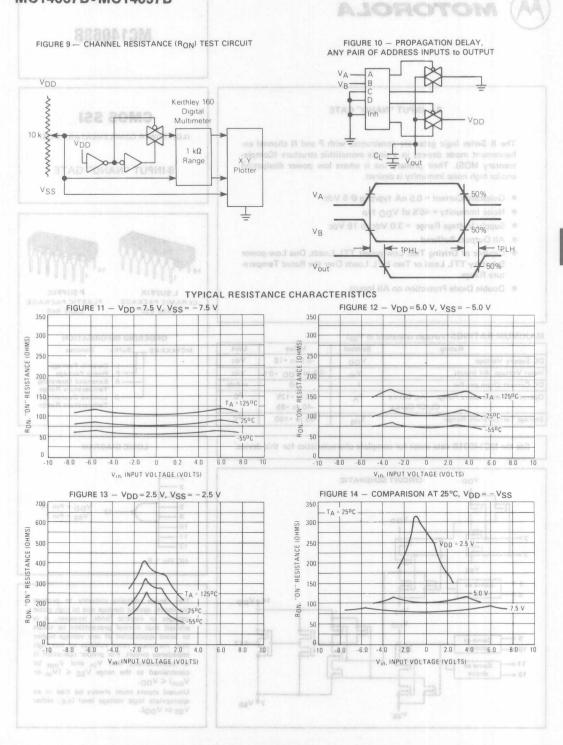
SWITCHING	CHARACTERISTICS	$(C_1 = 50 \text{ pF})$	$T_A = 25^{\circ}C$

			tuo V ot	WA SHARE	Max	
Characteristic	Symbol	V _{DD} -V _{SS} Vdc	Typ All Types	AL Device	CL/CP Device	Unit
Propagation Delay Times	tPLH, tPHL				8-	ns
Channel Input-to-Channel Output (R _L = 200 kΩ)			suoV-9-9			
MC14067B	(5:		1 2	199		
HI \$ CL = 50 pf	(Figure 3)	5.0	35	55 25	90	
= v = nive ====================================		10 15	15	18	30	
0 9-0-9		10	12	10	- 50	-
MC14097B		5.0	25	40	65	ns ns
		10	10	20	25	05 115
<-20 ns → <-20 ns	-	15	7	15	18	V _{in}
Control Input-to-Channel Output	DV .	22	/001_4		1	
Channel Turn-On Time ($R_1 = 10 \text{ k}\Omega$)	tPZH, tPZL		-109 14	Hard -	4 14-11	ns
anV = V see I	PZH, PZL		1		V	
MC14067B/097B	(F)	5.0	240	260	600	tuo's
No. of the second	(Figure 4)	10	115	175	290	100
Channel Turn-Off Time (R _L = 300 Ω)	*	15	75	115	190	
MC14067B/097B	tPHZ, tPLZ	5.0	250	375	625	ns
QQV=XV %0L	(Figure 4)	10	120	180	300	
	, iguio ii	15	75	115	190	
Any Pair of Address Inputs to Output	RU LY ST					ns
MC14067B	tPLH, tPHL	5.0	280	420	700	
	T CITY THE	10 15	115 85	175	290 215	
A STATE OF THE PROPERTY OF TAXABLE PARTY.	lane.					501 (200)
MC14097B WT YMA MEEWTER AUATZEORD - 8 SR	John	5.0	250 100	375 150	020	BUDINS
	(Figure 10)	10 15	75	115	190	
Sine Wave Distortion	-	10	0.3	- 1281	Sylicit dedict	%
$(R_L = 1 k\Omega, f = 1 kHz)$						
ON Channel Bandwidth	BW					MHz
[R _L = 1 k Ω , V _{in} = ½ (V _{DD} - V _{SS}) p-p(sine-wave)]				XI I	9-	
20 Log10 Vout = -3 dB) MC14067B	(Figure F)	10	15		- Common of the	
$20 \text{ Log}_{10} \frac{V_{\text{out}}}{V_{\text{in}}} = -3 \text{ dB}$ MC14067B MC14097B		10	25		dol	
OFF Channel Isolation		10	20	- Los		NAL I-
[R _L = 1 k Ω , V _{in} = ½ (V _{DD} - V _{SS}) p-p(sine-wave)]				neV		MHz
20 Logge Vout - 40 dB MC14067B	(Figure 5)	10	20	_	1 -	
$20 \text{ Log}_{10} \frac{V_{\text{out}}}{V_{\text{in}}} = -40 \text{ dB}$ MC14067B MC14097B		10	12	-	-	
Crosstalk, Channel to Channel	-	10	20	_	_	MHz
$[R_L = 1 k\Omega, V_{in} = \frac{1}{2} (V_{DD} - V_{SS}) p-p(sine-wave)]$						
$20 \text{ Log}_{10} \frac{V_{\text{out}(B)}}{V_{\text{in}(A)}} = -40 \text{ dB}) \text{ MUMIXAM} - 8 380203$	(Figure 6)		ON JORTHO	SSTALK, C	JRE 7 - CRD	DFI
			1	עבן סעדפעו	CHABI	
Crosstalk, Control Inputs-to-Channel Output	-	10	30	-	-	mV
$(R1 = 1 kΩ, R_L = 10 kΩ, Control/Inhibit$	(Figure 7)				A	
$t_f = t_f = 20 \text{ ns}$	i igure //			-	8	-17
Maximum Control Frequency		10	5	05	3=	MHz
$(R_L = 1 k\Omega, V_{out} = ½ V_{in})$	(Figure 8)		1.5	MA		

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).



MC14067B•MC14097B



MC14068B

8 - INPUT "NAND" GATE

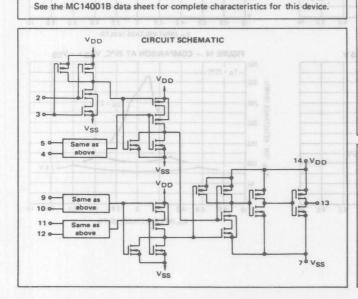
The B Series logic gates are constructed with P and N channel enhancement mode devices in a single monolithic structure (Complementary MOS). Their primary use is where low power dissipation and/or high noise immunity is desired.

- Quiescent Current = 0.5 nA typ/pkg @ 5 Vdc
- Noise Immunity = 45% of VDD typ
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range.
- Double Diode Protection on All Inputs

MAXIMUM RATINGS (Voltages referenced to VSS)

Rating	Symbol	Value	Unit	
DC Supply Voltage	VDD	-0.5 to +18	Vdc	
Input Voltage, All Inputs	Vin	-0.5 to V _{DD} +0.5	Vdc	
DC Current Drain per Pin		10	mAdo	
Operating Temperature Range - AL Device CL/CP Device	TA	-55 to +125 -40 to +85	°C	
Storage Temperature Range	T _{stg}	-65 to +150	°C	

orage remperature mange



CMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

8-INPUT "NAND" GATE



L SUFFIX CERAMIC PACKAGE CASE 632 P SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION MC14XXXB ___ Suffix Denotes

KB Suffix Denotes

L Ceramic Package
P Plastic Package
A Extended Operating
Temperature Range
C Limited Operating
Temperature Range

LOGIC DIAGRAM

2 3 4 5 9 13 V_{DD} = Pin 14 V_{SS} = Pin 7

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in})$ or $V_{out} \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or V_{DD}).

3



MC14069UB

HEX INVERTER

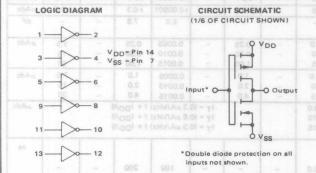
The MC14069UB hex inverter is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These inverters find primary use where low power dissipation and/or high noise immunity is desired. Each of the six inverters is a single stage to minimize propagation delays.

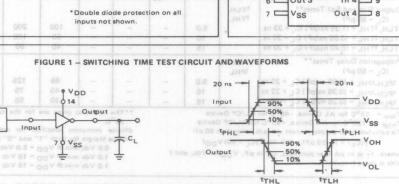
- Quiescent Current = 0.5 nA typ/pkg @ 5 Vdc
- Noise Immunity = 45% of VDD typ
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-Power TTL Loads,
 One Low-Power Schottky TTL Load or Two HTL Loads
 Over the Rated Temperature Range
- Double Diode Protection on All Inputs
- Pin-for-Pin Replacement for CD4069UB
- Meets JEDEC UB Specifications

MAXIMUM RATINGS (Voltages referenced to VSS)

Pulse

Rating	Symbol	Value	Unit	
DC Supply Voltage	V _{DD} -0.5 to +18		Vdc	
Input Voltage, All Inputs BB.0-	Vin	-0.5 to V _{DD} + 0.5	Vdc	
DC Current Drain per Pin - 35.5-	1.7-	- 10 6.1-	mAdc	
Operating Temperature Range — AL Device CL/CP Device	TA	-55 to +125 -40 to +85	°C	
Storage Temperature Range	T _{stg}	-65 to +150	°C	





CMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

HEX INVERTER



L SUFFIX CERAMIC PACKAGE CASE 632 P SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

MC14XXXUB Suffix Denotes

L Ceramic Package
P Plastic Package
A Extended Operating
Temperature Range
C Limited Operating
Temperature Range

MOTOROLA

ELECTRICAL CHARACTERISTICS

		VDD	Tio	w*		25°C		Thi	gh °	0.00
Characteristic	Symbol	ool Vdc	Min	Max	Min	Тур	Max	Min	Max	Unit
Output Voltage "0" Level	VOL	5.0	-	0.05	-	0	0.05	-	0.05	Vdc
Vin VDD or 0		10	-	0.05	-	0	0.05	-	0:05	
		15	-	0.05	-93	TROVA	0.05	-	0.05	
"1" Level	Vон	5.0	4.95	_	4.95	5.0	_	4.95	_	Vdc
V:- 0 or VDD		10	9.95	SOW W	9.95	10	nevni xe	9.95	MC14	
WPOWER COMPLEMENTARY MUST	0.37	15	14.95	single r	14.95	15000	i ingmed	14.95	N c <u>h</u> ann	bes
nput Voltage# "0" Level	VIL		BWOG W	N SISHN	850 A	86113Q DA	W 218715	htsi 18591	1 ,9101	Vdc
(V _O = 4.5 Vdc)	1.	5.0	of the sa	1.0	is desire	2.25	1.0	out To/pe	1.0	dissi
(VO = 9.0 Vdc)		10	-	2.0	noimes	4.50	2.0	ete algni	2.0	evni
(V _O = 13.5 Vdc)		15	-	2.5	14.5	6.75	2.5		2.5	
"1" Level	VIH				1000			THE STATE OF	11111111111	
(VO = 0.5 Vdc)	-111	5.0	4.0	_	4.0	2.75	V to Me	4.0	Many asso	Vdc
(V _O = 1.0 Vdc)		10	8.0	_	8.0	5.50	0.E = epr	8.0	pV vladi	8 0
(V _O = 1.5 Vdc)		15	12.5		12.5	8.25	vo.Low1	12.5	to eldage	0 0
Output Drive Current (AL Device)	lau	1	200	BAIR	W 1 10 0	0.20	изтоные	199V G 19-VA	SJ ent	mAd
(V _{OH} = 2.5 Vdc) Source	ЮН	5.0	-3.0	_	-2.4	-4.2	[emperat	-1.7	ds та <u>ч</u> О	MAG
(V _{OH} = 4.6 Vdc)		5.0	-0.64		-0.51	-0.88	00 140110	-0.36	iG elduc	0.00
(V _{OH} = 9.5 Vdc)		10	-1.6	_	-1.3	-2.25	ment for	-0.36	ni9-relin	8 0
(Va. 1 = 13 5 Vda)		15	-4.2		-3.4	-8.8	too Hono	-2.4	313-121-11	
		_	-				THE DESIGNATION OF THE PERSON	_	Udi. 7185	0 -1
(V _{OL} = 0.4 Vdc) Sink	IOL	5.0	0.64	-	0.51	0.88	-	0.36		mAd
(V _{OL} = 0.5 Vdc)		10	1.6	-	1.3	2.25	tages rates	0.9	MEATH	UNITX
(V _{OL} = 1.5 Vdc)		15	4.2		3.4	8.8	-	2.4		
Output Drive Current (CL/CP Device)	10Н	-shit	32.7	W20.	- War			-	-	mAd
(V _{OH} = 2.5 Vdc) Source		5.0	-2.5		-2.1	-4.2	-	-1.7	284TR0 A	Aiddine
(V _{OH} = 4.6 Vdc)		5.0	-0.52	JA of 9.0	-0.44	-0.88		-0.36	or, All In	rioV tu
(VOH = 9.5 Vdc)		10	-1.3	21 -	-1.1	-2.25	-	-0.9	Drain per	Carron
(V _{OH} = 13.5 Vdc)		15	-3.6	01.65	-3.0	-8.8	ALTDaws	-2.4	ota (allinos	-
(VOL = 0.4 Vdc) Sink	IOL	5.0	0.52	or 62-	0.44	0.88	/CP-Devis	0.36	-	mAd
(V _{OL} = 0.5 Vdc)		10	1.3	07 88-	1.1	2.25		0.9	100 US (\$5000)	eT see
(VOL = 1.5 Vdc)		15	3.6	-	3.0	8.8	-	2.4		a i digita
Input Current (AL Device)	lin	15	-	± 0.1		±0.00001	±0.1	-	±1.0	μAdc
nput Current (CL/CP Device)	lin	15	DITA	± 0.3	UDSHO	±0.00001	±0.3	HEARI	±1.0	μAdc
nput Capacitance	Cin	_	(WWO)	ROUTE	1/62010	5.0	7.5	-	-	pF
(V _{in} 0)	-111								1	
Quiescent Current (AL Device)	Inn	5.0	- 001	0.25	-	0.0005	0.25	-	7.5	μAdc
(Per Package)	IDD	10	- Add	0.50		0.0010	0.50	SE.	15	, artuc
(1 et 1 de kage)		15		1.00		0.0015	1.00	v _4 v	30	0
		-					1.00		7.5	1
Quiescent Current (CL/CP Device)	IDD	5.0	-	1.0	_	0.0005	2.0	0		μAdo
(Per Package)		10	BERRYO OF	2.0	-O T2NG	0.0010	4.0	-	15	1 5
0 4 cm 0 4 cm 0 - 0 - 0 - 0 - 0		15	-	4.0		0.0015		-	30	-
Total Supply Current**†	IT	5.0		1000		0.3 µA/kHz				μAd
(Dynamic plus Quiescent, Per Gate)		10		Lill		0.6 μA/kHz				
(CL = 50 pF)		15		1	1T = ((0.9 µA/kHz	f + IDD/	6 01-		21
emient smolute			- 00							
Output Rise and Fall Times**	tTLH,	100	lis no no	Source el	olo store	34		55	×1_	ns
(C _L = 50 pF)	tTHL.			mont	ron aruq				V	F3 18
TLH, THL = (1.35 ns/pF) CL + 33 ns		5.0	-	-	-	100	200	-	-	
TLH, THL = (0.60 ns/pF) CL + 20 ns		10	-	_	-	50	100	_		
TLH, THL = (0.40 ns/pF) CL + 20 ns		15	-	-	_	40	80	-	-	
Propagation Delay Times**	tPLH.	A TIUDS	D TEST E	MIT DU	SWITCH	L BAUDE	77			ns
(C _L = 50 pF)	tPHL	3 3.4							111111111111111111111111111111111111111	
tpLH,tpHL = (0.90 ns/pF) CL + 20 ns	Feb 50'S	5.0	-	-	-	65	125	-	-	12.
tpLH,tpHL = (0.36 ns/pF) CL + 22 ns		10	-	-	- 0	40	75	-	-	
tpLH,tpHL = (0.26 ns/pF) CL + 17 ns		15				30	55			1

^{*}Tlow = -55°C for AL Device, -40°C for CL/CP Device Thigh = + 125°C for AL Device, +85°C for CL/CP Device †To calculate total supply current at loads other than 50 pf:

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper

IT(CL) = IT (50 pF) + 6 X 10 3 (CL - 50) VDDf

where: $I_{\mbox{\scriptsize T}}$ is in $\mu\mbox{\scriptsize A}$ (per package), $\mbox{\scriptsize C}_{\mbox{\scriptsize L}}$ in pF, $\mbox{\scriptsize V}_{\mbox{\scriptsize DD}}$ in Vdc, and f kHz is input frequency.

^{**}The formulas given are for the typical characteristics only at 25°C.

[#]Noise immunity specified for worst-case input combination. Noise Margin for both "1" and "0" level =

^{0.5} Vdc min @ V_{DD} = 5.0 Vdc 1.0 Vdc min @ V_{DD} = 10 Vdc 1.0 Vdc min @ V_{DD} = 15 Vdc

operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leqslant (V_{in}$ or $V_{out}) \leqslant V_{DD}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).



CMOS SSI

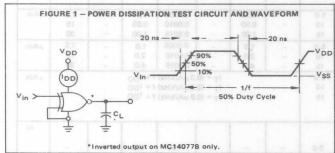
QUAD EXCLUSIVE "OR" AND "NOR" GATES

The MC14070B quad exclusive OR gate and the MC14077B quad exclusive NOR gate are constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These complementary MOS logic gates find primary use where low power dissipation and/or high noise immunity is desired.

- Quiescent Current = 0.5 nA typ/pkg @ 5 Vdc
- Noise Immunity = 45% of VDD typ
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range.
- Double Diode Protection on All Inputs
- MC14070B Replacement for CD4030B, CD4070B, and MC14507 Types
- MC14077B Replacement for CD4077B Type

MAXIMUM RATINGS (Voltages referenced to VSS)

Rating	Symbol	Value	Unit
DC Supply Voltage	VDD	-0.5 to +18	Vdc
Input Voltage, All Inputs	Vin	-0.5 to V _{DD} + 0.5	Vdc
DC Current Drain per Pin	3 111	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	TA	-55 to +125 -40 to +85	°C
Storage Temperature Range	T _{stg}	-65 to +150	°C



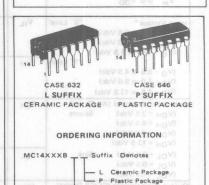
MC14070B

#C14070B*MC14077B

QUAD EXCLUSIVE "OR" GATE

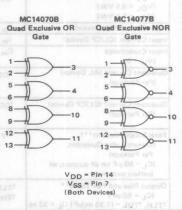
MC14077B

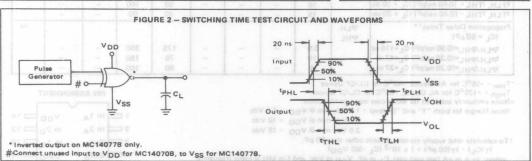
QUAD EXCLUSIVE "NOR" GATE



Extended Operating

Temperature Range Limited Operating Temperature Range





MC14070B•MC14077B

ELECTRICAL CHARACTERISTICS

	10.00	VDD	Tic	ow*		25°C		Thi	igh °	
Characteristic	Symbol	Vdc	Min	Max	Min	Тур	Max	Min	Max	Unit
Output Voltage "O" Level	VOL	5.0	-	0.05	-	0	0.05	-	0.05	Vdc
V _{in} · V _{DD} or 0	0.	10	-	0.05	-	0	0.05	-	0.05	-
D EXCLUSIVE "NOR" GA	AUD I	15	-	0.05	- 1	0	0.05	-	0.05	
"1" Level	VOH	5.0	4.95		4.95	5.0	-	4.95		Vdc
Vin Oor VDD	011	10	9.95	TAD "I	9.95	10	SIATE	9.95	GA <u>L</u> UO	
1111		15	14.95	METOMA	14.95	15	ant-a	14.95	10.1784	-
nput Voltage " "0" Level	VIL		The Island	Jan D 20	A AND			edep F	DIS -	Vdc
(VO = 4.5 or 0.5 Vdc)	112	5.0	1	1.5	5 76	2.25	1.5	anah u	1.5	The same
(VO = 9.0 or 1.0 Vdc)	38b	10	rizilonos	3.0	B 101	4.50	3.0	STITISCH TEN	3.0	N-chi
(V _O = 13.5 or 1.5 Vdc)		15	mary u	4.0	aned ord	6.75	4.0	amob as	4.0	Smile
"1" Level	VIH		10011200	7710	-111 29110	CHEDY TOTAL	110 110170	CHARLES COL	500, 8501	100,123
(VO = 0.5 or 4.5 Vdc)		5.0	3.5	-	3.5	2.75	0.5 pA	3.5	micael	Vdc
(Va - 1 0 or 9 0 Vdc)		10	7.0	_	7.0	5.50	V to #8	7.0	mrul ezi	dvi e
(V _O = 1.5 or 13.5 Vdc)		15	11.0	_	11.0	8.25	0.6- up	11.0	loV-vilgo	8 0
Output Drive Current (AL Device)	ОН		1			-		Buffere	SUCCESU C	mAdo
(VOH = 2.5 Vdc) Source	поп	5.0	-3.0	s. Cae L	-2.4	-4.2	out-ow?	0-1.7 C	to eldeo	10 8
(V _{OH} = 4.6 Vdc)		5.0	-0.64	ne Flated	-0.51	-0.88	ON-T 10	-0.36	T vitron	2
(VOH = 9.5 Vdc)		10	-1.6	_	-1.3	-2.25	_	-0.9	non-El-	100
(V _{OH} = 13.5 Vdc)		15	-4.2	_	-3.4	-8.8	-	-2.4	With the last	0 -
(VOI = 0.4 Vdc) Sink	lou	5.0	0.64		0.51	0.88	-	0.36		mAdo
$(V_{OL} = 0.5 \text{ Vdc})$	IOL	10	1.6	370B, an	1.3	2.25) Triemes	0.9	140708	IIIAGC
(VOL = 1.5 Vdc)		15	4.2		3.4	8.8		2.4	74507	NI.
		15	7.2	-	5.4	0.0	Smarrobs.	2.7	OCCOPIN	0
Output Drive Current (CL/CP Device)	ІОН	5.0	-2.5	-	-2.1	-4.2		-1.7		mAdo
(V _{OH} = 2.5 Vdc) Source		5.0	-0.52	_	-0.44	-0.88	naler rates	-0.36	RATIN	JUNEOX
(V _{OH} = 4.6 Vdc)		5.0	-1.3	deV_	-1.1	-2.25	_	-0.36	-	
(V _{OH} = 9.5 Vdc)		10	-3.6	01 3-0-	-3.0	-8.8	-	-2.4	-	
(V _{OH} = 13.5 Vdc)	-	15	-	-	1000		-		DESTIO!	ylagos
(VOL = 0.4 Vdc) Sink	OL	5.0	0.52	3V 55 3.0	0.44	0.88	_	0.36	on! #A.,s	mAdc
(V _{OL} = 0.5 Vdc)		10	1.3	01 7	1.1	2.25	-	0.9	130 Aigu	payrip0
(V _{OL} = 1.5 Vdc)	M .	15	3.6	or Tel.	3.0	8.8	- Z.J.	2.4	_	
nput Carrent (AL Device)	in I	15	- 88	± 0.1	-	±0.00001	± 0.1	10-	± 1.0	μAdc
nput Current (CL/CP Device)	lin	15	7687.	± 0.3	-	±0.00001	± 0.3	Sons	±1.0	μAdc
nput Capacitance	Cin	-	-	-	1 2	5.0	7.5	-	-	pF
(V _{in} = 0)	-1								-	
Quiescent Current (AL Device)	IDD	5.0	MOD 93	0.25	TILEDA	0.0005	0.25	0.8200	7.5	μAdc
(Per Package)		10	-	0.50	-	0.0010	0.50	-	15	
-a 1 - a - ()		15	- ne	1.00	-	0.0015	1.00	-	30	
Quiescent Current (CL/CP Device)	IDD	5.0	-	1.0	-	0.0005	1.0	-	7.5	μAdc
(Per Package)	- 00	10	-	2.0	-110	0.0010	2.0	_	15	
	-0	15	-	4.0	_ 20	0.0015	4.0	-	30	
Total Supply Current**†	IT	5.0	1		I== ((0.3 µA/kHz)	f + Inn		(aar)	μAdc
(Dynamic plus Quiescent,	61	10				0.6 µA/kHz)				pr. too
Per Package)		15	1025			0.9 µA/kHz)				1
(C ₁ = 50 pF on all outputs, all					., .,	0.0 p. ()e,				
buffers switching)		A							T	
Output Rise and Fall Times**	tTLH.		1		1	T			1	ns
(C ₁ = 50 pF)	tTHL					1	1			113
TLH, THL = (1.35 ns/pF) CL + 33 ns	THL	5.0		_	, gizo	100	200	benwal!	_	
TLH, THL = (0.60 ns/pF) C1 + 20 ns		10	-	-	-	50	100	-	-	-
TLH, THL = (0.40 ns/pF) CL + 20 ns		15	_	_	-	40	80	-	_	1
Propagation Delay Times**	tour	CHA TH	2012.42	TA SWILL	MILLIOT.	1	-	-		ns
(C ₁ = 50 pF)	tPLH.									ins.
- 10 ns	tPHL		20 06		1			100		
tpLH,tpHL=(0.90 ns/pF) CL+115 ns		5.0		-	-	175	350	0 -	-	
tpLH,tpHL=(0.36 ns/pF) CL+47 ns	20	10	rugal-	-	-	75	150	-	-	
tpLH,tpHL=(0.26 ns/pF) CL+37 ns		15	-	-	-	50	100	and the same		900

*T_{Iow} = -55°C for AL Device, -40°C for CL/CP Device T_{high} = +125°C for AL Device, +85°C for CL/CP Device. =Noise immunity specified for worst-case input combination.

Noise Margin for both "1" and "0" level = 1.0 Vdc min @ VDD = 5.0 Vdc 2.0 Vdc min @ VDD = 10 Vdc

2.5 Vdc min @ VDD = 15 Vdc

†To calculate total supply current at loads other than 50 pF: $I_T(C_L) = I_T(50 \text{ pF}) + 1 \times 10^{-3} (C_L - 50) \text{ Vppf}$

where: 1_T is in μ A (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency. *The formulas given are for the typical characteristics only at 25° C.

PIN ASSIGNMENT 1 = In 1A V_{DD} 14 In 2_D 13 2 = In 2A 3 OutA In 1_D 12 4 OutB Out_D 11 5 In 1B Outc 10 6 In 2B In 2_C 9 7 VSS In 1c 8



MC14071B

MOTOROL

QUAD 2-INPUT "OR" GATE

The MC14071 and MC14071B are constructed with P and N channel enhancement mode devices in a single monolithic structure (Complementary MOS). Their primary use is where low power dissipation and/or high noise immunity is desired.

- Quiescent Current = 0.5 nA typ/pkg @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typ
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range. (MC14071B only)
- Double Diode Protection on All Inputs
- Pin-for-Pin Replacement for CD4081B

MAXIMUM RATINGS (Voltages referenced to VSS)

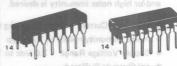
Rating	Symbol	Value	Unit
DC Supply Voltage	V _{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	Vin	-0.5 to V _{DD} +0.5	Vdc
DC Current Drain per Pin	1	10	mAdc
Operating Temperature Range - AL Device CL/CP Device	TA	-55 to +125 -40 to +85	°C
Storage Temperature Range	T _{stg}	-65 to +150	°C

See the MC14001B data sheet for complete characteristics of this device.

CMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

QUAD 2-INPUT "OR" GATE

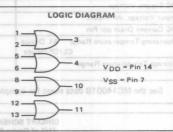


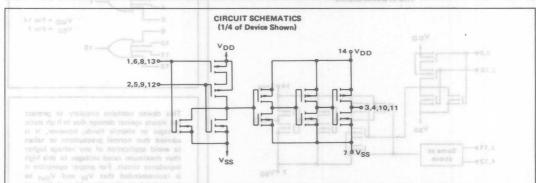
LSUFFIX CERAMIC PACKAGE PLASTIC PACKAGE CASE 632

CASE 646

ORDERING INFORMATION

Suffix Denotes MC14XXXB - L Ceramic Package P Plastic Package
A Extended Operating Temperature Range C Limited Operating Temperature Range





This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper

operation it is recommended that V in and V out be constrained to the range VSS \leq (V in or V out) \leq VDD. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD).



MC14072B

DUAL 4 INPUT "OR" GATE

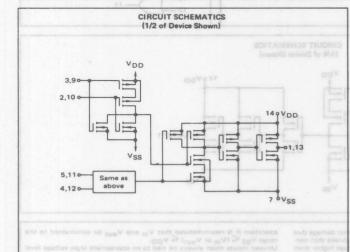
The B Series logic gates are constructed with P and N channel enhancement mode devices in a single monolithic structure (Complementary MOS). Their primary use is where low power dissipation and/or high noise immunity is desired.

- Quiescent Current = 0.5 nA typ/pkg @ 5 Vdc
- Noise Immunity = 45% of Vpp typ
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range.
- Double Diode Protection on All Inputs
- Pin-for-Pin Replacement for CD4072B

MAXIMUM RATINGS (Voltages referenced to Vss)

Rating	Symbol	Value	Unit	
DC Supply Voltage	VDD	-0.5 to +18	Vdc	
Input Voltage, All Inputs	Vin	-0.5 to V _{DD} +0.5	Vdc	
DC Current Drain per Pin	I	10	mAdo	
Operating Temperature Range AL Device CL/CP Device	TA	-55 to +125 -40 to +85	°C	
Storage Temperature Range	T _{stq}	-65 to +150	°C	

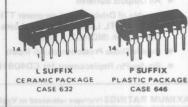
See the MC14001B data sheet for complete characteristics for this device.



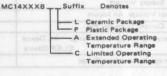
CMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

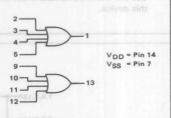
DUAL 4-INPUT "OR" GATE



ORDERING INFORMATION



LOGIC DIAGRAM



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that Vin and Vout be constrained to the range VSS < (Vin or Vout) < VDD.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD).

3





The B Series logic gates are constructed with P and N channel enhancement mode devices in a single monolithic structure (Complementary MOS). Their primary use is where low power dissipation and/or high noise immunity is desired.

- Quiescent Current = 0.5 nA typ/pkg @ 5 Vdc
- Noise Immunity = 45% of VDD typ
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range.
- Double Diode Protection on All Inputs
- Pin-for-Pin Replacement for CD4073B

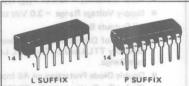
MAXIMUM RATINGS (Voltages referenced to Vos)

Rating	Symbol	Value Walle	Unit	
DC Supply Voltage	VDD	-0.5 to +18	Vdc	
Input Voltage, All Inputs	Vin	-0.5 to V _{DD} +0.5	Vdc	
DC Current Drain per Pin	1 :	10 01	mAde	
Operating Temperature Range AL Device CL/CP Device	TA	-55 to +125 -40 to +85	°C	
Storage Temperature Range	T _{stq}	-65 to +150	°C	

CMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

TRIPLE 3-INPUT "AND" GATE

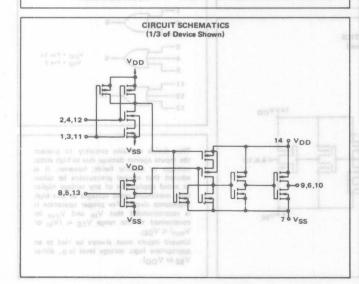


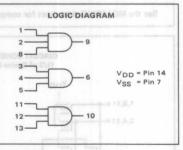
CERAMIC PACKAGE PLASTIC PACKAGE CASE 646

ORDERING INFORMATION MC14XXXB ___ Suffix Denotes L Ceramic Package Plastic Package Extended Operating Temperature Range C Limited Operating Temperature Range

CASE 632

See the MC14001B data sheet for complete characteristics for this device.





This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in})$ or Vout) < VDD.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD).

TRIPLE 3-INPUT "OR" GATE

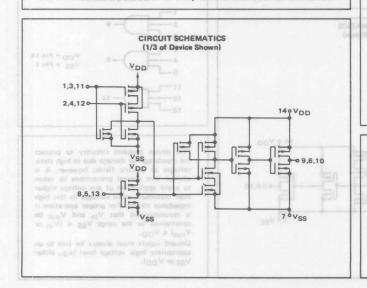
The B Series logic gates are constructed with P and N channel enhancement mode devices in a single monolithic structure (Complementary MOS). Their primary use is where low power dissipation and/or high noise immunity is desired.

- Quiescent Current = 0.5 nA typ/pkg @ 5 Vdc
- Noise Immunity = 45% of VDD typ
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range.
- Double Diode Protection on All Inputs
- Pin-for-Pin Replacement for CD4075B

MAXIMUM RATINGS (Voltages referenced to Vos)

Rating axxxxx	Symbol	Value	Unit
DC Supply Voltage	VDD	-0.5 to +18	Vdc
Input Voltage, All Inputs	Vin	-0.5 to V _{DD} +0.5	Vdc
DC Current Drain per Pin	1 3	10 01	mAdo
Operating Temperature Range - AL Device CL/CP Device	TA	-55 to +125 -40 to +85	°C
Storage Temperature Range	T _{stq}	-65 to +150	°C

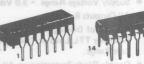
See the MC14001B data sheet for complete characteristics for this device.



CMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

TRIPLE 3-INPUT "OR" GATE



L SUFFIX CERAMIC PACKAGE PLASTIC PACKAGE **CASE 632**

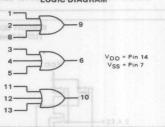
VO" GATE

P SUFFIX **CASE 646**

ORDERING INFORMATION MC14XXXB __ Suffix Denotes

Ceramic Package Plastic Package Extended Operating Temperature Range
C Limited Operating Temperature Range

LOGIC DIAGRAM



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range V_{SS} < (V_{in} or V_{out}) $\leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD).

3



MC14076B

4-BIT D-TYPE REGISTER with THREE-STATE OUTPUTS

The MC14076B 4-Bit Register consists of four D-type flip-flops operating synchronously from a common clock. OR gated outputdisable inputs force the outputs into a high-impedance state for use in bus organized systems. OR gated data-disable inputs cause the Q outputs to be fed back to the D inputs of the flip-flops. Thus they are inhibited from changing state while the clocking process remains undisturbed. An asynchronous master reset is provided to clear all four flip-flops simultaneously independent of the clock or disable

- Three-State Outputs with Gated Control Lines
- Fully Independent Clock Allows Unrestricted Operation for the Two Modes: Parallel Load and Do Nothing
- Asynchronous Master Reset
- For Bus Buffer Registers
- Quiescent Current = 5.0 nA/package typical @ 5 Vdc:
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range

MAXIMUM RATINGS (Voltages referenced to VSS)

Rating	Symbol	Value	Unit
DC Supply Voltage	V _{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	Vin	-0.5 to V _{DD} + 0.5	Vdc
DC Current Drain per Pin	- 1	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	TA	-55 to +125 -40 to +85	°C
Storage Temperature Range	Tstg	-65 to +150	°C

FUNCTION TABLE

	1	NPUTS			
-sbAu	sbAu d.71 -		Disable	Data	OUTPUT
Reset	Reset Clock	A	В	D	Q
1	×	×	×	×	0
0	0	×	×	×	a _n
0	5	1	×	×	Qnoorse
0	_	×	1	×	Q _n
0	_	0	0	0 sbV	IT - OV S nie
0	5	0	0	1	1:19.08

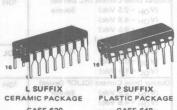
When either output disable A or B (or both) is (are) high the output is disabled to the highimpedance state; however sequential operation of the flip-flops is not affected.

X = Don't Care.

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

QUAD D-TYPE REGISTER with THREE STATE OUTPUTS



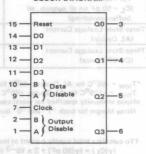
CASE 620

CASE 648

ORDERING INFORMATION

Suffix Denotes MC14XXXB L Ceramic Package - P Plastic Package A Extended Operating Temperature Range - C Limited Operating Temperature Range

BLOCK DIAGRAM



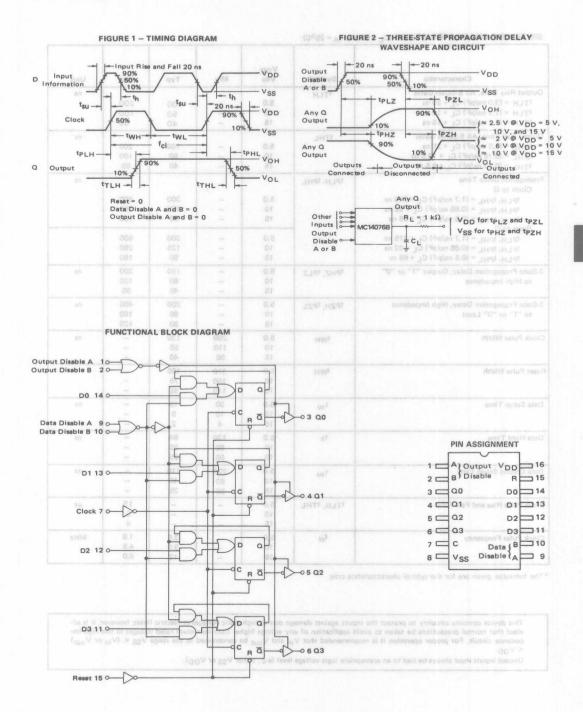
VDD = Pin 16 VSS = Pin 8



ELECTRICAL CHARACTERISTICS

		VDD	Tic	w*		25°C		Thi	gh *	
Characteristic	Symbol	Vdc	Min Max		Min Typ		p Max	Min	Max	Unit
Output Voltage "0" Level	VOL	5.0	-	0.05	-	0	0.05	-	0.05	Vdc
V _{in} = V _{DD} or 0		10	-	0.05	-	0	0.05	-	0.05	
		15	-	0.05	-	0	0.05	-	0.05	
"1" Level	VOH	5.0	4.95	-	4.95	5.0		4.95	_	Vdc
Vin = 0 or VDD	011	10	9.95		9.95	10	1-01	9.95	_	-
BIFOWER COMPLEMENTARY MOES	0.0	15	14.95	_81	14.95	15	-33NH	14.95	_	
Input Voltage# "0" Level	VIL									Vdc
(V _O = 4.5 or 0.5 Vdc)	1,5	5.0	off-eift.	1.5	·	2.25	1.5	5 SEC	1.5	1
(V _O = 9.0 or 1.0 Vdc)		10	portero bi	3.0	dan-	4.50	3.0	unerrords	3.0	1900
(V _O = 13.5 or 1.5 Vdc)		15	nebelo si	4.0	MONTH TO	6.75	4.0	to a Touch	4.0	and a
"1" Level	VIH		1				6.0			1
(V _O = 0.5 or 4.5 Vdc)	- 111	5.0	3.5	to anugni	3.5	2.75	RO an	3.5	anagno a	Vdc
(V _O = 1.0 or 9.0 Vdc)		10	7.0	200H-0	7.0	5.50	sid of	7.0	ats to be	pud
(V _O = 1.5 or 13.5 Vdc)	-	15	11.0	spond (in	11.0	8.25	de goign	11.0	bezidiri	918
Output Drive Current (AL Device)	lau	10	11.0	Hobium	11.0	0.20	and the same	11.0	Joednus	mAdo
(V _{OH} = 2.5 Vdc) Source	ІОН	5.0	-3.0	doolo s	-2.4	-4.2	ylaugen	-1.7	ripell-qifl	MAGC
(V _{OH} = 4.6 Vdc)		5.0	-0.64	_	-0.51	-0.88		-0.36	- 2	ingui
(VOH = 4.6 Vdc) (VOH = 9.5 Vdc)		10	-1.6		-1.3	-2.25	O driw	-0.30	d872-991	T 8
(VOH = 13.5 Vdc)		15	-4.2		-3.4	-8.8		-2.4	100	
			12 1000 130	100000000000000000000000000000000000000	-		a molu	ATTENDED	BORT VIII	- A -1
(V _{OL} = 0.4 Vdc) Sink	IOL	5.0	0.64	-	0.51	0.88	ie t m oJi	0.36	abo n l ov	mAdd
(V _{OL} = 0.5 Vdc)	To lar	10	1.6	-	1.3	2.25	TONE R YE	0.9	notrion/	9 0
(V _{OL} = 1.5 Vdc)		15	4.2	-	3.4	8.8	-	2.4	0 0	2.0
Output Drive Current (CL/CP Device)	ІОН			LABOUR TRI	D Inches	and the second	A- 02			mAdd
(V _{OH} = 2.5 Vdc) Source	ARSO	5.0	-2.5	P ATIC	-2.1	-4.2	5,0_nA	-1.7	3115_2201	1
(VOH = 4.6 Vdc)		5.0	-0.52	-	-0.44	-0.88	0.6 sp	-0.36	a V -tiqu	3 0
(V _{OH} = 9.5 Vdc)		10	-1.3	s, time t	-1.1	-2.25	o_TowT	-0.9	to elden	0 0
(V _{OH} = 13.5 Vdc)		15	-3.6	sta El ast	-3.0	-8.8	MIT YOU	-2.4	Land Barrie	13
(VOL = 0.4 Vdc) Sink	IOL	5.0	0.52	-	0.44	0.88	-	0.36	posE stu	mAdd
(V _{OL} = 0.5 Vdc)	SACTAS	10	1.3	-	1.1	2.25	-	0.9	-	
(V _{OL} = 1.5 Vdc)	1000	15	3.6	-	3.0	8.8	-	2.4	-	
Input Current (AL Device)	lin	15	-	± 0.1	-	±0.00001	±0.1	-	±1.0	μAdo
Input Current (CL/CP Device)	lin	15	-	± 0.3	-	±0.00001	±0.3	-	±1.0	μAdo
Input Capacitance	Cin	_	-	-	-	5.0	7.5	-	-	pF
(V _{in} = 0)	OIN					0.0		Havi 22		CIRRIES
Quiescent Current (AL Device)	las	5.0	10-	5.0	-	0.005	5.0	Erroral	150	μAdo
(Per Package)	IDD	10		10	₹₽d/w	0.005	10	prorei	300	µAdc
,		15	18	20	ea.	0.010	20		600	Ajdde
Outcomes (CL ICR Day)	To a		100		1			-	THE RESERVE	
Quiescent Current (CL/CP Device) (Per Package)	IDD	5.0	1	20	1	0.005	20	-	150	μAdo
(Per Package)	11		307	40	-	0.010	40		300	
- 10 10	-	15	- 633	80	I -A	0.015	80	- nansh	600	1 Buils
Total Supply Current**†	IT	5.0	- 00			.75 µA/kH2				μAdd
(Dynamic plus Quiescent,		10	081			.50 μA/kHz				ge Terre
Per Package) (C _L = 50 pF on all outputs, all buffers switching)		15			I _T = (2	.25 μA/kHz	f+ 1DC)		
Three-State Leakage Current (AL Device)	ITL	15	-	±0.1		±0.00001	± 0.1	-	±3.0	μAdo
Three-State Leakage Current	ITL	15	9700	±1.0	-	±0.00001	±1.0	-	± 7.5	μAdo
(CL/CP Device)			45 MA	823352	-					

^{*}Tlow = -55°C for AL Device, -40°C for CL/CP Device. Thigh = +125°C for AL Device, +85°C for CL/CP Device. **Noise immunity specified for worst-case input combination. Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_DD = 5.0 Vdc 2.0 Vdc min @ V_DD = 10 Vdc 2.5 Vdc min @ V_DD = 15 Vdc †*To calculate total supply current at loads other than 50 pF: $I_{T}(C_{L}) = I_{T}(50 \, \text{pF}) + 2 \, \text{x} \, 10^{-3} \, (C_{L} - 50) \, \text{V}_{DD} \text{f}$ where: I_{T} is in μ A (per package), C_{L} in pF, V_{DD} in Vdc, and f in kHz is input frequency. **The formulas given are for the typical characteristics only at 25°C.



SWITCHING CHARACTERISTICS* (CL = 50 pF, TA = 25°C)

5 ns 20 ns	19-21	V		and Fall 20	eringut Ale	
Characteristic	Symbol	VDD	Min	Тур	Max	Unit
Output Rise Time, All B-Series Gates	tTLH	88V	H In-	1		ns
tTLH = (3.0 ns/pF) CL + 30 ns		5.0	men DS	100	200	
tTLH = (1.5 ns/pF) CL + 15 ns	DynA	10	705-	50	100	
t _{TLH} = (1.1 ns/pF) C _L + 10 ns	Output	15	- 1	40	80	Cigor
Output Fall Time, All B-Series Gates	tTHL	85.A.	-	-1M1	-1997	ns
tTHL = (1.5 ns/pF) C ₁ + 25 ns	DynA	5.0		100	200	
tTHL = (0.75 ns/pF) CL + 12.5 ns	Output	10		50	100	
t _{THL} = (0.55 ns/pF) C _L + 9.5 ns	Cutputs	15	1. J-	40	80	
Propagation Delay Time	tPLH, tPHL	70V	I - Jegr		- F- HJT	ns
Clock to Q		F.0		300	600	
tpLH, tpHL = (1.7 ns/pF) CL + 215 ns		5.0	_		600	
tpLH, tpHL = (0.66 ns/pF) CL + 92 ns	Other Com	10	- 0	125		
tpLH, tpHL = (0.5 ns/pF) CL + 65 ns Reset to Q	Maria Maria	15	- 4	90	180	
tpLH, tpHL = (1.7 ns/pF) CL + 215 ns	Output Disable 5—6	5.0	_	300	600	
tPLH, tPHL = (0.66 ns/pF) CL + 92 ns	B to A	10	_	125	250	
tpLH, tpHL = (0.5 ns/pF) CL + 65 ns		15	-	90	180	
3-State Propagation Delay, Output "1" or "0"	tPHZ, tPLZ	5.0	_	150	300	ns
to High Impedance	THZ, TLZ	10	_	60	120	
to riigii impedence		15	_	45	90	
3-State Propagation Delay, High Impedance	tPZH, tPZL	5.0	-	200	400	ns
to "1" or "0" Level	YZH, YZL	10	_	80	160	
to 1 of o Level		15	_	60	120	
Clock Pulse Width	tWH	5.0	260	130	AMOUTONUT	ns
	.4411	10	110	55	_	
		15	80	40		
Reset Pulse Width	tWH	5.0	370	185	o	ns
		10	150	75	-	
		15	110	55	-	
Data Setup Time	t _{su}	5.0	30	15	-	ns
	00 80-	10	10	5	_	
	00 0	15	4	2	-7-0	a Dissblu A S
Data Hold Time	th	5.0	130	65	-	ns
		10	60	30	-	
		15	50	25	-	
Data Disable Setup Time	t _{su}	5.0	220	110		erions
2 CE STOMBOW N CE 18	- Su	10	80	40	-	
	10.50	15	50	25	-	
Clock Pulse Rise and Fall Time	tTLH, tTHL	5.0		<u>-</u>	15	μs
6 0 02 02		10		-	5	
		15		-	4	
Clock Pulse Frequency	fcl	5.0	1	3.6	1.8	MHz
Plated 2 T		10	PK ATT	9.0	4.5	02 12
B T Ves Dissis A S		15	1 -alle	12	6.0	

^{*}The formulae given are for the typical characteristics only.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in} \text{ or } V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD).



CMOS SSI

QUAD EXCLUSIVE "OR" AND "NOR" GATES

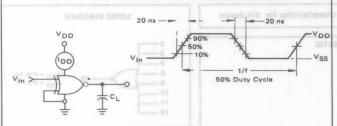
The MC14070B quad exclusive OR gate and the MC14077B quad exclusive NOR gate are constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These complementary MOS logic gates find primary use where low power dissipation and/or high noise immunity is desired.

- Quiescent Current = 0.5 nA typ/pkg @ 5 Vdc
- Noise Immunity = 45% of VDD typ
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range.
- Double Diode Protection on All Inputs
- MC14070B Replacement for CD4030B, CD4070B, and MC14507 Types
- MC14077B Replacement for CD4077B Type

MAXIMUM RATINGS (Voltages referenced to Vss)

Rating	Symbol	Value	Unit
DC Supply Voltage	VDD	-0.5 to +18	Vdc
Input Voltage, All Inputs	Vin	-0.5 to V _{DD} + 0.5	Vdc
DC Current Drain per Pin	1	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	TA	-55 to +125 -40 to +85	°C
Storage Temperature Range	T _{stg}	-65 to +150	°C

FIGURE 1 - POWER DISSIPATION TEST CIRCUIT AND WAVEFORM



*Inverted output on MC14077B only.

MC14077B

IOMOTON

QUAD EXCLUSIVE "NOR" GATE

FOR COMPLETE DATA SEE MC14070B

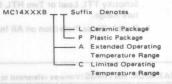


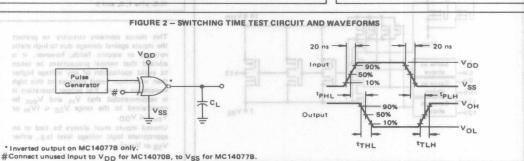
B -- IMPUT "NO



CASE 632 L SUFFIX CERAMIC PACKAGE CASE 646
P SUFFIX
PLASTIC PACKAGE

ORDERING INFORMATION







MC14078B

MOTOROLA

8 - INPUT "NOR" GATE

The B Series logic gates are constructed with P and N channel enhancement mode devices in a single monolithic structure (Complementary MOS). Their primary use is where low power dissipation and/or high noise immunity is desired.

- Quiescent Current = 0.5 nA typ/pkg @ 5 Vdc
- Noise Immunity = 45% of VDD typ
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range.
- Double Diode Protection on All Inputs

CMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

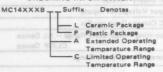
8-INPUT "NOR" GATE



L SUFFIX CERAMIC PACKAGE CASE 632

P SUFFIX
AGE PLASTIC PACKAGE
CASE 646

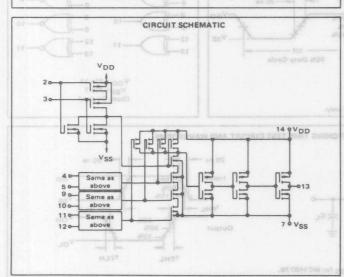
ORDERING INFORMATION

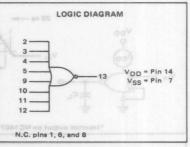


MAXIMUM RATINGS (Voltages referenced to VSS)

Rating	Symbol	Value	Unit
DC Supply Voltage	VDD	-0.5 to +18	Vdc
Input Voltage, All Inputs	Vin	-0.5 to VDD +0.5	Vdc
DC Current Drain per Pin	u0	10ge os 03	mAdc
Operating Temperature Range - AL Device CL/CP Device	TA	-55 to +125 -40 to +85	оС
Storage Temperature Range	Tstg	-65 to +150	°C

See the MC14001B data sheet for complete characteristics for this device.





This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leqslant (V_{in} \text{ or } V_{out}) \leqslant V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD).



MC14081B

QUAD 2-INPUT "AND" GATE

The MC14081 and MC14081B are constructed with P and N channel enhancement mode devices in a single monolithic structure (Complementary MOS). Their primary use is where low power dissipation and/or high noise immunity is desired.

- Quiescent Current = 0.5 nA typ/pkg @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typ
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range. (MC14081B only)
- Double Diode Protection on All Inputs
- Pin-for-Pin Replacement for CD4081B

MAXIMUM RATINGS (Voltages referenced to VSS)

Rating	Symbol	Value	Unit
DC Supply Voltage	V _{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	Vin	-0.5 to V _{DD} +0.5	Vdc
DC Current Drain per Pin	1	10 anva	mAdc
Operating Temperature Range – AL Device CL/CP Device	TA	-55 to +125 -40 to +85	°C
Storage Temperature Range	T _{stg}	-65 to +150	°C

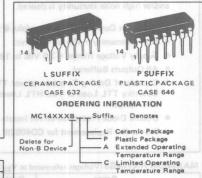
See the MC14001B data sheet for complete characteristics of this device.

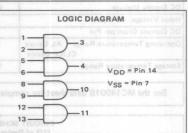
CMOS SSI

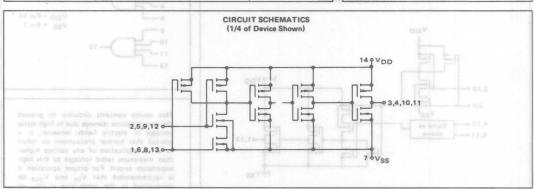
D" GATE

(LOW-POWER COMPLEMENTARY MOS)

QUAD 2-INPUT "AND" GATE







This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper

operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leqslant (V_{in} \text{ or } V_{out}) \leqslant V_{DD}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

MOTOROL

STAD "C



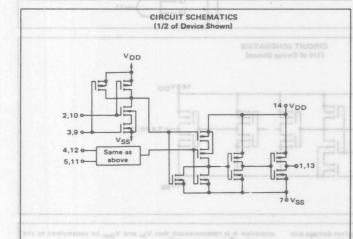
The B Series logic gates are constructed with P and N channel enhancement mode devices in a single monolithic structure (Complementary MOS). Their primary use is where low power dissipation and/or high noise immunity is desired.

- Quiescent Current = 0.5 nA typ/pkg @ 5 Vdc
- Noise Immunity = 45% of VDD typ
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range.
- Double Diode Protection on All Inputs
- Pin-for-Pin Replacement for CD4082B

MAXIMUM RATINGS (Voltages referenced to Vss)

Rating	Symbol	Value	Unit	
DC Supply Voltage	V _{DD}	-0.5 to +18	Vdc	
Input Voltage, All Inputs	Vin	-0.5 to VDD +0.5	Vdc	
DC Current Drain per Pin	1	10 11 01	mAdo	
Operating Temperature Range AL Devi	- M	-55 to +125 -40 to +85	°C	
Storage Temperature Range	T _{sta}	-65 to +150	оС	

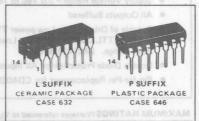
See the MC14001B data sheet for complete characteristics for this device.



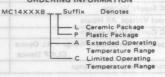
CMOS SSI

(LOW POWER COMPLEMENTARY MOS)

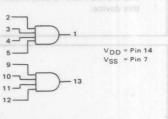
DUAL 4-INPUT "AND" GATE



ORDERING INFORMATION







This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leqslant (V_{in} \text{ or } V_{out}) \leqslant V_{OD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD).



Advance Information

QUAD 2-INPUT "NAND" SCHMITT TRIGGER

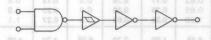
The MC14093B Schmitt trigger is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These devices find primary use where low power dissipation and/or high noise immunity is desired. The MC14093B may be used in place of the MC14011B quad 2-input NAND gate for enhanced noise immunity or to "square up" slowly changing waveforms.

- Quiescent Current = 0.5 nA typ/pkg @ 5 Vdc
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-Power TTL Loads, One Low-Power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range
- Double Diode Protection on All Inputs
- Pin-for-Pin Compatible with CD4093
- Can be Used to Replace MC14011B

MAXIMUM RATINGS (Voltages referenced to VSS)

Rating	Symbol	Value	Unit
DC Supply Voltage	VDD	-0.5 to +18	Vdc
Input Voltage, All Inputs	Vin	-0.5 to V _{DD} + 0.5	Vdc
DC Current Drain per Pin	10 1	10	mAdd
Operating Temperature Range AL Device CL/CP Device	TA -	-55 to +125 -40 to +85	°C ₀
Storage Temperature Range	T _{stg}	-65 to +150	оС

EQUIVALENT CIRCUIT SCHEMATIC (1/4 OF CIRCUIT SHOWN)



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leqslant (V_{in} \text{ or } V_{out}) \leqslant V_{DD}.$

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

CMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

QUAD 2-INPUT "NAND" SCHMITT TRIGGER





L SUFFIX CERAMIC PACKAGE CASE 632

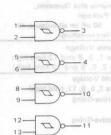
P SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

MC14XXXB ___ Suffix Denotes

L Ceramic Package
P Plastic Package
A Extended Operating
Temperature Range
Limited Operating
Temperature Range

LOGIC DIAGRAM



V_{DD} = Pin 14 V_{SS} = Pin 7



ELECTRICAL CHARACTERISTICS

		VDD	Tio	w*		25°C		Th	igh °	
Characteristic	Symbol	Vdc	Min	Max	Min	Тур	Max	Min	Max	Unit
Output Voltage "0" Level	VOL	5.0	-	0.05		0	0.05	-	0.05	Vdc
Vin = VDD or 0		10	-	0.05	-	0	0.05	-	0.05	
		15	- Æ	0.05	SILL	0	0.05	J.J. J. J. J.	0.05	
"1" Level	VOH	5.0	4.95	-	4.95	5.0	-	4.95	-	Vdc
Vin = 0 or VDD		10	9.95	-	9.95	10	-	9.95	-	
POWER COMPLEMENTARY MOSI	(FO2)	15	14.95	-	14.95	15	-	14.95	-	
nput Voltage# "0" Level	VIL		RE	TRIGG	TTHM	ND" SC		2-INPU	QAUO	Vdc
(V _O 4.5 or 0.5 Vdc)		5.0	-	1.5	-	-	1.5	-	1.5	
100 9.0 01 1.0 0001		10	mmalb.9	3.0	v batour	180,000	3.0	83B Sch	3.0	1
(VO - 13.5 or 1.5 Vdc)		15	differen	4.0	a mittee	wah Tabbe	4.0	tomina.	4.0	bos.
"1" Level	VIH		wer diss	og svel l	nedw w	primary of		piveb ea	ure. The	Spunze .
(V _O - 0.5 or 4.5 Vdc)		5.0	3.5	NCT4	3.5	pity is de	umīni ez	3.5	no\tana n	Vdc
(V _O : 1.0 or 9.0 Vdc)		10	7.0	INANG	7.0	OTTS que	MC Iv	7.0	ig nii be	be us
(V _O = 1.5 or 13.5 Vdc)		15	11.0	aliansla	11.0		in Total	11.0	on boo	- In
Output Drive Current (AL Device)	ІОН								amno	mAdo
(VOH = 2.5 Vdc) Source	Street, I	5.0	-3.0	-	-2.4	-4.2	-	-1.7	-	-
(VOH 4.6 Vdc)		5.0	-0.64	-	-0.51	-0.88	0.5 AA	-0.36) 10=050H	0
(V _{OH} = 9.5 Vdc)		10	-1.6	-	-1.3	-2.25	0.6 = 0	-0.9	oV vlag	0 50
(V _{OH} = 13.5 Vdc)	a lat	15	-4.2	-	-3.4	-8.8	-	-2.4	-	
(VOL = 0.4 Vdc) Sink	IOL	5.0	0.64	9 400 A	0.51	0.88	o Law	0.36	TO BIORO	mAdo
(V _{OL} = 0.5 Vdc)		10	1.6	steE en	1.3	2.25	DWI 10	0.9	1 Amiles	10
(VOL = 1.5 Vdc)	-	15	4.2	-	3.4	8.8	-	2.4	ne Rang	-
Output Drive Current (CL/CP Device)	ІОН		,			Stugn) ILA	no nois	de Prote	piQ stdu	mAdd
(VOH = 2.5 Vdc) Source	12	5.0	-2.5	-	-2.1	-4.2	-	-1.7	of Grant a	9 0
(V _{OH} = 4.6 Vdc)		5.0	-0.52	-	-0.44	-0.88	united and	-0.36	UC FOOTS	1
(V _{OH} = 9.5 Vdc)		10	-1.3	-	-1.1	-2.25	10M 938	-0.9	azU-sd n	0 0
(V _{OH} = 13.5 Vdc)		15	-3.6	-	-3.0	-8.8	-	-2.4	-	
(VOL = 0.4 Vdc) Sink	IOL	5.0	0.52	-	0.44	0.88	-	0.36	-	mAdd
(VOL = 0.5 Vdc)		10	1.3		1.1	2.25	-	0.9	-	-
(VOL = 1.5 Vdc)		15	3.6	-	3.0	8.8	-	2.4	DIATES O	SECONE
Input Current (AL Device)	lin	15	-	± 0.1	1	±0.00001	± 0.1	-	± 1.0	μAdo
Input Current (CL/CP Device)	lin	15		± 0.3	-	±0.00001	± 0.3	-2011	±1.0	μAdo
Input Capacitance	Cin			_	- 90	5.0	7.5			pF
(V _{in} = 0)	-111		9:0 +	ngV of 8	0- ni			1	want IfA	Notrage
Quiescent Current (AL Device)	IDD	5.0	-	0.25	-	0.0005	0.25	- 1	7.5	μAdo
(Per Package)	.00	10	28 -	0.50	- A	0.0010	0.50	- sphif	15	neT prid
1. 6. 1 66.6567		15	. 8	1,00	1	0.0015	1.00	NI2	30	
Quiescent Current (CL/CP Device)	Ipp	5.0	_ 08	1.0	- 600	0.0005	1.0	_ 602	7.5	μAdo
(Per Package)	טטי	10		2.0	1-605	0.0005	2.0	-	15	ДАОС
(rei rackage)		15		4.0	_	0.0015	4.0		30	-
Total Supply Current**†	IT	5.0	-	1.0	11				- 00	μAdo
(Dynamic plus Quiescent,	1,1	10				1.2 µA/kHz)				μAdd
Per Package)		15				2.4 μA/kHz) 3.6 μA/kHz)				
(CL · 50 pF, on all outputs, all		15			11-1	3.0 µA/KHZ)	TTIDD			
buffers switching)										1
		5.0	0.20	0.62	0.17	0.26	0.6	0.13	0.6	1 1/4
Hysteresis Voltage (Pins 1, 5, 8 and 12 held high	VH*	5.0	0.20	0.62	0.17	0.26	0.8	0.13	0.8	Vdc
		15	0.29	1.20	0.25	0.50	0.8	0.20	1.1	
or Pins 2, 6, 9 and 13 held high)		10	0.39	1.20	0.33	0.50	0.9	0.27	1.1	-
Threshold Voltage	.,		1.90	4.15	1.80	2.70	4.05	1.70	4.05	
(Pins 2, 5, 9, 12, held high)	V _{T+}	5.0	3.05	6.75	2.95	4.43	6.65	2.85	6.65	Vdc
Positive-Going		10	4.12	9.15	4.02	6.03	9.05	3.92	9.05	1
		15	-		-	-				-
Negative-Going	VT-	5.0	1.63	3.76	1.63	2.44	3.66	1.53	3.66	Vdc
		10	2.70	6.18	2.70	4.05	6.08	2.60	6.08	
		15	3.59	8.40	3.69	5.53	8.30	3.70	8.30	

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device. T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Noise immunity specified for worst-case input combination.

Noise Margin for both "1" and "0" level =

1.0 Vdc min @ V_{DD} = 5.0 Vdc

2.0 Vdc min @ V_{DD} = 10 Vdc 2.5 Vdc min @ V_{DD} = 15 Vdc †To calculate total supply current at loads other than 50 pF: IT (CL) = IT (50 pF) + 4 x 10⁻³ (CL -50) VDDf

where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.

**The formulas given are for the typical characteristics only at 25°C.

 $^{\mbox{$^+$}} v_H = v_{T+} - v_{T-}$ (But maximum variation of v_H is specified as less than v_{T+} max – v_{T-} min).

SWITCHING CHARACTERISTICS (CL = 50 pF, TA = 25°C)

Characteristic	Symbol	V _{DD} Vdc	Min	Тур	Max	Unit
Output Rise Time	tTLH	5.0	_	100 50	200 100	ns
		15		40	80	
Output Fall Time	tTHL	5.0	THUSATS TRA	100	200	ns
		10	-	50	100	
HQ		15	-	40	80	
Propagation Delay Time	tPLH, tPHL	5.0	_801	125	250	ns
		10	10 A -7	50	100	
		15	-	40	80	1

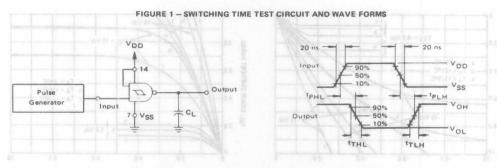
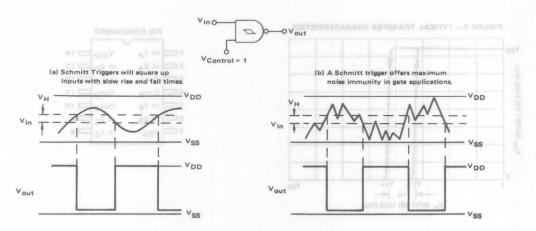
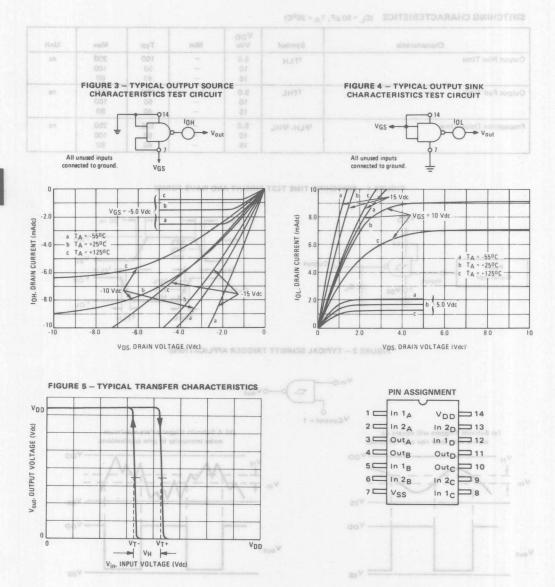


FIGURE 2 - TYPICAL SCHMITT TRIGGER APPLICATIONS









MC14094B

8-STAGE SHIFT/STORE REGISTER WITH THREE-STATE OUTPUTS

The MC14094B combines an 8-stage shift register with a data latch for each stage and a three-state output from each latch.

Data is shifted on the positive clock transition and is shifted from the seventh stage to two serial outputs. The Q_S output data is for use in high-speed cascaded systems. The Q'_S output data is shifted on the following negative clock transition for use in low-speed cascaded systems.

Data from each stage of the shift register is latched on the negative transition of the strobe input. Data propagates through the latch while strobe is high.

Outputs of the eight data latches are controlled by three-state buffers which are placed in the high-impedance state by a logic Low on Output Enable.

- Three-State Outputs
- Capable of Driving Two Low-Power TTL Loads, One Low-Power Schottky TTL Load or Two HTTL Loads Over the Rated Temperature Range
- Input Diode Protection
- Data Latch
- Dual Outputs for Data Out on Both Positive and Negative Clock
 Transitions
- Useful for Serial-to-Parallel Data Conversion
- Three-State Bus Compatible
- Pin-for-Pin Compatible with CD4094B

opa Rating 08 8	Symbol	Value	Unit
DC Supply Voltage	VDD	-0.5 to +18	Vdc
Input Voltage, All Inputs	Vin	-0.5 to V _{DD} + 0.5	Vdc
DC Current Drain per Pin	MU DAY AT	10	mAdo
Operating Temperature Range — AL Device CL/CP Device	TA	-55 to +125 -40 to +85	°C
Storage Temperature Range	T _{stg}	-65 to +150	°C

	Output			Parallel	Outputs	Serial (Outputs
Clock Enable	Enable	Strobe	Data	Q1	QN	Qs*	Q'S
5	0	X	X	38	38	Q7	No Chg.
1	0	X	X	38	38	No Chg.	07
5	1	0	X	No Chg.	No Chg.	Q7	No Chg.
5	1	1	0	0	Q _N -1	Q7	No Chg.
5	1	1	1	1	Q _N -1	Q7	No Chg.
1	1	1	1	No Chg.	No Chg.	No Chg.	Q7

3S = Three-State

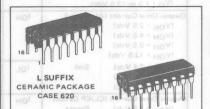
X = Don't Care

*At the positive clock edge, information in the 7th shift register stage is transferred to Q8 and Q8.

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

8-STAGE SHIFT/STORE REGISTER



PSUFFIX PLASTIC PACKAGE CASE 648

ORDERING INFORMATION

MC14	XXXB	- Suffi	ix Deno	tes
		L P	Ceramic Plastic P	
		Device!	Tempera Limited	Operating Operating Operating
pal	10	PIN ASSI	GNMEN	ий тергений
	2 = 3 =	Strobe Data Clock	V _{DD} Output Enable	16 15
	4 🖂	Q1	Q5 Q6	= 13
	6 🗆	Q2 Q3	Q8	12 11
	7 🗀	V _{SS}	Q'S QS	10 9

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leqslant (V_{in}$ or $V_{out}) \leqslant V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS

		VDD		ow*	25°C			Th		
Characteristic	Symbol	Vdc	Min	Max	Min	Тур	Max	Min	Max	Unit
Output Voltage "0" Level	VOL	5.0	-	0.05	-	0	0.05	-	0.05	Vdc
V _{in} - V _{DD} or 0		10	-	0.05	-	0	0.05	-	0.05	
	10	15	-	0.05	no sta	0	0.05		0.05	
"1" Level	VOH	5.0	4.95	71010	4.95	5.0	20100	4.95	_	Vdc
V _{ID} = 0 or V _{DD}	011	10	9.95	270	9.95	10	33BH7	9.95	-	
LINDS MAL		15	14.95	-	14.95	15	-	14.95		
nput Voltage" "0" Level	VIL		ote a sta	w tetries	s Stirle	- D	an elder	A GNOS	525183 or	Vdc
(VO - 4.5 or 0.5 Vdc)	DOM:	5.0	sh s dr	1.5		2.25	1.5	O OFFI	1.5	
(VO = 9.0 or 1.0 Vdc)		10		3.0	mon! Ju	4.50	3.0	stage an	3.0	tional.
(V _O = 13.5 or 1.5 Vdc)		15	affirle ai	4.0	lenent 7	6.75	4.0	no besti	4.0	4
Telegraphic and "1" Level	VIH	- 6	SO TURN	10 SW 80	1 .2500	10 161500	2897 OT 5	\$638 A37	1992 5711	10031
(Vo = 0.5 or 4.5 Vdc)	-114	5.0	3.5	iriua p'O	3.5	2.75	secure b	3.5	ni 480 1	Vdc
(Vo = 1.0 or 9.0 Vdc)		10	7.0	il moltis	7.0	5.50	en Taniou	7.0	he	rt irla
(VO = 1.5 or 13.5 Vdc)		15	11.0	in impose	11.0	8.25	- games	11.0	1102 120	11102
Output Drive Current (AL Device)		10	11.0		11.0	0.20	10001	102 1000	280 Deco	mAdo
	ІОН		-3.0	is lettchy	-2.4	-4.2	to ego	-1.7	morf ats	MAGE
(V _{OH} = 2.5 Vdc) Source	E33	5.0	-0.64	этерадоч	-0.51	-0.88	the stre	-0.36	tive trans	spen
(V _{OH} = 4.6 Vdc)		5.0	-1.6	-	-1.3	-2.25	doin a	-0.9	little class	the
(V _{OH} = 9.5 Vdc)	T 101	10			-3.4	-2.25		-2.4		
(V _{OH} = 13.5 Vdc)		15	-4.2	yd-ball	-	+	aseb 10		0 e-oqiii	-
(VOL = 0.4 Vdc) Sink	IOL	5.0	0.64	a ye stal	0.51	0.88	int -ni bi	0.36	HS MHICH	mAdo
(V _{OL} = 0.5 Vdc)	4	10	1.6	-	1.3	2.25	-	0.9	nil augnu	O no
(V _{OL} = 1.5 Vdc)	MARSO	15	4.2	-	3.4	8.8	-	2.4		
Output Drive Current (CL/CP Device)	ІОН							and the same	2000 000	mAdd
(VOH = 2.5 Vdc) Source		5.0	-2.5	LI SHO !	-2.1	-4.2	NO FOM	-1.7	to skilage	0.0
(VOH = 4.6 Vdc)		5.0	-0.52	B oct) 199	-0.44	-0.88	T to tisk	-0.36	Schools	
(VOH = 9.5 Vdc)		10	-1.3	-	-1.1	-2.25	- 1000	-0.9	Termoser	1100
(V _{OH} = 13.5 Vdc)		15	-3.6	-	-3.0	-8.8	-	-2.4	-	
(VOI = 0.4 Vdc) Sink	IOL	5.0	0.52	-	0.44	0.88	1700	0.36	enin and	mAdo
(VOL = 0.5 Vdc)	0.	10	1.3		1.1	2.25	_	0.9	riote-l sze	0.0
(VOL = 1.5 Vdc)		15	3.6		3.0	8.8		2.4		0.00
nput Current (AL Device)	a salin	15	20027 8	± 0.1	BV1311	± 0.00001	± 0.1		±1.0	μAdo
nput Current (CL/CP Device)	lin	15	1	±03		±0.00001	±0.3	-	±1.0	иAdd
nput Capacitance	_	-	-	-	- cois	5.0	I Indiasas	Ob leive	-	pF
(Vin = 0)	Cin					3.0	7.5	Bus Cor	ares-State	pr
Quiescent Current (AL Device)	1	5.0	-	5.0		0.005	5.0	I WARACT	150	uAdc
(Per Package)	IDD	10		10	_	0.005	10	100	150	MAGC
energy and segment		15	-	20	_	0.010	20	-	300	
			-	-		-		-	600	-
Quiescent Current (CL/CP Device)	IDD	5.0	-	20	10 -10	0.005	20	SS (Volta	150	μAdd
(Per Package)		10	-	40	.(8 <u>m</u> 19.	0.010	40	100 100	300	
1 JugityO		15	-	80	1= Divis	0.015	80	497118	600	
otal Supply Current**1	1T	5.0	804		IT = (4	1.1 µA/kHz) f + Ipp			μAdd
(Dynamic plus Quiescent,		10	8.0+0			4 μA/kHz				Variag
Per Package)		15			IT = (1	40 µA/kHz	f + IDD			77107.0
(CL = 50 pF on all outputs, all			001				minus Change			7 onle
buffers switching)			1		LA					Trans.
Carrett strikening)										

^{*}Tlow = -55°C for AL Device, -40°C for CL/CP Device.

Thigh = +125°C for AL Device, +85°C for CL/CP Device.

#Noise immunity specified for worst-case input combination.

Noise Margin for both "1" and "0" level = 1.0 Vdc min @ VDD = 5.0 Vdc

to see margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc

† To calculate total supply current at loads other than 50 pF:

IT(C_L) = IT(50 pF) + 1 × 10⁻³ (C_L -50) V_{DD}

where: IT is in µA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.

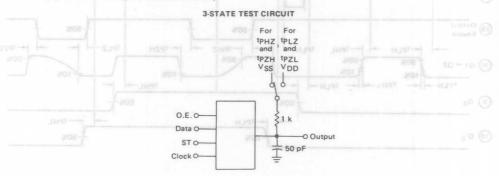
"The formulas given are for the typical characteristics only at 25°C.

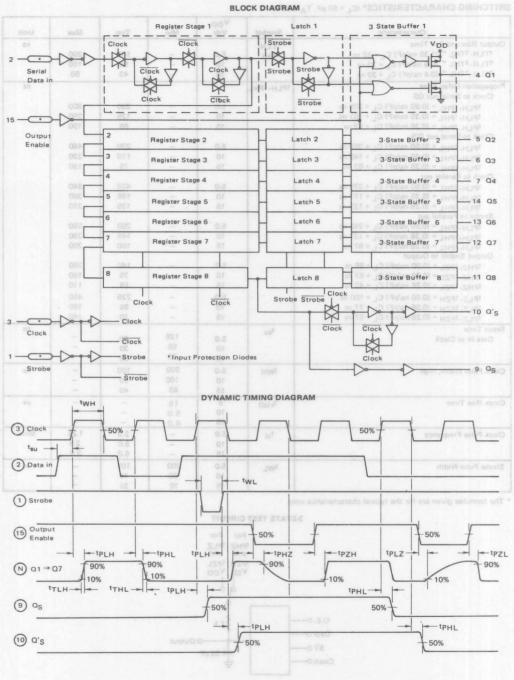
is recommended that V_{ijn} and V_{ijt} be constrained to the range $V_{SS} \leq |V_{ijt}|$ or

SWITCHING CHARACTERISTICS* (CL = 50 pF, TA = 25°C)

Characteristic	Symbol	V _{DD} Vdc	Min	Тур	Max	Unit
Output Rise and Fall Time	tTLH,		Clock	85010		ns
tTLH, tTHL = (1.35 ns/pF) C1 + 33 ns	tTHL	5.0	10/1 - 1	100	200	
tTLH, tTHL = (0.6 ns/pF) C1 + 20 ns	DAG TO THE	10	DM T	50	100	1
tTLH, tTHL = (0.4 ns/pF) C _L + 20 ns	Sucha	15	A species	40	80	Teheli
Propagation Delay Time	tPLH, tPHL		1 5			ns
Clock to Serial out QS			Syn			
tpLH, tpHL = (0.90 ns/pF) CL + 305 ns	9 114	5.0	-	350	600	
tpLH, tpHL = (0.36 ns/pF) CL + 107 ns		10		125	250	-
tplH, tpHL = (0.26 ns/pF) CL + 82 ns		15	_	95	190	
Clock to Serial out Q'S	10		Anna President		-	Cuspus
tplH, tpHL = (0.90 ns/pF) CL + 350 ns		5.0	-	230	460	eldan3 .
tPLH, tPHL = (0.36 ns/pF) CL + 149 ns		10	March 1874 (State of St.	110	220	
tpLH, tpHL = (0.26 ns/pF) CL + 62 ns		15	_	75	150	
Clock to Parallel out			Register Steps		the same of	
$t_{Pl} + t_{PHI} = (0.90 \text{ ns/pF}) C_1 + 375 \text{ ns}$		5.0	Andrew resembles	420	840	
tpLH, tpHL = (0.35 ns/pF) CL + 177 ns		10	-	195	390	
tpLH, tpHL = (0.26 ns/pF) C _L + 122 ns		15	Beginter Stage	135	270	
Strobe to Parallel out						
tpLH, tpHL = (0.90 ns/pF) CL + 245 ns	* H	5.0	appra nemigeri	290	580	
$t_{DLU} t_{DUL} = (0.36 \text{ ns/pF}) C_1 + 127 \text{ ns}$		10	-	145	290	
tpLH, tpHL = (0.26 ns/pF) CL + 87 ns	7 1	15	Pagistar Stage	100	200	
Output Enable to Output			1		1 4	
tpHZ, tpZL = (0.90 ns/pF) CL + 95 ns		5.0	-	140	280	
tpHZ, tpZL = (0.36 ns/pF) CL + 57 ns	10	10	Rogiz e ar Stelle	75	150	
tpHZ, tpZL = (0.26 ns/pF) CL + 42 ns		15	-	55	110	
tpLZ, tpZH = (0.90 ns/pF) CL + 180 ns	Serona	5.0	- 1	225	450	
tpLZ, tpZH = (0.36 ns/pF) CL + 77 ns		10	- 1	95	190	
tpLZ, tpZH = (0.26 ns/pF) CL + 57 ns		15	-	70	140	
Setup Time	t _{su}			130 3	4 4	ns
Data in to Clock	30	5.0	125	60	-	Clock
		10	55	30	-	
	20 0	15	35	20	0-1-0-	
Clock Pulse Width, High	twH	5.0	200	100	-	ndo ins
		10	100	50	-	
		15	83	40	-	
Clock Rise Time	tr(cl)	5	15	_	BWI-	μς
	1101/	10	5.0		-	
	Name of the last	15	4.0	- 1	-	
Clock Pulse Frequency	fcl	5.0	-/	2.5	1.25	MHz
manual beautiful beautiful beautiful	-	10	1	5.0	2.5	-
		15	_	6.0	3.0	1107
Strobe Pulse Width	1	5.0	200	100		ns ons
Strope Laise Martii	tWL	10	80	40		ns
	39	15	70	35		
		15	/0	35		1

* The formulae given are for the typical characteristics only.







MC14097B

FOR COMPLETE DATA SEE MC14067B

Advance Information

ANALOG MULTIPLEXERS/DEMULTIPLEXERS

The MC14067 and MC14097 multiplexers/demultiplexers are digitally controlled transmission gates featuring low ON resistance and very low leakage current. These devices can be used in either digital or analog applications.

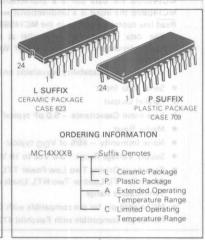
The MC14067 is a 16-channel multiplexer/demultiplexer with an inhibit and four binary control inputs A, B, C and D. These control inputs select 1-of-16 channels by turning ON the appropriate transmission gate (see MC14067 truth table).

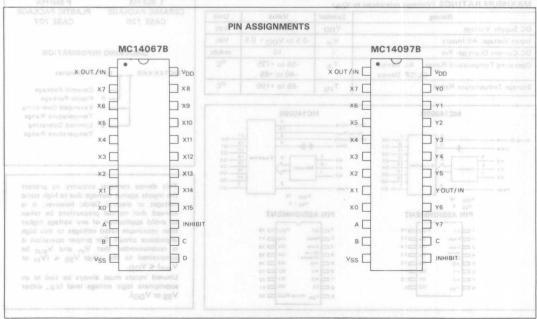
The MC14097 is a differential 8-channel multiplexer/demultiplexer with an inhibit and three binary control inputs A, B and C. These control inputs select 1 of 8 pairs of channels by turning ON the appropriate transmission gates (see MC14097 truth table).

- Low ON Resistance: 80 Ω @ VDD VSS = 15 V
- Low OFF Leakage Current
- Matched Channel Resistance
- Low Quiescent Power Consumption
- Low Crosstalk Between Channels
- Wide Operating Voltage Range: 3 to 18 V
- Transmits Frequencies Up to 65 MHz @10 V
- Low Noise
- Pin for Pin Replacement for CD4067B and CD4097B

CMOS
(LOW-POWER COMPLEMENTARY MOS)

ANALOG MULTIPLEXERS/
DEMULTIPLEXERS





ADI-919



MC14099B MC14599B



The MC14099B and MC14599B are 8-bit addressable latches. Data is entered in serial form when the appropriate latch is addressed (via address pins A0, A1, A2) and write disable is in the low state. Chip enable must be high for writing into MC14599B. For the MC14599B the data pin is a bidirectional data port and for the MC14099B the input is a unidirectional write only port. The Write/Read line controls this port in the MC14599B.

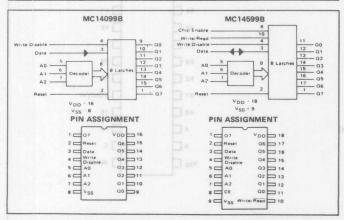
The data is presented in parallel at the output of the eight latches independently of the state of Write Disable, Write/Read or Chip Enable.

A Master Reset capability is available on both parts.

- Serial Data Input
- Parallel Output
- Low Input Capacitance 5.0 pF typical
- Master Reset
- Noise Immunity 45% of VDD typical
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-Power TTL Loads, One Low-Power Schottky TTL Load or Two HTL Loads over the Rated Temperature Range
- MC14099B pin for pin compatible with CD4099B
- Pin for pin compatible with Fairchild 4724.

MAXIMUM RATINGS (Voltages referenced to VSS)

Rating	Symbol	Value	Unit
DC Supply Voltage	VDD	-0 5 to +18	Vdc
Input Voltage, All Inputs	V _{in}	-0.5 to V _{DD} + 0.5	Vdc
DC Current Drain per Pin	1	10	mAdo
Operating Temperature Range - AL Device CL/CP Device	ТА	-55 to +1'25 -40 to +85	°C
Storage Temperature Range	T _{stg}	-65 to +150	°C



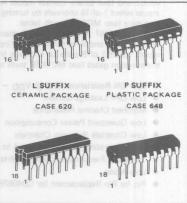
CMOS MSI

noting

(LOW-POWER COMPLEMENTARY MOS)

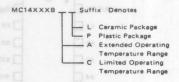
8-BIT ADDRESSABLE LATCH

MC14599B WITH BIDIRECTIONAL PORT



L SUFFIX CERAMIC PACKAGE CASE 726 P SUFFIX
PLASTIC PACKAGE
CASE 707

ORDERING INFORMATION



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in})$ or $V_{out} > V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either $v_{SS} \ \mbox{or} \ v_{DD}).$

ELECTRICAL CHARACTERISTICS

			VDD	Tio	w*		25°C		Th	igh"	
Characteristic	Typ	Symbol	Vdc	Min	Max	Min	Тур	Max	Min	Max	Unit
Output Voltage	"0" Level	VOL	5.0	1	0.05	-	0	0.05	orm) T. II	0.05	Vdc
Vin = VDD or 0	1991	-	10	1	0.05	-	0	0.05	10/m_86.1	0.05	HATE
100	08	h	15	-	0.05	-	0	0.05	Reven 8.0	0.05	43377
	"1" Level	VOH	5.0	4.95		4.95	5.0	05+30	4.95	APPLY OF	Vdc
Vin = 0 or VDD		·OH	10	9.95	16/19	9.95	10	_	9.95	yaleD no	regago!
00%	200		15	14.95	195-	14.95	15	-	14.95	зицью о	Date
Input Voltage#	"0" Level	VII	. 01								Vdc
(Vo = 4.5 or 0.5 Vdc)	08	-11	5.0		1.5	_	2.25	1.5	_	1.5	1
(V _O = 9.0 or 1.0 Vdc)	200		10		3.0	_	4.50	3.0	10000	3.0	estaw.
(VO = 13.5 or 1.5 Vdc)	08		15	L .	4.0	_	6.75	4.0	_	4.0	
0031	"1" Level	VIH	07				-			-	Vdc
(V _O = 0.5 or 4.5 Vdc)	GT Level	AIH	5.0	3.5	_	3.5	2.75	_	3.5	eniuD at	Page 27
$(V_0 = 1.0 \text{ or } 9.0 \text{ Vdc})$	08		10	7.0		7.0	5.50		7.0		
(V _O = 1.5 or 13.5 Vdc)	88	-	15	11.0	1	11.0	8.25	_	11.0		
Output Drive Current (AL D			0.8	11.0		11.0	0.20		Tr.o		- A -
(VOH = 2.5 Vdc)	Source	ЮН	5.0	-3.0		-2.4	-4.2	(vier 6	-1.7	THO OF SEC	mAdd
$(V_{OH} = 4.6 \text{ Vdc})$	Source		5.0	-3.0	=	-2.4	-4.2	14-71.0	-0.36	10 HOURS	100
(V _{OH} = 9.5 Vdc)			10	-1.6		-1.3	-2.25		-0.36		-
(V _{OH} = 13.5 Vdc)	enne I		15	-4.2	1941	-3.4	-8.8	0 8 00 12	-2.4	yeleti no	ragage of
	200			-	100	1			-	NY LETTERN 2	1411114
(VOL = 0.4 Vdc)	Sink	IOL	5.0	0.64	-	0.51	0.88	-	0.36	-	mAde
(V _{OL} = 0.5 Vdc)	-88		10	1.6	-	1.3	2.25	-	0.9	_	
(V _{OL} = 1.5 Vdc)	200		15	4.2	-	3.4	8.8	-	2.4	HECTOLIS	abba.
Output Drive Current (CL/C		ЮН	10								mAdd
(V _{OH} = 2.5 Vdc)	Source	-	5.0	-2.5		-2.1	-4.2	-	-1.7	_	
(V _{OH} = 4.6 Vdc)			5.0	-0.52	1000	-0.44	-0.88	-	-0.36	Terinb	W estu
(V _{OH} = 9.5 Vdc)	100		10	-1.3	1997	-1.1	-2.25	-	-0.9	-	nzeG
(V _{OH} = 13.5 Vdc)	. 80	007	15	-3.6	-	-3.0	-8.8	_	-2.4	-	_
(V _{OL} = 0.4 Vdc)	Sink	IOL	5.0	0.52	-	0.44	0.88	-	0.36	-	mAdd
(V _{OL} = 0.5 Vdc)	200		10	1.3	-	1.1	2.25	-	0.9	- 10	A,ddr
(V _{OL} = 1.5 Vdc)	100	200	15	3.6	-	3.0	8.8	-	2.4	-	
Input Current (AL Device)	88	lin	15	-	±0.1	-	±0.00001	±0.1	-	±1.0	μAdd
Input Current (CL/CP Devic	e) (V	lin	15	-	±0.3	-	±0.00001	±0.3	-	±1.0	μAdo
Input Capacitance	0)-	Cin	- 01	-	_		5.0	7.5	-	-	pF
(V _{in} = 0)	29	08	16								
Input Capacitance	189	Cin	5.0 -			_	15.0	22.5	-	Disable	pF
MC14599B - Data (pin 3) 58	081	10								
(V _{in} = 0)	08	120	15			Pod la					1 1
Quiescent Current (AL Devi	ce)	IDD	5.0		5.0	_	0.005	5.0	_	150	μAdo
(Per Package)	08	.00	10		10	_	0.010	10	_	300	atsU
,	28	50	1501		20	_	0.015	20	_	600	
Quiescent Current (CL/CP D	evice)	IDD	5.0		20	_	0.005	20	-	150	μAdo
(Per Package)	011001	טטי	10		40		0.005	40		300	μΑσο
(i ci i denage)	et 1	081	15		80		0.015	80		600	sers Cl
Total Supply Current**†	40				00	1/4	1			000	
	23	37	5.0				5 μA/kHz)				μAdo
Dynamic plus Quiescent, Per Package)				-			.0 μA/kHz)				
(C _L = 50 pF on all outpu			15			T = (4	5 μA/kHz)	+ DD			not or
all buffers switching)	ts,	Barrier St.									

 $^{^{\}circ}$ T $_{low}$ = -55 o C for AL Device, -40 o C for CL/CP Device. T $_{high}$ = +125 o C for AL Device, +85 o C for CL/CP Device.

[#]Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level =

[&]quot;0" level =

1.0 Vdc min @ V_{DD} = 5.0 Vdc

2.0 Vdc min @ V_{DD} = 10 Vdc

2.5 Vdc min @ V_{DD} = 15 Vdc

[†]To calculate total supply current at loads other than 50 pF:

 $I_T~(C_L)=I_T~(50~pF)+4\times10^{-3}~(\dot{C}_L-50)~V_{DD}f$ where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.

^{**}The formulas given are for the typical characteristics only at 25°C .

tioU xoNi	Charact	eristic			Symbol	VDD	Min	Тур	Max	Unit
Output Rise and Fa	1111111		1			1	10000000		DEPOSITION TO THE	ns
tTLH, tTHL = (C. 42	12 ne		TLH.	5.0	10A H	100	200	
					THL				200	
tTLH, tTHL = (80.0	10		50	100	
tTLH, tTHL = (0.4 ns/pF) C	L +20	ns	4.85	- 1 80	15	Valu	40	80	
Propagation Delay	Time				tPHL,			-	noV to I	- ns
Data to Output					tPLH 30	5.0	-	200	400	
						10		75	150	
					8.5	15	212	50	100	
Write Disable to	Output				3.0	5.0		200	400	ns
0.4	Output				4.0	10			160	
					10.5	15		60	120	
Vdc							NEV I	It / Ital		
Reset to Output					- 8.8	5.0	-	175	350	ns
	7.0			7.0	- 0.0	1001	-	80	160 a 0.1	
					- 0.1	15	-	65	130 00	
Address to Out	put		1			5.0	HOL	225	450	ns
CE to Output (f	*	only)	1 54- 1		- 0.3	10	110	100	200	
		-	88.0-		- 0.8	15		75	150	(HDV)
Propagation Delay	Time MC14	EDOD .		E.1-		101		1	9,5 Vde)	ns
Chip Enable, Wr			8.8-		tPHL,			200	400	
					tPLH	5.0	-			HO A)
					P0	100.8	101	80	(160).0	10A)
					- 8	1501	-	65	130 8.0	LIOV)
Address to Data	2.4				- 5	5.0	-	200	400	_ ns
						10	HE	90	180	upur Dr
					- 8.5	15	-	75	150	
Pulse Widths	86.0-	-	88.0-	86,9-		5.0			(abV 8, b a	ns
Data					tWH,	5.0	200	100	(abV 8.6 ×	HOVE
-					tWL	10	100	50	13.5 Ved	HOVI
					- 58	1500	80	40	(65V-8,0+	HOVI
					- 1			-		-
Address					- 8	5.0	400	200	1.5 Vde)	o ns
					-	10	200	100	the second secon	NOL
					1.0: -	15	125	65	ent (AL Devia	gut Cun
Reset 0.11					E.0: 4	5.0	150	75	ent (CL/CP D	no ns
						10	75	40	Tomer a	GBD five
						15	50	25	- (0	
Write Disable						5.0	320	160	=anel(ae	-
						10	160		808 - Bets (p	
						15	120	60	1	
			1				-	-	150	
Set Up Time					0.8 t _{su}		- agi	(epive	Current (AL I)	
Data 008					10	5.0	100	50	-(egasts	(Per Pa
					20	10	50	25	-	
150 sAdo	-	200	0.005		20	15	35	20	Current (CL)	Tenance
Hold Time	-	00	0,010	-	Da th	10			(apasts	ns
Data 008					08	5.0	150	75	_	
obAu.					-	10	75	40		
Charles 1						15	50	95	ity Current***	
		adi 4	0 MAZKHZ) F	et Ti		100	00	int,	ic plus Quiesce	Daynass

^{*} The formulae given are for the typical characteristics only.

To calculate total supply current at loads other than 80 pF:

tr (C1) = tr (50 pF) = 4 x 10⁻³ (C1 -50) Vnpf

where IT is in uA (per package), CL in pF, Vpp in Vds, and f in

**The formulas given are for the typical characteristics only at

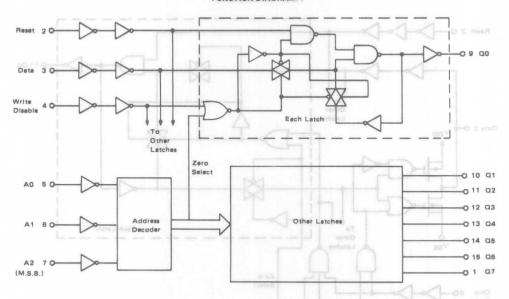
 $^{\circ}$ T_{10W} = -85°C for AL Device, -40°C for GL/CP Device. $^{\circ}$ T_{10D} = +125°C for AL Device, +35°C for GL/CP Device. eVipise immiunity specified for worst-case input combination

or both "1" and "0" level =

1.0 Vac min @ V_{DD} = 5.0 Vac

2.0 Vale min @ V_{DD} = 10 Vac

MC14099B FUNCTION DIAGRAM



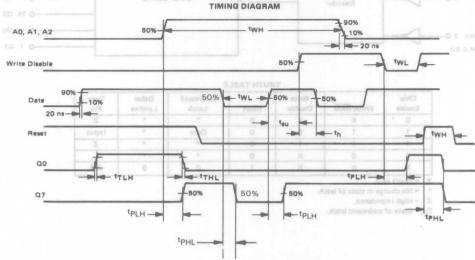
TRUTH TABLE

Write Disable	Reset	Addressed Latch	Unaddressed Latch
0	0	Data	Q _n °
0	1	Data	Reset†
1	0	Qn*	Q _n *
1	1	Reset	Reset

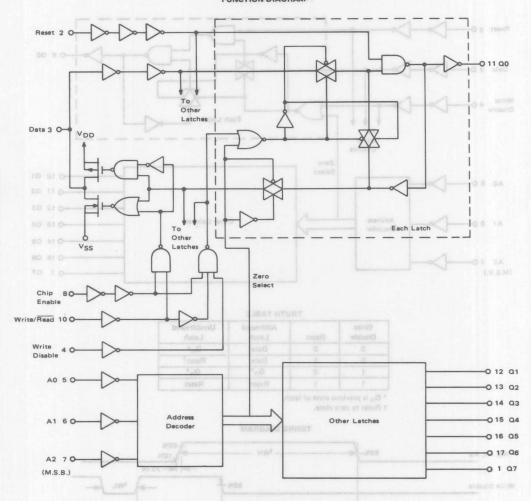
* Qn is previous state of latch.

† Reset to zero state.

TIMING DIAGRAM



MC14599B FUNCTION DIAGRAM



	H			

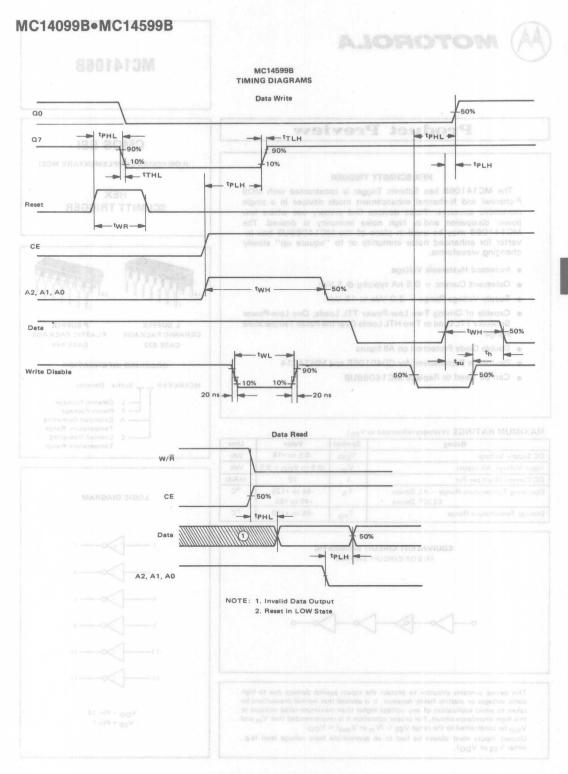
Chip Enable	Write/Read	Write Disable	Reset	Addressed Latch	Other Latches	Data Pin
0	X	X	0	•		Z
_ 1	1 10-	0	0	Data		Input
1	1	- 1	0	•		Z
1	0	X	0			Qn
X	Х	X	1	0	0	Z/0

X = Don't care.

^{* =} No change in state of latch.

Z = High impedance.

Qn = State of addressed latch.



MC14106B

Product Preview

SMARBAID SUMMIT

HEX SCHMITT TRIGGER

The MC14106B hex Schmitt Trigger is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These devices find primary use where low power dissipation and/or high noise immunity is desired. The MC14106B may be used in place of the MC14069UB hex inverter for enhanced noise immunity or to "square up" slowly changing waveforms.

- Increased Hysteresis Voltage
- Quiescent Current = 0.5 nA typ/pkg @ 5 Vdc
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-Power TTL Loads, One Low-Power Schottky TTL Load or Two HTL Loads Over the Rated Temperature
- Double Diode Protection on All Inputs
- Pin-for-Pin Replacement for CD40106B and MM74C14
- Can Be Used to Replace MC14069UB

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V _{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	Vin	-0.5 to V _{DD} + 0.5	Vdc
DC Current Drain per Pin	1	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	ТА	-55 to +125 -40 to +85	°C
Storage Temperature Range	T _{stg}	-65 to +150	оС

EQUIVALENT CIRCUIT SCHEMATIC

(1/6 OF CIRCUIT SHOWN)

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that Vin and Vout be constrained to the range VSS ≤ (Vin or Vout) ≤ VDD.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD).

CMOS SSI

(LOW POWER COMPLEMENTARY MOS)

HEX SCHMITT TRIGGER





L SUFFIX CERAMIC PACKAGE CASE 632

P SUFFIX PLASTIC PACKAGE CASE 646

ORDERING INFORMATION

MC14XXXB Suffix Denotes

> Ceramic Package Plastic Package A Extended Operating

Temperature Range - C Limited Operating Temperature Range

LOGIC DIAGRAM

V_{DD} = Pin 14 VSS = Pin 7



CMOS MSI

SYNCHRONOUS PROGRAMMABLE 4-BIT COUNTERS

The MC14160B – MC14163B are synchronous programmable counters constructed with complementary MOS P-Channel and N-Channel enhancement mode devices in a single monolithic structure. These counters are functionally equivalent to the 74160 – 74163 TTL counters.

Two are synchronous programmable decade counters with asynchronous and synchronous clear inputs respectively (MC14160B, MC14162B. The other two are synchronous programmable 4-bit binary counters with the asynchronous and synchronous clear respectively (MC14161B, MC14163B).

- Internal Look-Ahead for Fast Counting
- Carry Output for N-Bit Cascading
 - Synchronously Programmable
 - Synchronous Counting
 - Load Control Line
 - Synchronous or Asynchronous Clear
 - Positive Edge Clocked

MAXIMUM RATINGS (Voltages referenced to VSS, Pin 8).

MAXIMON NATINGS (Voltages referenced t	UVSS, FIII C	0/.	
ab Aur Bat Rating 05 200	Symbol	Value	Unit
DC Supply Voltage	VDD	-0.5 to +18	Vdc
Input Voltage, All Inputs	Vin	-0.5 to V _{DD} + 0.5	Vdc
DC Current Drain per Pin	4 00.4	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	TA	-55 to +125 -40 to +85	°C
Storage Temperature Range	T _{stg}	-65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leqslant (V_{in} \text{ or } V_{out}) \leqslant V_{DD}.$ Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or $V_{DD}).$

MC14160B

DECADE COUNTER with Asynchronous Clear

MC14161B

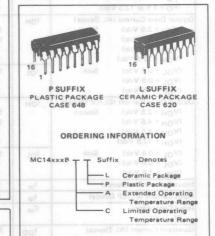
4-BIT BINARY COUNTER with Asynchronous Clear

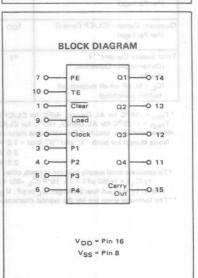
MC14162B

DECADE COUNTER with Synchronous Clear

MC14163B

4-BIT BINARY COUNTER with Synchronous Clear





M) MOTOROLA

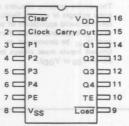


ELECTRICAL CHARACTERISTICS

MIGIAIOID		VDD	TIC	w*		25°C		Thi	igh °	
Characteristic	Symbol	Vdc	Min	Max	Min	Тур	Max	Min	Max	Unit
Output Voltage "O" Level	VOL	5.0		0.05	-	0	0.05	-	0.05	Vdc
Vin VDD or 0		10	-	0.05	-	0	0.05		0.05	
22 22 2 3 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2		15	-	0.05	-0.0	0	0.05	-	0.05	
"1" Level	VOH	5.0	4.95	-	4.95	5.0	1011	4.95	-	Vdc
Vin O or VDD	1	10	9.95	-	9.95	10	-	9.95	-	
wish Synchropaus Clear		15	14.95	(1955) G	14.95	15	10 2110	14.95	11672	
nput Voltage "0" Level	VIL					POSTIAL	1000	-		Vdc
(VO 4.5 or 0.5 Vdc)		5.0	-	1.5	22.0	2.25	1.5	-	1.5	
(VO 9.0 or 1.0 Vdc)		10	1	3.0	-	4.50	3.0	- 1	3.0	
(VO = 13.5 or 1.5 Vdc)		15	denter	4.0	nefrenci	6.75	4.0	- (500)	4.0	
"1" Level	VIH	1	lor loren	40-9 R	ary No	pamalana	o drive	bersuntr	noo con	muga
(VO - 0.5 or 4.5 Vdc)		5.0	3.5	linamen s	3.5	2.75	aboth 10	3.5	no Turne	Vdc
(V _O : 1.0 or 9.0 Vdc)		10	7.0	als Tax as	7.0	5.50	are Turn	7.0		enut
(VO = 1.5 or 13.5 Vdc)		15	11.0	- N	11.0	8.25	1101 010	11.0	1000	1.65
Output Drive Current (AL Device)	ГОН						niar anna			mAdc
(VOH = 2.5 Vdc) Source	011	5.0	-3.0	unos as	-2.4	-4.2	end smo	-1.7	576 (7)	
(VOH = 4.6 Vdc)	Silver 1	5.0	-0.64	A Takkto	-0.51	-0.88	maile in	-0.36	hranovs	21/36
(VOH = 9.5 Vdc)	2007 H	10	-1.6	กาศาฐากกา	-1.3	-2.25	e divis	-0.9	11628.	MCI
(VOH = 13.5 Vdc)		15	-4.2	synchros	-3.4	-8.8	the arti	-2.4	Index V	De Id
(VOI = 0.4 Vdc) Sink	loL	5.0	0.64	-	0.51	0.88	B MACS	0.36	n viewing	mAdc
(VOL = 0.5 Vdc)	- OL	10	1.6		1.3	2.25	_	0.9	-	
(VOL = 1.5 Vdc)		15	4.2		3.4	8.8	vol-hoor	2.4	internal	6
Output Drive Current (CL/CP Device)	To .					0.0	5 -10 14	of Justic	Charles Co.	mAdc
(VOH = 2.5 Vdc) Source	IOH	5.0	-2.5		-2.1	-4.2	Or 2110 PT	-1.7	or divine	MAGE
(V _{OH} = 4.6 Vdc)		5.0	-0.52		-0.44	-0.88	HITTER SECOND	-0.36	PHICH YE	
(V _{OH} = 9.5 Vdc)		10	-1.3		-1.1	-2.25	gmismu	-0.9	Philipping	
(V _{OH} = 13.5 Vdc)	11	15	-3.6		-3.0	-8.8	91	-2.4	KO DEOT	
		5.0	0.52	-	0.44	0.88	adonyas	0.36	MARSON V.	mAdc
(V _{OL} = 0.4 Vdc) Sink (V _{OL} = 0.5 Vdc)	IOL	10	1.3		1.1	2.25	Dosla	0.36	Postalve	MAdc
		15	3.6		3.0	8.8		2.4	_	
(V _{OL} = 1.5 Vdc)			-					-		-
nput Current (AL Device)	lin	15	-	± 0.1	-	± 0.00001	± 0.1	-	± 1.0	μAdc
nput Current (CL/CP Device)	1 in	15	-	± 0.3	-	±0.00001	± 0.3	-	±1.0	μAdc
nput Capacitance (V _{in} = 0)	Cin				-	5.0	7.5	-	-	pF
Quiescent Current (AL Device)	IDD	5.0	-	5.0		0.005	5.0	-	150	μAdc
(Per Package)	-	10	-	10	-	0.010	10	-	300	
		15		20	.[8 m/9].	0.015	20	BS (Yolu)	600	NUMB
Quiescent Current (CL/CP Device)	IDD	5.0	-	20	Peder	0.005	20	4000	150	μAdc
(Per Package)	30	10	- 81-	40	7370	0.010	40	-	300	A v Propositi
BLOCK DIAGRAM		15	270	80	- 00	0.015	80	-	600	
Total Supply Current**†	IT	5.0			IT : 10	.56 µA/kHz) f + Inn			μAdc
(Dynamic plus Quiescent,	1	10				.1 μA/kHz				1
Per Package) (C1 = 50 pF on all outputs, all		15	1			.9 μA/kHz				T griffs
buffers switching)			I man							ema7 as

†To calculate total supply current at loads other than 50 pF: $I_T(C_L) = I_T(50 \text{ pF}) + 1 \times 10^{-3} (C_L - 50) \text{ VDpf}$ where: $I_T = I_T(50 \text{ pF}) + 1 \times 10^{-3} (C_L - 50) \text{ VDpf}$ where: $I_T = I_T = I$

PIN ASSIGNMENT



^{*}Tlow = -55°C for AL Device, -40°C for CL/CP Device.
Thigh = +125°C for AL Device, +85°C for CL/CP Device.
*Noise immunity specified for worst-case input combination.

Noise Margin for both "1" and "0" level = 1.0 Vdc min @ VDD = 5.0 Vdc

2.0 Vdc min @ VDD = 10 Vdc

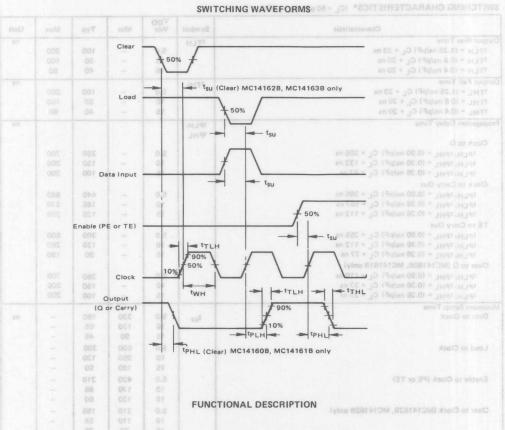
2.5 Vdc min @ VDD = 15 Vdc

oulse, regardless of the levels of the enable inputs, This

we overflow carry pulse can be used to en

3

^{*}The formulae given are for the typical characteristics only.

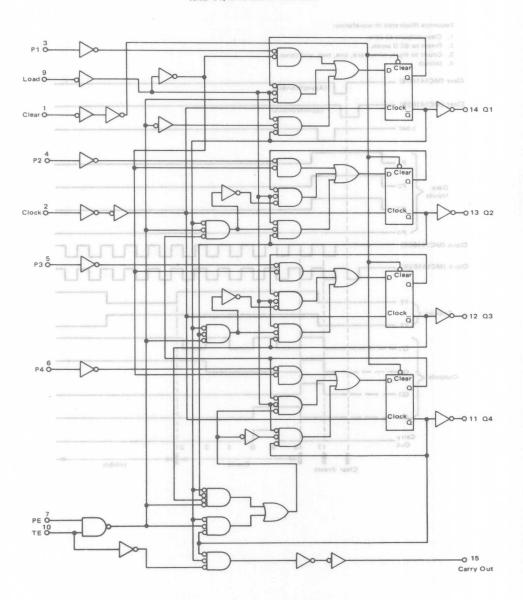


These counters are fully programmable; that is the outputs may be preset to either level. As presetting is synchronous, settling up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels of the enable inputs. The clear function for the MC14160B, MC14161B is asynchronous and a low level at the clear input sets all four of the flip-flop outputs low regardless of the levels of the clock, load or enable inputs. The clear function for the MC14162B and MC14163B is synchronous and a low level at the clear input sets all four of the flip-flop outputs low after the next clock pulse, regardless of the levels of the enable inputs. This synchronous clear allows the count length to be modified easily; decoding the maximum count desired can be

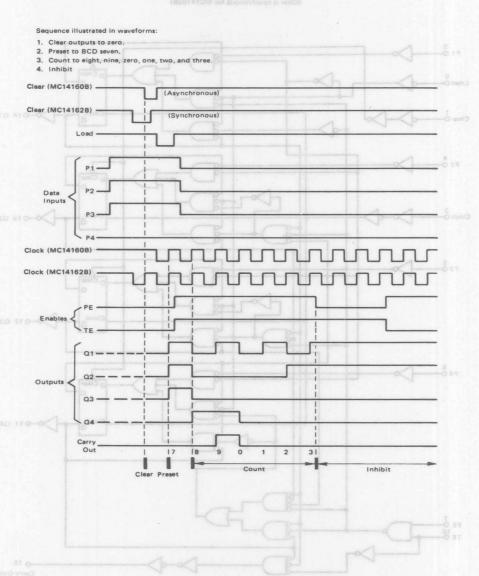
accomplished with one external NAND gate. The gate output is connected to the clear input to synchronously clear the counter to 0000 (LLLL).

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a carry output. Both count-enable inputs (PE, TE) must be high to count, and enable input TE fed forward to enable the carry output. The carry output thus enabled will produce a positive output pulse with a duration approximately equal to the positive portion of the Q1 output. This positive overflow carry pulse can be used to enable successive cascaded stages.

MC14160B, MC14162B LOGIC DIAGRAM (Clear is synchronous for MC14162B)



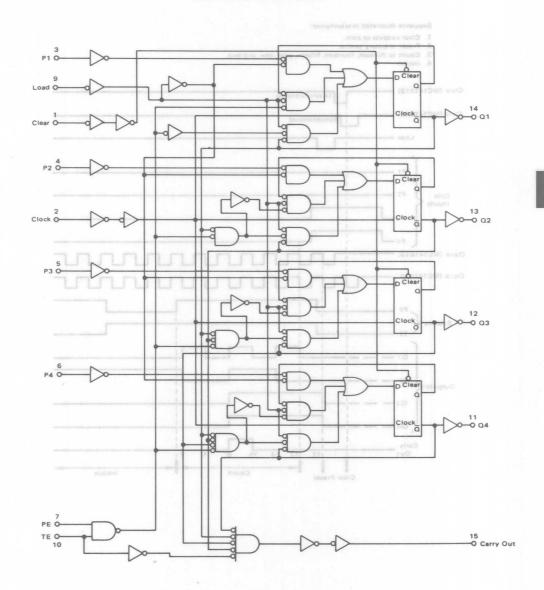
MC14160B, MC14162B TIMING DIAGRAM



2

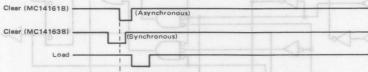
3

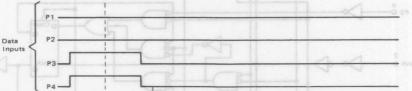
MC14161B, MC14163B LOGIC DIAGRAM (Clear is Synchronous for MC14163B)



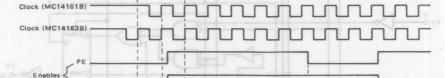
- 1. Clear outputs to zero.
- 2. Preset to binary twelve.
- 3. Count to thirteen, fourteen, fifteen, zero, one, and two,

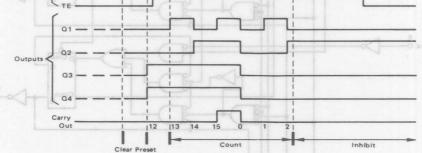






MC14161B, MC14163B TIMING DIAGRAM







MC14174B

HEX TYPE D FLIP-FLOP

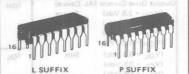
The MC14174B hex type D flip-flop is constructed with MOS Pchannel and N-channel enhancement mode devices in a single monolithic structure. Data on the D inputs which meets the setup time requirements is transferred to the Q outputs on the positive edge of the clock pulse. All six flip-flops share common clock and reset inputs. The reset is active low, and independent of the clock.

- Static Operation
- All Inputs and Outputs Buffered
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Noise Immunity = 45% of VDD typical
- Output Compatible with Two HTL Loads, Two Low-Power TTL Loads or One Low-Power Schottky TTL Load
- Functional Equivalent to TTL 74174

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

HEX TYPE D FLIP-FLOP



L SUFFIX CERAMIC PACKAGE CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

MAXIMUM RATINGS (Voltages referenced to Voc.)

MAXIMON NATINGS (Voltages referenced to	4551		
Rating & D.C	Symbol	Value	Unit
DC Supply Voltage	VDD	-0.5 to +18	Vdc
Input Voltage, All Inputs	V _{in} -0.5 to V _{DD} + 0		Vdc
DC Current Drain per Pin	1	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	TA	-55 to +125 -40 to +85	°C
Storage Temperature Range 08 8103	T _{stg}	-65 to +150	°C

TRUTH TABLE (Postive Logic)

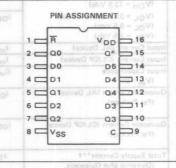
	OUTPUT		INPUTS	
	Q	Reset	Data	Clock
AND THE WORLD	0	1	0	
ow of = nov	1 ab	1	1	
No	Q 50	1	Х	7
Change	0	0	X	X

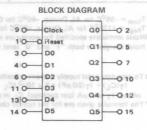
X = Don't Care

This device contains circultry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is

recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in} \text{ or } V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD).





V_{DD} = Pin 16 V_{SS} = Pin 8

MOTOROLA

ELECTRICAL CHARACTERISTICS

		VDD	Tio	w*		25°C		Th	igh °	
Characteristic	Symbol	Vdc	Min	Max	Min	Тур	Max	Min	Max	Unit
Output Voltage "O" Level	VOL	5.0	-	0.05	-	0	0.05	-	0.05	Vdc
V _{in} = V _{DD} or 0	1	10	-	0.05	-	0	0.05	-	0.05	
		15	-	0.05	-	0	0.05	-	0.05	
"1" Level	VOH	5.0	4.95	-	4.95	5.0	-	4.95	-	Vdc
V _{in} = 0 or V _{DD}		10	9.95	-	9.95	10	-	9.95	-	
		15	14.95	-	14.95	15	-	14.95	-	
nput Voltage# "0" Level	VIL				100 100		murr w			Vdc
$(V_0 = 4.5 \text{ or } 0.5 \text{ Vdc})$		5.0	-	1.5	HOTH	2.25	1.5	BH_	1.5	-
$(V_0 = 9.0 \text{ or } 1.0 \text{ Vdc})$		10	-	3.0	-	4.50	3.0	-	3.0	
(V _O = 13.5 or 1.5 Vdc)		15	804/ rb	4.0	विमाल ह	6.75	4.0	1748 her	4.0	
"1" Level	VIH		gle mon		spivab sl	om inems	onadas	l-channel	nel and	nario
(V _O = 0.5 or 4.5 Vdc)		5.0	3.5	06/2 510	3.5	2.75	0 m2 (1)	3.5	nutoente :	Vdc
(V _O = 1.0 or 9.0 Vdc)		10	7.0	triuctu ed	7.0	5.50	No.Imber	7.0	roments	E PROTE
(V _O = 1.5 or 13.5 Vdc)		15	11.0	os Topis	. 11.0	8.25	0(F-T)10	11.0	lug Slagt	the
Dutput Drive Current (AL Device)	ІОН				t to ma	indepent t	ns wol	vizos al 1	The ruse	mAdo
(VOH = 2.5 Vdc) Source		5.0	-3.0	-	-2.4	-4.2	-	-1.7	atic Ope	2 0
(V _{OH} = 4.6 Vdc)	1000	5.0	-0.64	-	-0.51	-0.88	NA	-0.36	-	0.0
(V _{OH} = 9.5 Vdc)		10	-1.6	-	-1.3	-2.25	Hud ste	-0.9	it inguts	
(V _{OH} = 13.5 Vdc)	I lay	15	-4.2	_	-3.4	-8.8	ign+liA	-2.4	ton4aboi	3 0
(VOL = 0.4 Vdc) Sink	IOL	5.0	0.64	-	0.51	0.88	0.E-= sg	0.36	pV Tlags	mAdd
(V _{OL} = 0.5 Vdc)		10	1.6	-	1.3	2.25	V To are	0.9	mmT seio	4 0
(V _{OL} = 1.5 Vdc)	snan la	15	4.2	-	3.4	8.8	-	2.4	-	S
Output Drive Current (CL/CP Device)	ІОН		1 1 Innio	EMOT A	8.3 (8DB)	2777	PE 100170	213010301913	an sodie	mAdd
(VOH = 2.5 Vdc) Source		5.0	-2.5	-	-2.1	-4.2	ng Jawo	-1.7	O 10 2060	2
(V _{OH} = 4.6 Vdc)		5.0	-0.52	-	-0.44	-0.88	T 43 T	-0.36	lant#10ne	0
(V _{OH} = 9.5 Vdc)		10	-1.3	-	-1.1	-2.25	-	-0.9	-	-
(V _{OH} = 13.5 Vdc)		15	-3.6	-	-3.0	-8.8	-	-2.4	-	
(VOL = 0.4 Vdc) Sink	IOL	5.0	0.52	-	0.44	0.88	-	0.36	-	mAdo
(V _{OL} = 0.5 Vdc)		10	1.3	-	1.1	2.25	-	0.9	-	
(VOL = 1.5 Vdc)		15	3.6	-	3.0	8.8	-	2.4	-	
nput Current (AL Device)	lin	15	-	± 0.1	-	±0.00001	± 0.1	-	±1.0	μAdc
nput Current (CL/CP Device)	lin	15	-	± 0.3	- 13	±0.00001	±0.3	CS every	±1.0	μAdc
nput Capacitance	C _{in}	[mil)		in/-	Limited	5.0	7.5	materi	-	pF
(Vin = 0) = 0			010	2.5.5	-			-	and the last	
Quiescent Current (AL Device)	IDD	5.0	Dan .	5.0	1	0.005	5.0	-	150	μAdo
(Per Package)	.00	10	100+0	10	1 niv	0.010	10	811	300	1140.4
176-920 20-0		15	-	20	-	0.015	20	ni	600	thatro.
Quiescent Current (CL/CP Device)	IDD	5.0	057	20	1 6	0.005	20	- Square	150	μAdo
(Per Package)	יטטי	10	084	40		0.010	40	U3	300	μΑσο
		15	180_ 1	80	+12	0.015	80	sgmal	600	noT agu
Total Supply Current**†	IT	5.0		. 00	1				000	μAdo
(Dynamic plus Quiescent,	-1	10	-		T = (1	1 µA/kHz)	DD			ДАОС
Per Package)		15			IT = (2	.3 μA/kHz) 3.7 μA/kHz)	DD			
(C ₁ = 50 pF on all outputs, all		13			.1-12	.7 µA/KHZ)				
buffers switching)										

°T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
Thigh = +125°C for AL Device, +85°C for CL/CP Device.

#Noise immunity specified for worst-case input combination.

Noise immunity specified for worst-case input combination.

Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc

2.0 Vdc min @ V_{DD} = 10 Vdc

2.5 Vdc min @ V_{DD} = 15 Vdc

2.5 Vac min @ V_{DD} = 15 Vac

1_T(C_L) = 1_T(50 pF) + 3 × 10⁻³ (C_L -50) V_{DD}

where: 1_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.

*The formulas given are for the typical characteristics only at 25°C.

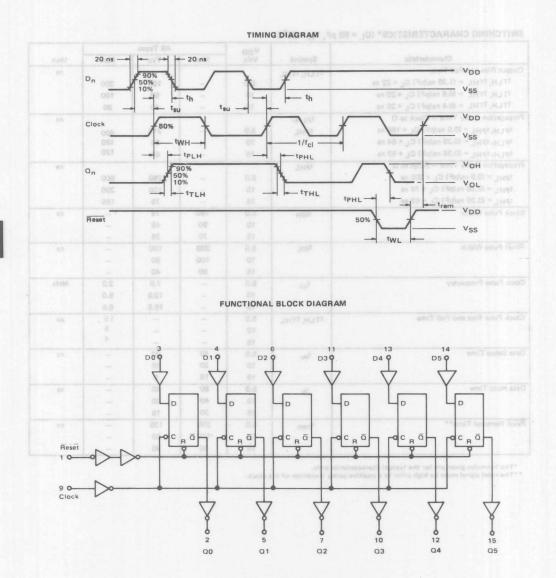
SWITCHING CHARACTERISTICS* (CL = 50 pF, TA = 25°C)

		VDD		All Types		
Characteristic	Symbol	Vdc	Min	Тур	Max	Unit
Output Rise and Fall Time	tTLH, tTHL	prince		200		ns
tTLH, tTHL = (1.35 ns/pF) CL + 32 ns	1 1	5.0	\	100	200	1
tTLH, tTHL = (0.6 ns/pF) CL + 20 ns	.0	10	- 41	50	100	
[†] TLH, [†] THL = (0.4 ns/pF) C _L + 20 ns		15	oT - To	40	80	
Propagation Delay Time - Clock to Q	tPLH,		1		RealS	ns
tpLH, tpHL = (0.9 ns/pF) CL + 165 ns	TPHL	5.0	1-	210	400	
tpLH, tpHL = (0.36 ns/pF) CL + 64 ns	1/10	10		85	160	
tpLH, tpHL = (0.26 ns/pF) CL + 52 ns	Jeer-H	15	-10 JHT	65	120	
Propagation Delay Time - Reset to Q	tPHL		- 350	3	-	ns
tpHL = (0.9 ns/pF) CL + 205 ns	1	5.0	- 8	250	500	
tpHL = (0.36 ns/pF) C ₁ + 79 ns	33477	10	Bay!	100	200	
tpHL = (0.26 ns/pF) CL + 62 ns	et. Jeer on a	15	152.11	75	150	
Clock Pulse Width	tWH	5.0	150	75	-	ns
A MON		10	90	45	780071	
		15	70	35		
leset Pulse Width	tWL	5.0	200	100	-	ns
		10	100	50		
		15	80	40	_	
Clock Pulse Frequency	fcl	5.0	_	7.0	2.0	MHz
		10	-	12.0	5.0	
	SLOCK DIAGRAM	15	-	15.5	6.5	
Clock Pulse Rise and Fall Time	tTLH, tTHL	5.0	-	-	15	μя
		10	-	-	5	
		15	-	_	4	
Data Setup Time	t _{su}	5.0	40	20	-	ns
	100	10	20	10	_	
	77 7	7 15	15.	0	-	
Data Hold Time	th	5.0	80	40	_	ns
		10	40	20	_	
		15	30	15	_	
Reset Removal Time**	trem	5.0	250	125	-	ns
	ala da ala	10	100	50	_	
		15	80	40		Best

^{*}The formulas given are for the typical characteristics only.

**The reset signal must be high prior to a positive-going transition of the clock.







MC14175B

QUAD TYPE D FLIP-FLOP

The MC14175B quad type D flip-flop is constructed with MOS Pchannel and N-channel enhancement mode devices in a single monolithic structure. Each of the four flip-flops is positive-edge triggered by a common clock input (C). An active-low reset input (R) asynchronously resets all flip-flops. Each flip-flop has independent Data (D) inputs and complementary outputs (Q and Q). These devices may be used as shift register elements or as type T flip-flops for counter and toggle applications.

- Complementary Outputs
- Static Operation
- All Inputs and Outputs Buffered
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Noise Immunity = 45% of VDD typical
- Output Compatible with Two HTL Loads, Two Low-Power TTL Loads or One Low-Power Schottky TTL Load
- Functional Equivalent to TTL 74175

MAXIMUM RATINGS (Voltages referenced to Vsc)

Rating	Symbol	Value	Unit
DC Supply Voltage	V _{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	Vin	-0.5 to V _{DD} + 0.5	Vdc
DC Current Drain per Pin	0/ 1_	00 10	mAdc
Operating Temperature Range – AL Device CL/CP Device	TA	-55 to +125 -40 to +85	°C
Storage Temperature Range	T _{stg}	-65 to +150	°C

TRUTH TABLE (Postive Logic)

	INPUTS		OUT	PUTS	
Clock	Data	Reset	Q	Q	- 0
	0	1	0	nist 1 x	nav 0
	1	1	1	0	onve
~	X	1	Q	ā	No Change
X	×	0	0	1	Change

X = Don't Care

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper

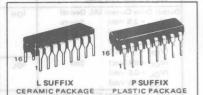
operation it is recommended that Vin and V_{out} be constrained to the range $V_{SS} \le (V_{in} \text{ or } V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD).

CMOS SSI

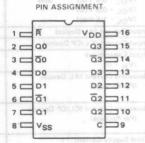
(LOW-POWER COMPLEMENTARY MOS)

QUAD TYPE D FLIP-FLOP

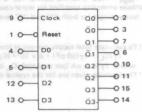


CASE 620

CASE 648



BLOCK DIAGRAM



V_{DD} = Pin 16 VSS = Pin 8

ELECTRICAL CHARACTERISTICS

		VDD	Tic	w*		25°C	100	Thi	gh	
Characteristic	Symbol	Vdc	Min	Max	Min	Тур	Max	Miri	Max	Unit
Output Voltage "0" Level	VOL	5.0	-	0.05	-	0	0.05	-	0.05	Vdc
Vin = VDD or 0		10	-	0.05	-	0	0.05	-	0.05	1
		15	-	0.05	-	0	0.05	-	0.05	
"1" Level	VOH	5.0	4.95	-	4.95	5.0	_	4.95	-	Vdc
V _{in} = 0 or V _{DD}	0	10	9.95	-	9.95	10	-	9.95	-	
ree-enum		15	14.95	- 9	14.95	15	YT-GA	14.95	-	
Input Voltage# "0" Level	VIL									Vdc
(V _O = 4.5 or 0.5 Vdc)		5.0	SOH HIS	1.5	sings at	2.25	1.5	1758 a	1.5	1
(V _O = 9.0 or 1.0 Vdc)	11	10	non-sing	3.0	ivel ab	4.50	3.0	neitto-M	3.0	chan
(V _O = 13.5 or 1.5 Vdc)		15	-	4.0	-	6.75	4.0	diam at	4.0	origin.
"1" Level	VIH		Total Control	mine you	a month	ma at 1	D) rugg	shoots re	PHENON'S	out
(V _O = 0.5 or 4.5 Vdc)		5.0	3.5		3.5	2.75		3.5	n vii uon	Vdc
(V _O = 1.0 or 9.0 Vdc)		10	7.0	aristvii s	7.0	5.50	mon-du	7.0	n yeucen	(0)
(V _O = 1.5 or 13.5 Vdc)		15	11.0	(1 _(13	11.0	8.25	ercialities	11.0	a striden	107
Output Drive Current (AL Device)	ТОН	-	edo.	1.00	7 00 10	-	THE PERSON NAMED IN	71777		mAdo
(VOH = 2.5 Vdc) Source	.Un	5.0	-3.0	_	-2.4	-4.2	noitsaile	-1.7	bns res	ngs.
(V _{OH} = 4.6 Vdc)		5.0	-0.64	_	-0.51	-0.88	_	-0.36	_	
(VOH = 9.5 Vdc)	200	10	-1.6	_	-1.3	-2.25	ETUQT	-0.9	ompleme	0
(V _{OH} = 13.5 Vdc)	602	15	-4.2	_	-3.4	-8.8	_	-2.4	ag O-size:	0
(VOI = 0.4 Vdc) Sink	loL	5.0	0.64	-	0.51	0.88	hulf-shirt	0.36	etueni li	mAdo
(V _{OL} = 0.5 Vdc)	OL	10	1.6	_	1.3	2.25		0.9		
(V _{OL} = 1.5 Vdc)		15	4.2	_	3.4	8.8	ani TiA.	2.4	וספת דרס	9 0
Output Drive Current (CL/CP Device)	The second	13	7.2		0.4	0.0	1.0	- Carrier	W yiqq	mAdo
DES UZAZI	ЮН	5.0	-2.5		-2.1	-4.2	1 to 288	-1.7	nmt_salo	MAGG
011		5.0	-0.52		-0.44	-0.88	THIW	-0.36	iO regru	0
(V _{OH} = 4.6 Vdc)	annual	10	-1.3	WORLD DI	-1.1	-2.25		-0.9		
(V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc)		15	-3.6	_	-3.0	-8.8	Power S	-2.4) nember	
• • • • • • • • • • • • • • • • • • • •			-	-	-	10 1 10 10 1	1 705 101	ALCO AND TO	COUNTY TOTAL	
(VOL = 0.4 Vdc) Sink	IOL	5.0	0.52	-	0.44	0.88	=	0.36	-	mAdd
(V _{OL} = 0.5 Vdc)		10	1.3	-	1.1	2.25	-	0.9	-	
(V _{OL} = 1.5 Vdc)		15	3.6	-	3.0	8.8	-	2.4	-	-
nput Current (AL Device)	lin	15	-	± 0.1	-	±0.00001	± 0.1	-	±1.0	μAdd
Input Current (CL/CP Device)	lin	15	-	± 0.3	- 10	±0.00001	± 0.3	GS tyou	±1.0	μAdd
nput Capacitance (V _{in} = 0)	Cin	zīħU	-	ola V	lown	5.0	7.5	gnizsfi	-	pF
Quiescent Current (AL Device)	IDD	5.0	-	5.0	- 00)	0.005	5.0	-	150	μAdo
(Per Package)	יטטי	10	80 0	10	Low	0.010	10	100	300	-
11-150		15	-	20	- 1	0.015	20	_ 0/	600	20197110
Quiescent Current (CL/CP Device)	lon	5.0	_827	20	I A	0.005	20	1075.71	150	μAdd
(Per Package)	IDD	10	38	40		0.005	40	CL	0.000	ДАО
(Fer Fackage)		15	150_	80		0.015	80	_spms/	300 600	me Test
Total Supply Current**†	I-		-	1 80	1				600	1
(Dynamic plus Quiescent,	IT	5.0				.7 μA/kHz)				μAdd
						3.4 μA/kHz)				
Per Package) (C ₁ = 50 pF on all outputs, all		15			17 = (5	5.0 μA/kHz)				
buffers switching)										1

^{*}T_{IOW} = -55°C for AL Device, -40°C for CL/CP Device.
Thigh = +125°C for AL Device, +85°C for CL/CP Device.

#Noise immunity specified for worst-case input combination.

Noise Margin for both "1" and "0" level = 1.0 Vdc min @ VDD = 5.0 Vdc

2.0 Vdc min @ VDD = 10 Vdc
2.5 Vdc min @ VDD = 15 Vdc

1 To calculate total supply current at loads other than 50 pF:

1 T(CL) = 1 T(50 pF) + 4 x 10⁻³ (CL - 50) VDDf

where: $T_1 = T_1 = T_2 = T_3 = T_3 = T_4

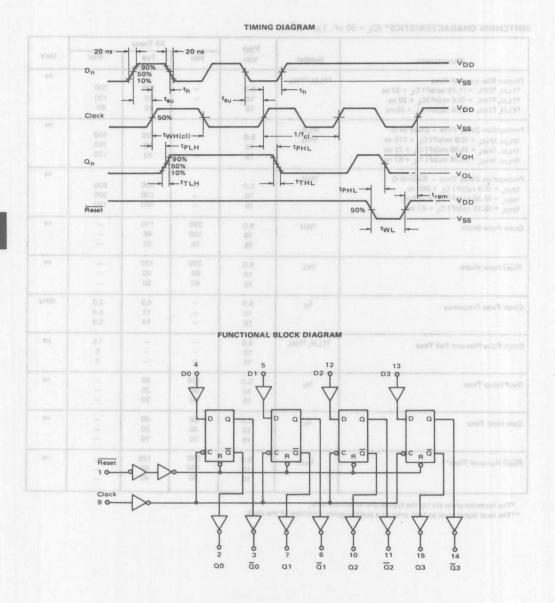
SWITCHING CHARACTERISTICS* (CL = 50 pF, TA = 25°C)

		V _{DD}		All Types		Unit
Characteristic	Symbol	Vdc	Min	Тур	Тур Мах	
Output Rise and Fall Time	tTLH, tTHL	A		2017	1620	ns
tTLH, tTHL = (1.35 ns/pF) C _L + 32 ns	TEH, THE	5.0	- 4-	100	200	
tTLH, tTHL = (0.6 ns/pF)C ₁ + 20 ns	0, 1	10	_ "	50	100	
tTLH, tTHL = (0.4 ns/pF) CL + 20 ns		15	-	40	80	
Propagation Delay Time - Clock to Q	tPLH,	1	-/	T	-	ns
tpLH, tpHL = (0.9 ns/pF) CL + 175 ns	tPHL	5.0	h=-(b)H	220	400	
tpLH, tpHL = (0.36 ns/pF) CL + 72 ns	JH91	10	HJ107	90	160	
tpLH, tpHL = (0.26 ns/pF) CL + 57 ns		15	- 266	70	120	
Propagation Delay Time — Reset to Q	tPHL		201	7	1000	ns
tpHL = (0.9 ns/pF) CL + 280 ns	7 19 7 on 19 1	5.0	81172-1	325	500	
tpHL = (0.36 ns/pF) C ₁ + 112 ns		10	-	130	200	
tpHL = (0.26 ns/pF) CL + 87 ns	2	15	-	100	150	
Clock Pulse Width	tWH	5.0	250	110	-	ns
		10	100	45	-	
		15	75	35	-	
Reset Pulse Width	tWL	5.0	200	100	-	ns
		10	80	40	-	
		15	60	30	-	1
Clock Pulse Frequency	f _{cl}	5.0	-	4.5	2.0	МН
olour raise risquality		10	-	11	5.0	
		15	-	14	6.5	
Clock Pulse Rise and Fall Time	tTLH, THL	5.0	-	-	15	μs
		10	-	-	5	
61	12	15		-	4	
Data Setup Time	t _{su}	5.0	120	60	-	ns
	N/	10	50	25	-	1
Y .		15	40	20	_	
Data Hold Time	th o	5.0	80	40	-	ns
		10	40	20	-	
		15	30	15	-	
Reset Removal Time**	trem	5.0	250	125	Tago FI	ns
		10	100	50	-0-	
		15	80	40	-	

^{*}The formulas given are for the typical characteristics only.

**The reset signal must be high prior to a positive-going transition of the clock.





MC14194B



4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTER

*The MC14194B is a 4-bit static shift register capable of operating in the parallel load, serial shift left, serial shift right, or hold mode. The asynchronous Reset input, when at a low level, overrides all other inputs, resets all stages, and forces all outputs low. When Reset is at a logic 1 level, the two mode control inputs, SO and S1, control the operating mode as shown in the truth table. Both serial and parallel operation are triggered on the positive-going transition of the Clock input. The Parallel Data, Data Shift, and mode control inputs must be stable for the specified setup and hold times before and after the positive-going Clock transition.

> TRUTH TABLE INPUTS

(Reset = 1)

× X

DSR DSL

X

X

- Quiescent Current = 5.0 nA typ/pkg @ 5 Vdc
- Typical Shift Frequency = 9.0 MHz @ 10 Vdc
- Synchronous Right/Left Serial Operation
- Synchronous Parallel Load
- Asynchronous Hold (Do Nothing) Mode

S1

0 0 X ×

0 1 0 X

0

1

SO

0 X 0

0 X

1

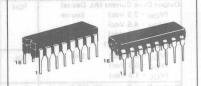
1 X

Functional Pin for Pin Equivalent of 74194

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

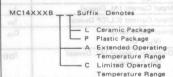
4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTER



SHEELY CERAMIC PACKAGE CASE 620

PSUFFIX PLASTIC PACKAGE CASE 648

ORDERING INFORMATION



X = Don't Care

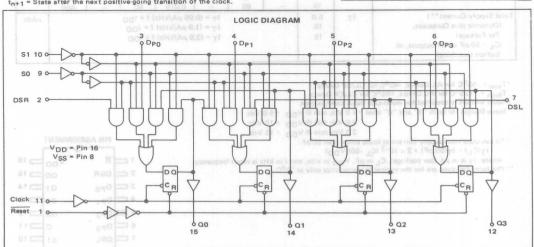
Shift Left

Shift Right

Parallel

OPERATING MODE

tn+1 = State after the next positive-going transition of the clock.



OUTPUTS (@ tn + 1)

02 03 1

00

03

02

00 Q1 02 03

00 01 02 0

01 02 03

0 00 01 02

0 0 0 0

1 1 1 1

DP0-3

×

X

X

0

		VDD	Tie	ow*		25°C		Th	igh [*]	
Characteristic	Symbol	Vdc	Min	Max	Min	Тур	Max	Min	Max	Unit
Output Voltage "0" Level	VOL	5.0	-	0.05	-	0	0.05		0.05	Vdc
Vin VDD or 0	1	10	-	0.05	-	0	0.05	-	0.05	
		15	-	0.05	-	0	0.05	-	0.05	100
"1" Level	VOH	5.0	4.95	-	4.95	5.0	-	4.95		Vdc
Vin O or VDD	011	10	9.95	R THE	9.95	10	JAMO	9.95	HOLS T	8-9
		15	14.95	-	14.95	15	_	14.95	_	
nput Voltage " "0" Level	VIL	- 8	tis rado	n ajminh	1 myrigh	China Sing	2 11/2-6- 9	of Open	F1 J10 101	Vdc
(VO - 4.5 or 0.5 Vdc)	110	50	born bie	15	o riligia i	2.25	1.5	load, sa	1.5	T. CIL
(VO 9.0 or 1.0 Vdc)		10	errigies	3.0	evol_s 1	4.50	3.0	nous fr	3.0	- Fhs
(V _O = 13.5 or 1.5 Vdc)		15	rIW_we	4.0	d fla_29:	6.75	4.0	etwen :	4.0	edito
"1" Level	VIH	13	d bas 08	stugni	manos	0.75	Arth Jav	[58b0	8 Ju 21 J	Jari
(V _O = 0.5 or 4.5 Vdc)	HI	5.0	3.5	alder e	3.5	2.75	es abom	3.5	o edy lor	Vdc
(VO = 1.0 or 9.0 Vdc)		10	7.0	TOTAL TO		5.50	alan mani	7.0	letterso	bos
(VO = 1.5 or 13.5 Vdc)		15	11.0	State - On	7.0	8.25	December 1	11.0	No=O-eck	e to
		15	11.0	om the	11.0	8.25	SIB FOT DE			-
Output Drive Current (AL Device)	ІОН	91	nes hetc	hold til	INE QUIT	perlined:		eldata s	tenun at	mAd
(V _{OH} = 2.5 Vdc) Source		5.0	-3.0	7	-2.4	-4.2	ping-Cid	-1.7	oriz-reste	bos
(V _{OH} = 4.6 Vdc)		5.0	-0.64	-	-0.51	-0.88	N-03	-0.36	Inspatiu	0 0
(V _{OH} = 9.5 Vdc)	Titles	10	-1.6	-	-1.3	-2.25	AnLO.d	-0.9	1	
(V _{OH} = 13.5 Vdc)	202	15	-4.2	-	-3.4	-8.8	B-yons	-2.4	HS lealey	-
(VOL = 0.4 Vdc) Sink	IOL	5.0	0.64	-	0.51	0.88	Leit-Ser	0.36	onewleny	mAd
(V _{OL} = 0.5 Vdc)	- une	10	1.6	-	1.3	2.25	bato J lis	0.9	enon/sm	2 8
(VOL = 1.5 Vdc)	1	15	4.2	-	3.4	8.8	NATIONAL PROPERTY.	2.4	most onve	
Output Drive Current (CL/CP Device)	ГОН						No. 2 and	wat ald	man vani	mAde
(VOH = 2.5 Vdc) Source	0	5.0	-2.5	-	-2.1	-4.2	in Equit	-1.7		1
(V _{OH} = 4.6 Vdc)	ARSO	5.0	-0.52		-0.44	-0.88	-	-0.36	-	
(VOH = 9.5 Vdc)		10	-1.3	-	-1.1	-2.25	-	-0.9	-	
(V _{OH} = 13.5 Vdc)		15	-3.6		-3.0	-8.8	187	-2.4	-	
(VOI = 0.4 Vdc) Sink	IOL	5.0	0.52	- 1	0.44	0.88		0.36	-	mAd
(V _{OL} = 0.5 Vdc)	.OL	10	1.3		1.1	2.25	_	0.9	_	
(V _{OL} = 1.5 Vdc)	11	15	3.6	-	3.0	8.8	T. T.	2.4	LATING	1390
nput Current (AL Device)	I.	15	0.0	± 0.1	0.0	± 0.00001	± 0.1	12-1	± 1.0	μAdo
THE RESERVE AND THE PARTY OF TH	in	15	10	± 0.1	V- 1	±0.00001	± 0.3	0]	±1.0	иAdd
nput Current (CL/CP Device)	lin	17	10 T co	₹ 0.5	N. I	17				
nput Capacitance (V _{in} = 0)	Cin	T 20	0 00	170	× ·	5.0	12.0	0	-	pF
Quiescent Current (AL Device)	IDD	5.0	D T OD	5.0	X-1	0.005	5.0	0 7	150	μAde
(Per Package)		10	0 1 0	10	0-1	0.010	10	Y =	300	
Remark interestment		15		20	-	0.015	20		600	10
Quiescent Current (CL/CP Device)	¹DD	5.0		20		0.005	20		150	μAd
(Per Package)	00	10	-	40	-	0.010	40	-	300	Produ
		15	_	80	die clook	0.015	80	FIRSQ TXB/	600	mig -
otal Supply Current**†	IT	5.0			1- = 11				000	μAd
(Dynamic plus Quiescent,	.1	10							ДАО	
Per Package)		15				2.9 µA/kHz)				
(C ₁ = 50 pF on all outputs, all	030	15	1111	1000	11 - 12	MM/KI12/	000			
TOE JO PE OII all Outputs, all										0 00 0

^{*}Tlow = -55°C for AL Device, -40°C for CL/CP Device.

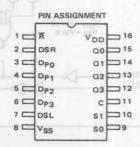
Thigh = +125°C for AL Device, +85°C for CL/CP Device.

#Noise immunity specified for worst-case input combination.

Noise Margin for both "1" and "0" level = 1.0 Vdc min @ VDD = 5.0 Vdc

2.0 Vdc min @ VDD = 10 Vdc 2.5 Vdc min @ VDD = 15 Vdc

†To calculate total supply current at loads other than 50 pF: $I_{T}(C_{L}) = I_{T}(50 \text{ pF}) + 2 \times 10^{-3} \text{ (}C_{L} - 50\text{) V}_{DD}f$ where: $I_{T} \text{ is in } \mu\text{A (per package), } C_{L} \text{ in pF, V}_{DD} \text{ in Vdc, and f in kHz is input frequency.}$ *The formulas given are for the typical characteristics only at 25°C.



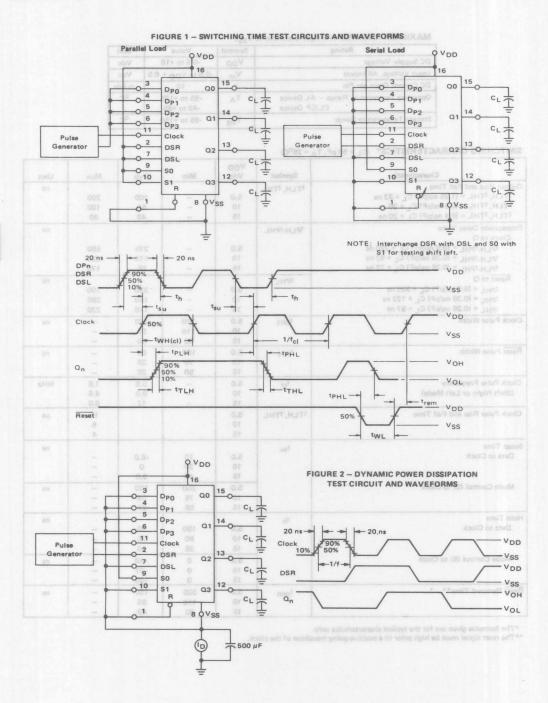
MAXIMUM RATINGS (Voltages referenced to V_{SS})

bas Island Rating	Symbol	Value	Unit
DC Supply Voltage	V _{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	Vin	-0.5 to V _{DD} + 0.5	Vdc
DC Current Drain per Pin	- bar	00 10 0	mAdd
Operating Temperature Range – AL Device CL/CP Device	TA	-55 to +125 -40 to +85	°C
Storage Temperature Range	T _{stg}	-65 to +150	°C

Characteristic	Symbol	V _{DD} Vdc	Min	Тур	Max	Unit
Output Rise and Fall Time tTLH, tTHL = (1,35 ns/pF) C _L + 32 ns tTLH, tTHL = (0.6 ns/pF) C _L + 20 ns tTLH, tTHL = (0.4 ns/pF) C ₁ + 20 ns	^t TLH, ^t THL	5.0 10 15	vo a o	100 50 40	200 100 80	ns
Propagation Delay Time Clock to Q tp_H,tpHL = (0.9 ns/pF) CL + 230 ns tp_H,tpHL = (0.36 ns/pF) CL + 92 ns tp_H,tpHL = (0.26 ns/pF) CL + 72 ns	tpLH,tPHL	5.0 10 15	= 05 + -	275 110 85	550 220 170	ns
Reset to Q tpHL = (0.9 ns/pF) CL + 305 ns tpHL = (0.36 ns/pF) CL + 122 ns tpHL = (0.26 ns/pF) CL + 97 ns	tPHL	5.0 10 15	= -	350 140 110	700 280 220	ns
Clock Pulse Width	twH	5.0 10 15	280 110 85	140 55 40	-100D	ns
Reset Pulse Width	tWH	5.0 10 15	180 70 50	90 35 26	- 40	ns
Clock Pulse Frequency (Shift Right or Left Mode)	f _{Cl}	5.0 10 15	10/27	3.6 9.0 12	1.8 4.5 6.0	MHz
Clock Pulse Rise and Fall Time	tTLH, tTHL	5.0 10 15			15 5 4	μs
Setup Time Data to Clock MOUTA 41231G 133401 DIMANYO - E 2010 Mode Control (S) to Clock	^t su	5.0 10 15 5.0	10 20 40 200 75	-8.0 0 9.0 100 36	-	ns
Hold Time Ďata to Clock	t _h	5.0	180	90	d -	ns
OGV MOS S	T Class	10	50 35	25 10	# .	No.
Mode Control (S) to Clock	seo I	5.0 10 15	0 0	-40 -27 -20	-	ns
Reset Removal Time**	trem	5.0 10 15	300 110 80	150 55 40	=	ns

*The formulas given are for the typical characteristics only.

**The reset signal must be high prior to a positive-going transition of the clock.





QUAD PRECISION TIMER/DRIVER

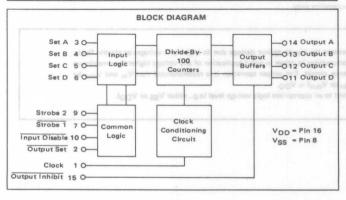
The MC14415 quad timer/driver is constructed with complementary MOS enhancement mode devices. The output pulse width of each digital timer is a function of the input clock frequency. Once the proper input sequence is detected the output buffer is set (turned on), and after 100 clock pulses are counted, the output buffer is reset (turned off).

The MC14415 was designed specifically for application in high speed line printers to provide the critical timing of the hammer drivers, but may be used in many applications requiring precision pulse widths.

- Four Precision Digital Time Delays
- Schmitt Trigger Clock Conditioning
- NPN Bipolar Output Drivers
- Timing Disable Capability Using Inhibit Output
- Positive or Negative Edge Strobing on the Inputs
- Synchronous Polynomial Counters Used for Delay Counting
- Power Supply Operating Range
 - = 3.0 Vdc to 18 Vdc (MC14415EFL/FL/FP)
 - = 3.0 Vdc to 6.0 Vdc (MC14415EVL/VL/VP)

MAXIMUM RATINGS (Voltages referenced to VSS, Pin 8)

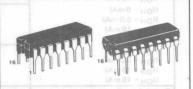
Rating	Symbol	Value	Unit
DC Supply Voltage	VDD		Vdc
- MC14415EFL/FL/FP	-	+18 to -0.5	
- MC14415EVL/VL/VP	-	+6.0 to -0.5	01
Input Voltage, All Inputs — 9000000	Vin	V _{DD} +0.5 to V _{SS} -0.5	Vdc
DC Current Drain per Input Pin	lin	10	mAdc
DC Current Drain per Output Pin	lout	20	mAdc
Operating Temperature Range - MC14415EFL/EVL	TA	-55 to +125	°C
- MC14415FL/FP/VL/VP		-40 to +85	144 1551
Storage Temperature Range	T _{stg}	-65 to +150	°C



CMOS LSI

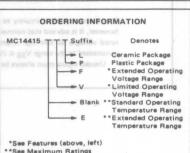
(LOW-POWER COMPLEMENTARY MOS)

QUAD PRECISION TIMER/DRIVER



L SUFFIX CERAMIC PACKAGE CASE 620 P SUFFIX PLASTIC PACKAGE CASE 648





ELECTRICAL CHARACTERISTICS

		VDD	TI	ow*		25°C		Th	igh*	
Characteristic	Symbol	Vdc	Min	Max	Min	Тур	Max	Min	Max	Unit
Output Voltage "0" Level	Vout	5.0	-	0.01	-	0	0.01	-	0.05	Vdc
(No Load)	001	10	-	0.01	-	0	0.01	-	0.05	
		15	_	-	-	-	-	-	-	
"1" Level		5.0	-	PEV	3.0	4.14	RECHSI	9 GAU	0 -	Vdc
		10	_	-	8.0	9.09	-	-	-	
		15	nomen d	Since Transfer	100 To 10	14.12	non-	o BIM	COLT AN	
Noise Immunity	VNL	- 4	biw estr	a diametrica	ody so	Junty afters	n thancie	nedne 2	DAT VIE	Vdd
(△V _{out} ≤ 1.5 Vdc)		5.0	1.5	1000000	1.5	2.25	ut T di	1.4	Initia-des	n 100
(△V _{out} ≤ 3.0 Vdc)		10	3.0	Kalaia h	3.0	4.50	uanbas z	2.9	sto ett	Onc
(△V _{out} ≤ 4.5 Vdc)	(a)	15	Sal Journ	d trighto	919 0000	6.75	Mandans 2	July 100	/au lan	DING
(△V _{out} ≤ 1.5 Vdc)	VNH	5.0	1.4	Appropriate to the same of the	1.5	2.25	744	1.5	-	Vdc
(△V _{out} ≤ 3.0 Vdc)		10	2.9	-	3.0	4.50	7110	3.0	pital of 1	11183
(△V _{out} ≤ 4.5 Vdc)		15	id ai no	iteoilggs	10T_VIN	6.75	engiseb :	M GIG	HISM or	
Output Drive Voltage (NPN Driver)	Vон	- 19	- 11 miles	10 KS (ET)	1011 80-01	1357 1914 1	experiency of	5-10/110	N SERVE	Vdd
(IOH = 0 mA) Source	OII	5.0	precision	chillipa	3.0	4.14	(III Dast	ad_Asu	1110 31	MALIE -
(IOH = 5.0 mA)			-	-	2.7	3.44	-	-	artiti <u>n</u> ius	stad
(I _{OH} = 10 mA	-		-	-	2.5	3.30	emi T lat	sig mole	091 ⁴ 1U0	8 0
(IOH = 15 mA)			-	-	2.2	3.08	and Date	Et Samuel	T. stimel	0 8
(I _{OH} = 0 mA)		10	-	- 1	8.0	9.09		-	-	Vde
(I _{OH} = 5.0 mA)			-	-	7.7	8.45	nav <u>b</u> Q a	epuD 18	onie Ma	11.0
(I _{OH} = 10 mA)			-		7.5	8.30	d v ri tide	able Car	O gmim	T 0
(IOH = 15 mA)	Short 1		-	-	7.1	8.14	2 To 3	- ale	-	0 4
(I _{OH} = 0 mA)		15	-	-	-	14.12	_	-	-	Vdd
(I _{OH} = 5.0 mA)	W Uar		<u> </u>	ud Q_ysla	G rol bs	13.81	iomi <u>a</u> l Co	us Eoly	anougan.	3 0
(I _{OH} = 10 mA)			-	-	-	13.70	all mits	so O- yla	Sug Town	9.0
(I _{OH} = 15 mA)			-	#99\	13/133	13.61	18 Vide	es ob V	.8 -	
Output Drive Current	IOL			1977	MA INTE	TABTOM!	ab V 0.8	or obV	18 =	mAd
(VOL = 0.4 Vdc) Sink		5.0	0.23	-	0.20	0.78	-	0.16	-	
(VO) = 0.5 Vac)	CERM	10	0.60	-	0.50	2.0	-	0.40	-	
(VOL = 1.5 Vdc)		15	-	-	-	7.8	-	-	-	
nput Leakage Current	lin	-	-	-	-	10	-		arri a	pAd
nput Capacitance	Cin	_	-	-	- B	5.0	- notice	-	-	pF
(V _{in} = 0)			101	EaV	Evinter)			gerited		
Quiescent Dissipation	Pa	Vola			OOV				egutio	mV
PHN ASSIGNMENT		5.0	-3.0-	0.25	-	0.00005	0.25	NOTHER	3.5	
		10	25.0-	1.0	-	0.00022	1.0	NC14415	14	
		15 V	- B.	+ act/	el ⁴	0.00050	-	- 171	and Feb. s	stipV n
ower Dissipation**	PD		8:0-	28V				-		mV
(Dynamic plus Quiescent)										themuS
(C ₁ = 15 pF)	P 18	5.0			PD = (5	66 mW/MHz) f + Po			memus
CI CON BINO BISS CON		10				25 mW/MH				T onite
SCT 880 0 0 0 0 0 0		15	300			10 mW/MH				British)

^{*}T_{IOW} = -55°C for MC14415EFL, EVL; -40°C for MC14415FL,FP,VL,VP Thigh = +125°C for MC14415EFL,EVL; +85°C for MC14415FL,FP,VL,VP

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range V_{SS} \leq (V_{in} or V_{out}) \leq V_{DD}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD).

^{* *} The formulae given are for the typical characteristics only.

SWITCHING CHARACTERISTICS (CL = 15 pF, TA = 25°C)

Characteristic	Symbol	V _{DD} Vdc	Min	Тур	Max	Unit
Output Rise Time* tr H = (2.0 ns/pF) C _L + 10 ns	tTLH	5.0	_	40	85	ns
t _{T1 H} = (1.25 ns/pF) C ₁ + 6 ns		10	_	25	60	
t _{TLH} = (1.10 ns/pF) C _L + 3 ns		15		20		stdestO rue
Output Fall Time*	tTHL	1		1	5	ns
t _{THL} = (1.5 ns/pF) C _L + 47 ns	1112	5.0	-	70	150	
t _{THL} = (0.75 ns/pF) C _L + 24 ns		10	Eco mus	35	80	Strobe
t _{THL} = (0.55 ns/pF) C _L + 17 ns		15	Roo mud	25	_	. 102
Turn-Off Delay Time*	tPLH	10 411 980	-	-	F-500	ns
tpLH = (2.7 ns/pF) CL + 560 ns		5.0	-	600	1200	red ruszud
tpHI = (1.2 ns/pF) C ₁ + 282 ns		10	_	300	600	ing sugars
tpLH = (0.91 ns/pF) CL + 286 ns		15	-	150	-	lidetal rug
Turn-On Delay Time*	tPHL	1	process.	-	promp	ns
tpHL = (2.4 ns/pF) CL + 564 ns	1116001	5.0		600	1200	ROOK
tpHL = (1.0 ns/pF) CL + 285 ns		10	2408 1	300	600	A rugrodi
tpHL = (0.75 ns/pF) CL + 289 ns		15	-	150	-	
Turn-On Delay Time (Inhibit to Output)	tPHL		HJ	92.		ns
		5.0	-	300	550	
		10	_	225	425	
		15	-	110	-	
Turn-Off Delay Time (Inhibit to Output)	tPLH	1	_		1	ns
		5.0	-	300	550	
		10	-	225	425	
		15	_	110	_	
Input Pulse Coincidence (Figure 3)	PCmin	1				ns
		5.0	500	450	-	
		10	450	350	-	
		15	-	-	-	
Input Pulse Width (Figure 1)	twH	1.				ns
		5.0	500	450	_	
MODE 6: POSITIVE-EDDE STRODE (ST2) INITIATES TIME DELAY	YAJED 3	10	450	350	FUCLIS 3	61016
		15	-	-	-	
Input Clock Frequency	fcl		1			MHz
Input Disable	0.	5.0	-	0.7	-	elstade to
		10	-	1.0		
\$1:00x 2 10x		15	-	1.5	-	Surphy ?
Clock Input Rise and Fall Times (Figure 1)	tTLH, tTHL	5.0	-	-	15	μs
		10	-	-	5.0	aquits
SO A - 00 V 0 M 000 - 4.76 V 00		15	-	/ FL 20	4.0	5.782

^{*}The formulae given are for the typical characteristics only.

FIGURE 1 – SWITCHING CHARACTERISTICS – WAVEFORM RELATIONSHIPS

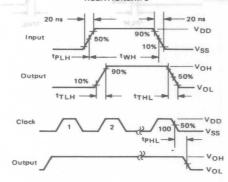
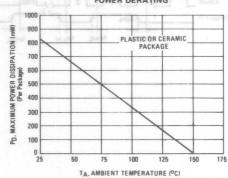
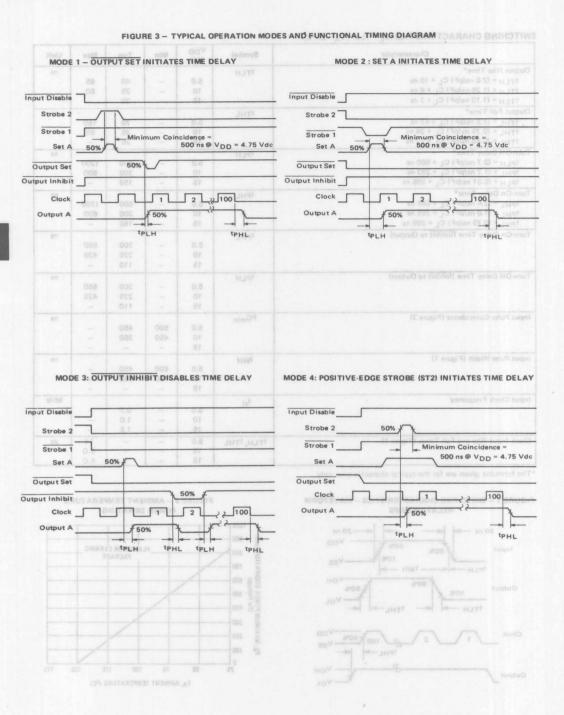
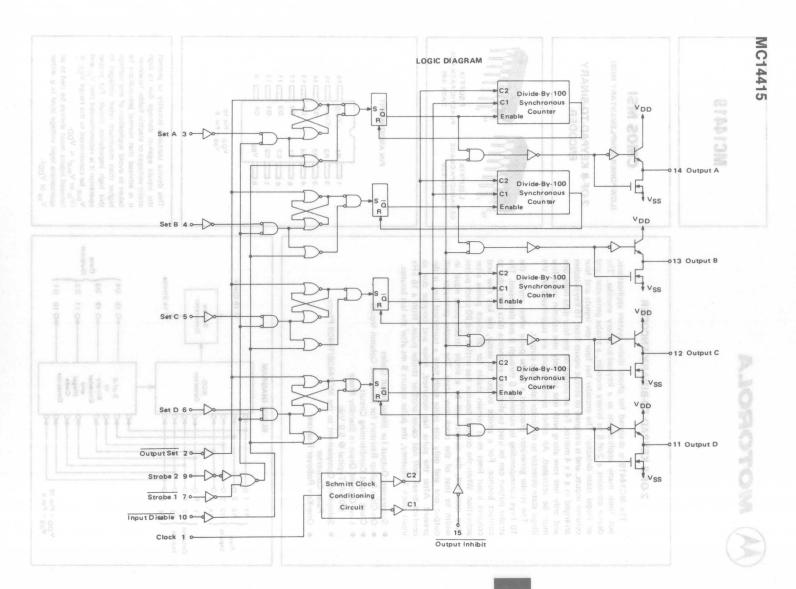


FIGURE 2 – AMBIENT TEMPERATURE POWER DERATING











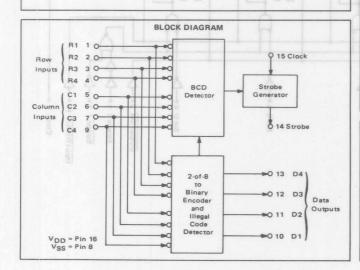
MC14419

2-OF-8 KEYPAD-TO-BINARY ENCODER

The MC14419 is designed for phone dialer system applications, but finds many applications as a keypad-to-binary encoder. The device contains a 2-of-8 to binary encoder, a strobe generator, and an illegal state detector. The encoder has four row inputs and four column inputs, and is designed to accept inputs from 16 keyswitches arranged in a 4 x 4 matrix. For an output on the four data lines, one and only one row along with one and only one column input line must be activated. All other combinations are suppressed by the illegal state detector to eliminate false data output.

The strobe generator produces a strobe pulse when any of the 10 keys corresponding to numerals 0 through 9 are depressed. The strobe output can be used to eliminate erroneous data entry due to contact bounce. For a strobe output to occur, the key row and column input lines must remain stable for 80 clock pulses after activation. When the contact bounce has settled and 80 clock pulses have occurred, the output will be a single strobe pulse equal in width to that of the clock low state. The strobe generator will output one and only one pulse each time a numerical key is depressed. After the pulse has occurred, noise and bounce due to contact break will not cause another strobe pulse. With a 16 kHz input clock frequency, the pulse occurs 5 ms after the last bounce.

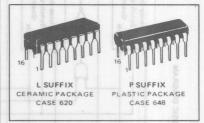
- Suppressed Output for Illegal Input Codes
- On-Chip Pullup Resistors for Row and Column Inputs
- Clock Input Conditioning Circuit
- Low Current Drain in Standby Mode
 5.0 μA Typical @ 5.0 Vdc
- Subsystem Complement to the MC14408/14409 Phone Pulse Converter
- One-Key Rollover Feature

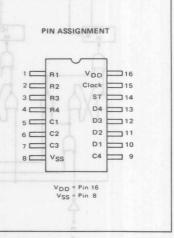


CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

2-OF-8 KEYPAD-TO-BINARY ENCODER





This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields: however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that $V_{\rm in}$ and $V_{\rm out}$ be constrained to the range $V_{\rm SS} \leqslant (V_{\rm in} \ {\rm or} \ V_{\rm DD}.$ Unused inputs must always be tied to an

unused inputs must always be fied to an appropriate logic voltage level (e.g. either V_{SS} or V_{DD}).

3

MAXIMUM-RATINGS (Voltages referenced to Vss., Pin 8.)

Rating	Symbol	Value	Unit	
DC Supply Voltage	V _{DD}	+6.0 to -0.5	Vdc	
Input Voltage, All Inputs	V _{in}	V _{DD} + 0.5 to V _{SS} -0.5	Vdc	
DC Current Drain per Pin	taV —	10	mAdo	
Operating Temperature Range	T _A	-40 to +85	o _C	
Storage Temperature Range	T _{stg}	-65 to +150	°C	

ELECTRICAL CHARACTERISTICS

		V _{DD}	-40	o°C		25°C		+85	°C	
Characteristic	Symbol	Vdc	Min	Max	Min	Тур	Max	Min	Max	Unit
Supply Voltage Operating Range	V _{DD}	Sultar	3.0	6.0	3.0	5.0	6.0	3.0	6.0	Vdc
Output Voltage "0" Level	Vout	5.0	-	0.05	-	0	0.05	-	0.05	Vdc
"1" Level		5.0	4.95	-	4.95	5.0	-	4.95	-	Vdc
Input Voltage "0" Level (VO = 4.5 or 0.5 Vdc)	VIL	5.0	1,5	-	1.5	2.25	60" 6 060	1.4	-	Vdc
"1" Level (V _O = 0.5 or 4.5 Vdc)	VIH	5.0	3.5	-	3.5	2.25	1/2	3.6	Raw or Column	Vdc
Output Drive Current (VOH = 2.5 Vdc) Source	ЮН	5.0	-0.23	un Tolle	-0.20	-1.7	-	-0.16	-	mAdc
(VOL = 0.4 Vdc) Sink	IOL	5.0	0.23	- 1	0.20	0.78	-	0.16	Strong Co	mAdc
Input Leakage Current (Vin = VDD)	ТІН	5.0	etro (VF nete	±0.1	eriš woli	±0.00001	±0.1	T2W9	±1.0	μAdc
Pullup Resistor Source Current (Row and Column Inputs) (Vin = VSS)	IIL	5.0	265	460	190	250	330	125	215	μAdc
Input Capacitance (Vin = VSS)	C _{in}	-	3.(8AT)	FURT	-	5.0	_	-	-	pF
Standby Supply Current	IDDS	3.0	-	3.0	-	1.0	3.0	-	6.0	μAdc
(f _{clock} = 16 kHz, No Keys Depressed)	thecoun	5.0 6.0	nma	15 60	WOR.	5.0	15 60	-	30 120	
Standby Supply Current as a Function of Clock Frequency* (No Keys Depressed)	IDDS	5.0	0 1	1 1	I _{DDS} = 0	.09 μA/kHz	+ 3.0 μΑ			μAdc

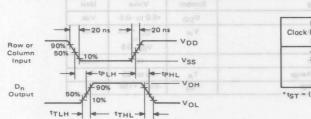
^{*}The formula given is for the typical characteristics only.

SWITCHING CHARACTERISTICS (C₁ = 50 pF, T_A = 25°C)

Characteristic	Symbol	VDD	Min	Тур	Max	Unit
Output Rise and Fall Times, D1 thru D4 (Figure 1)	tTLH, tTHL	5.0	1 - 1	300	-	ns
Propagation Delay Time, Row or Column Input to Data Output (Figure 1)	tPLH, tPHL	5.0	1-	1000	-	ns
Clock Pulse Frequency Range	PRF	3.0 to 6.0	n-	-	80	kHz



FIGURE 2 - TYPICAL STROBE PULSE DELAY TIMES



PRF Clock Frequency kHz	tST* Strobe Pulse Delay Time ms
4.0	20
8.0	10mmu0 00 10
16	5.0
32	2.5
80	1.0

*tST = (1/PRF) • 80, with PRF in kHz, tST in ms.

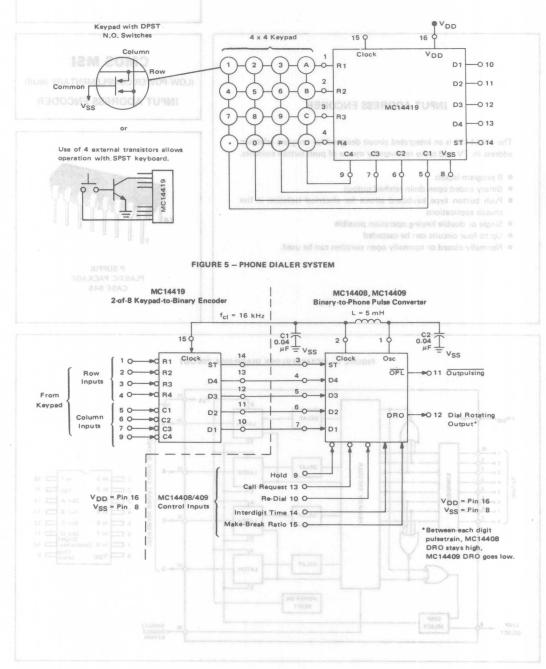
3

	RAM	DIAGR	TIMING	ENERATOR	ORE GE	RE 3 - STR	FIGUR				
		zun V	0.0		0.05	-	0				
	ntact reak ounce	Bre		Noise Spike			ontact Make ounce		5.7		
(ab V 6.9 to 6.0 = 0.7		////	8.0	3.6		2.5			8.6	Row or Column Input	
				PWST**	P	t _{ST} -	-1.3		87.0-		
Vol. = 0.4 Vdel Sink					-	80 Clock Pulses			enerator	Strobe G	
t Coarsos Current Vin * Vag)		HIT	(PWL).	Pulse Width	te Clock		ulse Width	Strobe F	**PWST	0.71	
				TH TABLE	TRU						
	Gr I	800	U.C		Inputs		0.	1			
		Outputs	0.8	olumn		Row	0.				
	Strobe		D4 D3 D	C3 C2 C1		4 R3 R2 R	Key** R4	Auto			
	777	0 1 1 0 1 1	0 0	1 1 0 1 0 1 0 1 1	1	1 1 0	1 1 2 1 3 1				
	7	0 1 1 0	0 1 0 1 0 1	1 1 1 1 1 0 1 0 1 0 1 1	1 1 1	1 0 1	A 1 1 5 1 6 1				
	0	0 1		1 1 1			B 1	gy	Dilan		
	7,	0 0		1 0 1			8 1	008			
	ئ	0 1 1 0	1 1	0 1 1 1 1	0	0 1 1	9 1 C 1	900	-		
	3	1 0 0 0 1 1	0 0	1 1 0 1 0 1 0 1 1	1	1 1 1 1	* 0 0 0 # 0				
	. 0	1 1	1 1	1 1 1	0	1 1 1	D 0				

^{* *}See Figure 4 for keypad designation.

MC14430

FIGURE 4 - TYPICAL KEYPAD INTERFACE APPLICATION



INPUT ADDRESS ENCODER

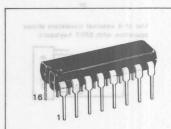
The MC14430 is an integrated circuit designed for program selection address in TV and radio receivers by means of push button switches.

- 8 program inputs
- Binary coded open drain latched output
- Push button type keyboard allows for electrical isolation in live chassis applications
- Single or double keying operation possible
- Up to four circuits can be cascaded
- Normally closed or normally open switches can be used.

CMOS MSI

(LOW POWER COMPLEMENTARY MUS)

INPUT ADDRESS ENCODER



P SUFFIX
PLASTIC PACKAGE
CASE 648

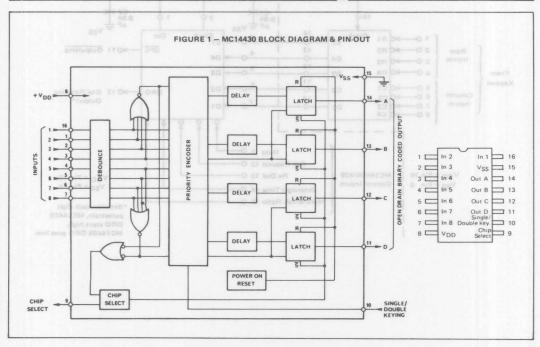


FIGURE 4 - TYPICAL KEYPAG INTERFACE APPLICATION

FIRE S - PHONE DIALER SYSTEM

E-049 - May 1979

3

MAXIMUM RATINGS (TA = 25 °C)

Rating	Symbol	Value	Unit	
DC Supply Voltage	V _{DD}	+10 to -0.5	Vdc	
Input Voltage, All Inputs	V _{in}	V _{DD} to -0.5	Vdc	
DC Current Drain per Pin	1	10	mAdo	
Operating Temperature Range	TA	0 to +70	°C	
Storage Temperature Range	T _{stg}	-65 to +150	°C	

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields: however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leqslant (V_{in} \text{ or } V_{out}) \leqslant V_{DD}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g. either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS (TA = 0 to 70°C)

Characteristics		Symbol	Min.	Тур.	Max.	Unit
Operating Supply Voltage	12 12	V _{DD}	4	5.2	6	Vdc
Quiescent Current per Package (Pins 16,1,2, 3,4,5,6,7 open or grounded)	V _{DD} = 5 V	IDD	-	0.068	10	μAdc
Input Voltage	"O" Level	V _{IL} V _{IH}	- 3.5	2.25 2.75	1.5 -	Vdc
Input Current	V _{DD} = 5 V V _{in} = 1 V V _{in} = 2 V V _{in} = 5 V	rioune o	-BMIY)	2.1 2.6 2.6	6.0	μAdc
Output Drive Current (VOL = 0.5 V)	V _{DD} = 5 V	lor	2.5	6.2	-	mAdc
Output Drive Current (V _{OL} = 0.5 V)	V _{DD} = 5 V	lor	0.9	2.25	0 -11	mAdc

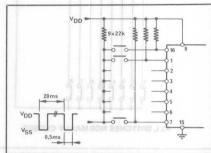
APPLICATION INFORMATION

Incorrect encoding of the selected program number can occur whenever the last bounce, on opening a normally open switch, is 40 to $60\,\mu sec.$ wide. Should the type of switch used have a characteristic within this timing, the switch configuration opposite is recommended.

By pulsing the common switch line at a rate lower than the whole bounce period (15 msec. max.), chances of misfunction are reduced.

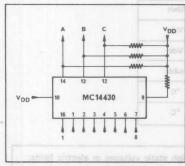
Pulsing can be provided by a unijunction transistor relaxation oscillator or by a switching transistor driven by the vertical deflection flyback signal or others. The pulse width can vary between few hundred μ sec. and few milliseconds.

FIGURE 2 - BOUNCE IMMUNE APPLICATION



3

APPLICATION INFORMATION



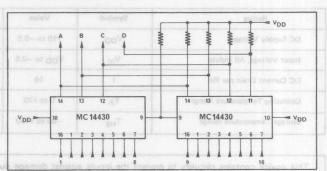
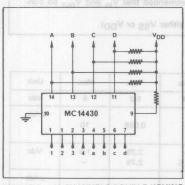


FIGURE 3 - 8 CHANNELS SINGLE KEYING

FIGURE 4 - 16 CHANNELS SINGLE KEYING



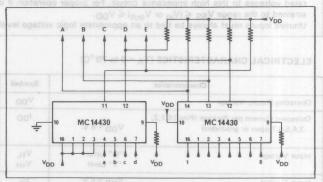
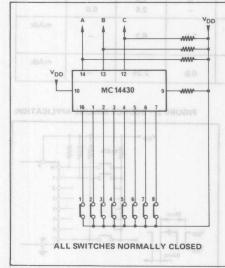


FIGURE 5 - 16 CHANNELS DOUBLE KEYING

FIGURE 6 - 32 CHANNELS DOUBLE KEYING



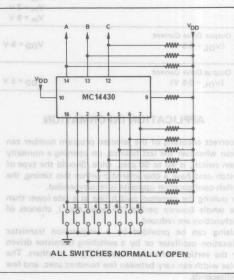


FIGURE 7 - PUSH BUTTON ELECTRICAL DIAGRAM

INPUT/OUTPUT FUNCTIONS

SINGLE/DOUBLE KEYING - Single Keying Mode (SKM) is selected by connecting pin 10 to Vnn. Double Keying Mode (DKM) is obtained by connecting pin 10 to ground.

In SKM, input pins: 16, 1, 2, 3, 4, 5, 6, 7 select programs 1 to 8 respectively. The corresponding binary coded output (000 for program 1) will appear on lines A, B, C. Output D (pin 11) is a chip select output and will remain activated (at VSS) as long as the chip is selected. Refer to application information.

In DKM, keys are divided into two groups: keys 1, 2, 3, 4 (pin 16, 1, 2, 3) and keys a, b, c, d, (pin 4, 5, 6, 7) which affect output lines A, B, and C, D respectively (see application information).

Keying sequence is important since output lines A and B are reset every time a, b, c, d are actuated.

For example: program b3 is selected by keying b first. then 3. If key d is then actuated, program d1 is selected.

POWER ON RESET - When power is switched on, channel 1 (or channel 1a in DKM) will be automatically selected.

PRIORITY ENCODER - When two or more keys belonging to the same chip are activated simultaneously, the key having the lowest number will have priority and the corresponding code will be selected.

MOTOROLA

In Double Keying Mode, key 1 has priority over keys 2,3 and 4, key a has priority over keys b, c and d.

MULTI CHIP SYSTEM - As long as one key is activated the chip select pin 9 of the corresponding chip is pulled to ground.

That chip is now selected and any other chip connected in parallel will be disabled.

If two or more keys belonging to different chips are acutated at the same time, the chip corresponding to the first actuated key will be selected. When releasing the keys, the chip corresponding to the last released key will remain selected. ggV to #2k = ytinummil scroM @

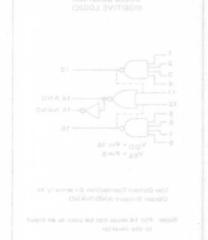
BINARY CODED OUTPUT - In SKM, binary coded program number minus one is present on lines A, B, C (pin 14, 13, 12).

Output D (pin 11) goes low when the corresponding chip is selected. In DKM the binary code output is present on lines A, B, C, D.



Ceranic Package Flavic Package Extended Operating Temperature Range Limited Operating Temperature Range	





are Line		

In Double STAD SIGNATE I has priority over keys 2,3

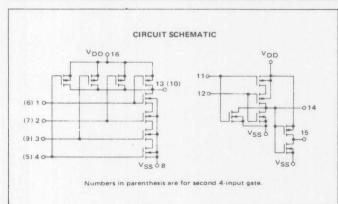
DUAL 4-INPUT "NAND" GATE
2-INPUT "NOR/OR" GATE
8-INPUT "AND/NAND" GATE

The MC14501UB constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These complementary MOS logic gates find primary use where low power dissipation and/or high noise immunity is desired. Additional characteristics can be found on the Family, Data Sheet.

- Quiescent Current = 0.5 nA/package typical @ 5 Vdc
- Noise Immunity = 45% of VDD typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
 - Single Supply Operation Positive or Negative
 - High Fanout > 50
 - Input Impedance = 10¹² ohms typical
 - Logic Swing Independent of Fanout
 - Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range

MAXIMUM RATINGS (Voltages referenced to Vss.)

Rating	Symbol	Value	Unit
DC Supply Voltage	V _{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	Vin	-0.5 to V _{DD} + 0.5	Vdc
DC Current Drain per Pin	1	10	mAdo
Operating Temperature Range - AL Device CL/CP Device	ТА	-55 to +125 -40 to +85	°C
Storage Temperature Range	T _{stg}	-65 to +150	°C



CMOS SSI

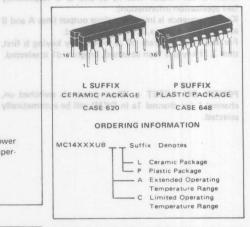
BNGLE/DOUBLE KEYING - Single Kayine Made

visited pri

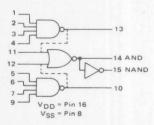
(LOW-POWER COMPLEMENTARY MOS)

TRIPLE GATE

DUAL 4-INPUT "NAND" GATE
2-INPUT "NOR/OR" GATE
8-INPUT "AND/NAND" GATE



LOGIC DIAGRAM (POSITIVE LOGIC)



Use Dotted Connection Externally to Obtain 8-Input AND/NAND

Note: Pin 14 must not be used as an input to the inverter.

ELECTRICAL CHARACTERISTICS

ifgld 1	3	VDD	Tio	w* WOL		25°C		Th	igh *	
Characteristic	Symbol	Vdc	Min	Max	Min	Тур	Max	Min	Max	Unit
Output Voltage "0" Level	V _{OL}	5.0	-	0.05	- 1	0	0.05	_1001	0.05	Vdc
V _{in} = V _{DD} or 0	OL OL	0.010	3 -	0.05		0	0.05	(Serve)	0.05	
IN DD or a		15	-	0.05	_	0	0.05	-	0,05	
"1" Level	V	5.0	4.95	-	4.95	5.0	1	4.95	-	Vdc
V _{in} = 0 or V _{DD}	VOH	10	9.95		9.95	10		9.95		
in ou abb	808	15	14.95	0	14.95	15 00	9-1	14.95	(A) 1050	
0.81 - 0.8	010	on'	14.55	10	14.00			11.00	-	Des Ducte
nput Voltage# "0" Level	VILAR	10.0	1 0	11						Vdc
(V _O = 3.6 or 1.4 Vdc)	1 800	5.0		1.5		2.25	1.5	CP Devi	1.4	
(V _O = 7.2 or 2.8 Vdc)	e ore	10	- 0	3.0	_ [6	4.50	3.0	_	2.9	
(V _O = 11.5 or 3.5 Vdc)	an	15	-	3.75		6.75	3.75		3.6	
(V _O = 1.4 or 3.6 Vdc) "1" Level	VIH	5.0	3.6		3.5	2.75		3.5		Vdc
(V _O = 2.8 or 7.2 Vdc)		10	7.1	-	7.0	5.50	+	7.0	LinkTriO	
(V _O = 3.5 or 11.5 Vdc)	+ 1 (shall	15	11.4	-	11.25	8.25	+	11.0	HUD Erlej	
Output Drive Current	ІОН						110	inugitud	Ite no Re	mAdc
(AL Device)									(goirloth	
(VOH = 2.5 Vdc) Source		5.0	-1.2	-	-1.0	1.7	1	-0.7	-	
(VOH = 4.6 Vdc)		5.0	-0.25	-	-0.2	-0.36	, -402°C to	-0.14	A 101-0 YE	
(VOH = 9.5 Vdc) NAND		10	-0.62	-	-0.5	-0.9	10°20+,s	-0.35	101 37,92	
(VOH = 13.5 Vdc)		15	-1.8	-	-1.5	-3.5	SESO-DITOW	-1.1	mas Amus	mini suel
(VOH = 2.5 Vdc) NOR		5.0	-2.1	-	-1.75	-3.0	D601 T8 143	-1.22	BE TRUOT TO	mAdc
(V _{OH} = 4.6 Vdc)		5.0	-0.42		-0.35	-0.63	101,0	-0.24	g 985_r4	
(V _{OH} = 9.5 Vdc)		10	-1.06	shbl ni h	-0.88	-1.58	go), Ci. in a	-0.62	P. Plat. print	Ti serady
(VOH = 13.5 Vdc)		15	-3.1	- D.S	-2.63	-6.12	to legions s	-1.84	000 <u>10</u> IS	
(VOH = 2.5 Vdc) NOR-		5.0	-3.6	-	-3.0	-5.1	-	-2.1	-	mAdc
(VOH = 4.6 Vdc)		5.0	-0.72	7500	-0.6	-1.08	****	-0.42	CRAR	
(VOH = 9.5 Vdc) Inverter		10	-1.8	12.0	-1.5	-2.7	STIGS**	-1.05	menny.	
(VOH = 13.5 Vdc)	fodes	e 15 e	-5.4	-	-4.5	-10.5	el tel vez popular	-3.15	-	
(VOL = 0.4 Vdc) Sink	lou	5.0	0.64		0.51	0.88		0.36	_	mAdc
(Va. = 0.5 Vdc) NAND	IOL	10	1.6	AON,	1.3	2.25	_	0.9	2011	per l'i Turqu
()/ 1 E \/d=\		15	4.2	_	3.4	8.8	201	2.4	Rightin O.3	
					0.77		975	0.54	Cottage Co.	A
(V _{OL} = 0.4 Vdc) NOR		5.0	0.92	_		1.32	201	1.36	Rejuin I.	mAdc
(V _{OL} = 0.5 Vdc)	JHT	10	2.34	AOM ,0	1.95	3.37	-		sm.	
(V _{OL} = 1.5 Vdc)	H TYPE	15	6.12	-	5.1	13.2	-	3.57	Onlan d. I	1000
(VOL = 0.4 Vdc) NOR-	11 3	5.0	1.54	-	1.28	2.2	2.5 m	0.90	D. 75 marg	mAdc
(VOL = 0.5 Vdc) Inverter		10	3.90	-	3.25	5.63	Ten da	2.27	gyen da.t	
(V _{OL} = 1.5 Vdc)	40.195	15	10.2	1871907	8.5	22	-	5.95	0.75	sielfk name
Output Drive Current 007 0.8	ІОН						12.5 ns	+ 30.65	(J.D.S. res/p	mAdc
(CL/CP Device)	0		1. 1					+ 10 (3	0.60 na/p	
(VOH = 2.5 Vdc) Source		5.0	-1.0	-	-0.8	-1.7	-m V	-0.6	olan o ald	
(V _{OH} = 4.6 Vdc)	JHTS	5.0	-0.2	1027041	-0.16	-0.36	-	-0.12	5000	
(VOH = 9.5 Vdc) NAND	1177	10	-0.5	-	-0.4	-0.9	En 2.00	-0.3	0.67 cade	
(V _{OH} = 13.5 Vdc)		15	-1.4	-	-1.2	-3.5		-1.0	N. 100 TA 4	
(VOH = 2.5 Vdc) NOR		5.0	-1.68	_	-1.4	-3.0	m 8.11	-1.05	olan #514	mAdc
(V _{OH} = 4.6 Vdc)	-	5.0	-0.34	_	-0.28	-0.63	217.50-1	-0.21	-	
(V _{OH} = 9.5 Vdc)	J4,19	10	-0.84	_	-0.7	-1.58	an 25-4 c	-0.52	at America	
(V _{OH} = 13.5 Vdc)	THAI	15	-2.52	_	-2.1	-6.12	40.00 T	-1.57	CON - 111	
(VOH = 2.5 Vdc) NOR-		5.0	-2.88	_	-2.4	-5.1	10 /E + 1	-1.8	2.01	mAdc
and the second		5.0	-0.58	_	-0.48	-1.08	W 105 7 J	-0.36	- 11 - 11s	
	,HJ9	10	-1.44		-1.2	-2.7	an 05 + 3	-0.9	(4) a 1b	
(V _{OH} = 9.5 Vdc) Inverter	THEFT	15	-4.32		-3.6	-10.5	m 26+ 10	-2.7	0.0) = 11	
(V _{OH} = 13.5 Vdc)	-		-	_			10 lb.+ 6	-	1.07.5	gt 'm fat.
(VOL = 0.4 Vdc) Sink	OL	5.0	0.52	182 10901	0.44	0.88	10 50 + J	0.36	(A) = (B)	mAdc
(VOL = 0.5 Vdc) NAND	31697	10	1.3	-	1.1	2.25	in TE+ 30	0.9	(i,0) = jp	
(V _{OL} = 1.5 Vdc)		15	3.6	-	3.0	8.8	an (5. 4.)	2.4	10) F 10	St. 12.102
(VOL = 0.4 Vdc) NOR		5.0	0.79	-	0.66	1.32	he typical	0.54	revorton	mAdc
$(V_{OL} = 0.5 \text{ Vdc})$		10	1.98	- "	1.65	3.37	-	1.36	-	
(V _{OL} = 1.5 Vdc)		15	5.4	-	4.5	13.2	-	3.57	-	
(VOL = 0.4 Vdc) NOR-		5.0	1.32	-	1,1	2.2	-	0.90	- 1	mAdc
(VOL = 0.5 Vdc) Inverter	nigh stat	100	3.3	suieme i	2.75	5.63	cuitry to	2.27	ica con	
(VOL = 1.5 Vdc)	ne to no	1801508	9.0	nexts)	7.5	22.0	mor_terft	5.95	1 1 1 1 1	

constrained to the range VSS \ll (V_{in} or V_{out}) \ll Vpp. Unused inputs must siways be ried to an appropriate logic voltage level (e.g. either VSS or Vpp).

(VOH = 2.5 Vdd) NOR

ELECTRICAL CHARACTERISTICS (Continued)

Think*	003	VDD	T _{low} *			25°C		Thigh*		
Characteristic	Symbol	Vdc	Min	Max	Min	Тур	Max	Min	Max	Unit
Input Current (AL Device)	lin	15	- 20	±0.1	-	±0.00001	±0.1	17/30	±1.0	μAdc
Input Current (CL/CP Device)	o lin o	15	- 80	0±0.3	-	±0.00001	± 0.3	-	±1.0	μAdc
Input Capacitance (V _{in} = 0)	Cin	. 89.	_ 80	96	1	5.0 B HO	7.5	to fin	-	pF
Quiescent Current (AL Device) (Per Package)	IDD	5.0 10 15	at	0.25 0.50 1.00	1	0.0005 0.0010 0.0015	0.25 0.50 1.00		7.5 15.0 30.0	μAdc
Quiescent Current (CL/CP Device) (Per Package)	I DDOS	5.0 10 15	- 0 - 81	1.0 2.0 4.0	-	0.0005 0.0010 0.0015	1.0 2.0 4.0	- to	7.5 15.0 30.0	μAdc
Total Supply Current * * † (Dynamic plus Quiescent, Per Package) (C _L = 50 pF on all outputs, all buffers switching)	50 Ti	5.0 10 15	1	- 7	IT =	(1.2 μA/kHz) (2.4 μA/kHz) (3.6 μA/kHz)	f + IDD			μAdc

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device. Thigh = +125°C for AL Device, +85°C for CL/CP Device. #Noise immunity specified for worst-case input combination.

†To calculate total supply current at loads other than 50 pF: $I_T(C_L) = I_T(50 \text{ pF}) + 4 \times 10^{-3} (C_L - 50) \text{ V}_{DD}f$

where: I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

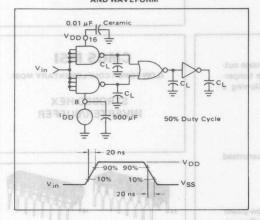
SWITCHING CHARACTERISTICS** (CL = 50 pF, TA = 25°C)

Characteristic	-10.5	4,5	-	A.8 Figure	15	Symbol	VDD	Typ All Types	V Max	Unit
Output Rise Time t _{TLH} = (3.0 ns/pF) C _L + 30 ns	2,25	NAND	, NOR	2,3	10	^t TLH	5.0	180	360 180	ns
t _{TLH} = (1.5 ns/pF) C _L + 15 ns t _{TLH} = (1.1 ns/pF) C _L + 10 ns				0.92			15	65	130	iovi
Output Fall Time t_H = (1.5 ns/pF) C ₁ + 25 ns	13.2	NAND	, NOR	2,3	15	[‡] THL	5.0	100	200	ns
t _{THL} = (0.75 ns/pF) C _L + 12.5 ns t _{THL} = (0.55 ns/pF) C _L + 9.5 ns				1.54 3,90	5,0		10		100	10VI
Output Rise Time	20	NOR-II	nverter	3	67	tTLH		19	OV C.T -	ns
t _{TLH} = (1.35 ns/pF) C _L + 32.5 ns t _{TLH} = (0.60 ns/pF) C _L + 20 ns t _{TLH} = (0.40 ns/pF) C _L + 17 ns	5.1-			0.1-	5.0	HOI	5.0 10 15	100 50 40	200 100 80	(CL/C)
Output Fall Time t _{THL} = (0.67 ns/pF) C _L + 26.5 ns t _{THL} = (0.45 ns/pF) C _L + 17.5 ns t _{THL} = (0.37 ns/pF) C _L + 11.5 ns	0.0- 0.0- 0.0-	NOR-I	nverter	80.1-	10 15 5.0	†THL	5.0 10 15	60 40 30	120 80 60	IO ns IOV)
Propagation Delay Time tp_H, tpHL = (1.7 ns/pF) CL + 45 ns tp_H, tpHL = (0.66 ns/pF) CL + 37 ns tp_H, tpHL = (0.5 ns/pF) CL + 25 ns	-0.63 -1.58 -8.12 -5.1	NAND		96.0 2 48.0 - 92.5 -	9.0 10 15 5.0	tPLH, tPHL	50 10 15	130 70 50	260 140 100	HOVI HOVI
tpLH, tpHL = (1.7 ns/pF) C _L + 30 ns tpLH, tpHL = (0.66 ns/pF) C _L + 32 ns tpLH, tpHL = (0.5 ns/pF) C _L + 20 ns	-1.08 -2.7 -10.6	NOR		58.0-3 55.1- 58.4-	0.0 01 01	tPLH, tPHL	5.0 10 15	115 65 45	230 130 90	IO ns
tpLH, tpHL = (1.7 ns/pF) CL + 45 ns tpLH, tpHL = (0.66 ns/pF) CL + 37 ns tpLH, tpHL = (0.5 ns/pF) CL + 25 ns	0.88 2.26 8.8	NOR-I	nverter	\$8.0 3	6.0 10 16	tPLH, tPHL	5.0 10 15	130 70 50	260 140 100	o ns IOV)

* * The formulae given are for the typical characteristics only.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields: however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g. either V_{SS} or V_{DD}).

FIGURE 1 - POWER DISSIPATION TEST CIRCUIT AND WAVEFORM



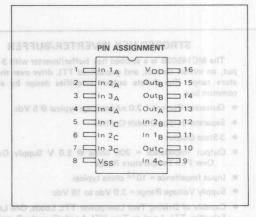


FIGURE 2 - 4-INPUT "NAND" GATE SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

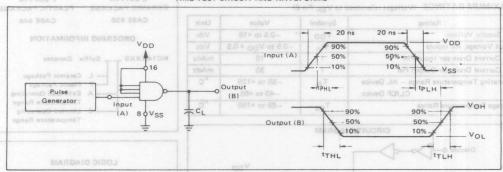
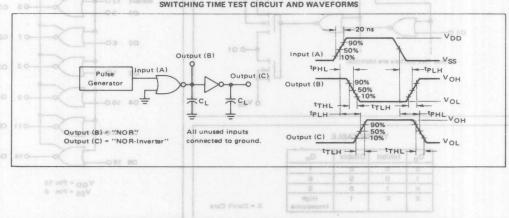


FIGURE 3 - "NOR" GATE and "NOR-INVERTER" SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



MC14502B

PATION TEST CIRCUIT

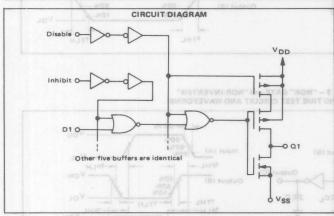
STROBED HEX INVERTER/BUFFER

The MC14502B is a strobed hex buffer/inverter with 3-state output, an inhibit control, and guaranteed TTL drive over the temperature range. The 3-state output simplifies design by allowing a common bus.

- Quiescent Current = 2.0 nA/package typical @ 5 Vdc
- Separate Output Disable Control
- 3-State Output
- Output Impedance = 200 ohms @ 5.0 V Supply Guaranteed Over Full Temperature Range
- Input Impedance = 10¹² ohms typical
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range.

MAXIMUM RATINGS (Voltages referenced to VSS, Pin 8)

Rating	Symbol	Value	Unit
DC Supply Voltage	V _{DD}	0.5 to +18	Vdc
Input Voltage, All Inputs	Vin	-0.5 to V _{DD} + 0.5	Vdc
DC Current Drain per Input Pin	360G LgC	10	mAdc
DC Current Drain per Output Pin	and I have	30	mAdo
Operating Temperature Range — AL Device CL/CP Device	TA	-55 to +125 -40 to +85	°C
Storage Temperature Range	T _{stg}	-65 to +150	°C

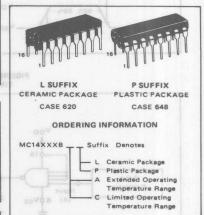


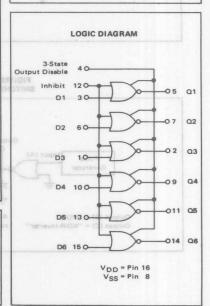
	TRU	TH TABL	E 10) tugiuc
Dn	Inhibit	Disable	Qn
0	0	0	1
1	0	0	0
X	1	0	0
×	х	1	High Impedance

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

STROBED HEX INVERTER/BUFFER





3

X = Don't Care

ELECTRICAL CHARACTERISTICS

Alt Tyges Louis	Manage	VDD	Tic	w"		25°C	and the same	Thi	gh *	
Characteristic	Symbol	Vdc	Min	Max	Min	Тур	Max	Min	Max	Unit
Output Voltage "O" Level	VOL	5.0	-	0.05	-	0 .	. 0.05	-	0.05	Vdc
Vin VDD or 0	6:0	10	-	0.05	-	0	0.05	IDFILCL +	0.05	TY2
001 00 -	0.7	15	-	0.05	-	0	0.05	1,04990	0.05	177
OB OA "1" Level	VOH	5.0	4.95	_	4.95	5.0	10 0	4.95	in E.E. = 1	Vdc
V _{in} = 0 or V _{DD}	On	10	9.95	_	9.95	10	_	9.95	emi Z lb 3	sugguO
08 08 -	5.0	15	14.95	_	14.95	15	se 01	14.95	in 8.9) =	1177
Input Voltage# "0" Level	VIL						bit 0.8	- 13 (Figh	en 6.01 -	Vdc
(V _O = 4.5 or 0.5 Vdc)	15	5.0	_	1.5	_	2.25	1.5	10 Bala	1.5	HTI
(V _O = 9.0 or 1.0 Vdc)	5.0	10	-	3.0	_	4.50	3.0	eO moit	3.0	000004
(V _O = 13.5 or 1.5 Vdc)	01	15	_	4.0	_	6.75	4.0	-	4.0	
09 "1" Level	VIH									
(V _O = 0.5 or 4.5 Vdc)	0.8	5.0	3.5	-	3.5	2.75	O or ridi	3.5		Vdc
(V _O = 1.0 or 9.0 Vdc)		10	7.0		7.0	5.50	- 00 1000	7.0	Amari Lidio	1
(V _O = 1.5 or 13.5 Vdc)	ar	15	11.0	_	11.0	8.25	_	11.0		13.0
Output Drive Current (AL Device)	ТОН	-	11.0		11.0	-	1 /2			mAdc
(V _{OH} = 2.5 Vdc) Source	ОН	5.0	-3.0	_	-2.4	-4.2	o to O, In	-1.7	tion Diney	1111111
(V _{OH} = 4.6 Vdc)	15	5.0	-0.64	_	-0.51	-0.88	_	-0.36	_	
07 051111		10	-1.6		-1.3	-2.25	to thorns	-0.9		
	0.8	15	-4.2	_	-3.4	-8.8	L., andang	-2.4	ad agrigor	3-6000
	The contract of	5.0	3.5		2.8	6.6	_	2.0		mAdc
	IOL	10	7.8	_	6.3	17		4.4		
		15	29		24	66	Hgn Tinge	16	aldegaqon'	3-State!
(V _{OL} = 1.5 Vdc)	0.5	15	23	-	24	00	-	10	-	1
Output Drive Current (CL/CP Device)	ІОН		0.5							mAdc
(V _{OH} = 2.5 Vdc) Source		5.0	-2.5	-	-2.1	-4.2	Custons	-1.7	Propages	3-5100
(V _{OH} = 4.6 Vdc)		50	-0.52	-	-0.44	-0.88	-	-0.36		
(V _{OH} = 9.5 Vdc)		10	-1.3	-	-1.1	-2.25		-0.9		
(V _{OH} = 13.5 Vdc)	0.2	15	-3.6		-3.0	-8.8	agent stall	-2.4	1	Interest II
(VOL = 0.4 Vdc) Sink	OL	5.0	2.3		1.9	6.6	-	1.6	-	mAdc
(V _{OL} = 0.5 Vdc)		10	5.0	-	4.2	17	-	3.4	-	
(V _{OL} = 1.5 Vdc)		15	19	-	16	66	-	13	-	
Input Current (AL Device)	lin	15	-	± 0.1	10 53001	±0.00001	±0.1	101 930 1	± 1.0	μAdc
Input Current (CL/CP Device)	lin	15	-	± 0.3	-	±0.00001	± 0.3	- 1	± 1.0	μAdc
Input Capacitance	Cin	-	-	_	-	5.0	7.5	-	_	pF
(V _{in} = 0)	-111					0.0				
Quiescent Current (AL Device)	Inn	5.0		1.0		0.002	1.0		30	μAdc
(Per Package)	IDD	10	inst darm	2.0	mi ent in	0.002	2.0	entaine	60	MAGC
any voltage higher tran maxi-		15	ovs of ni	4.0	noitusa	0.006	4.0	e adyise	120	everi
0 (01 108 5	oour six		2 100010		tic sonz		College College	autorito		Tiuria .
Quiescent Current (CL/CP Device) (Per Package)	IDD	5.0	-	4.0 8.0	tuoV 10	0.002	4.0	in self of	30	μAdc
AggV 10 22V 18rts		10	ov pipoi	16	ggs_ns	0.004	8.0	181401 83	60	Unu
	-	-	- 18-	10					120	-
Total Supply Current**†	-IT	5.0	-		IT = (2	2.7 µA/kHz	f + IDD			μAdc
(Dynamic plus Quiescent,		10	0 - 1		T = (5	i.3 μA/kHz	I + IDD			
Per Package)		15	L. TOWN		T = (8	3.0 μA/kHz) f + IDD			
(C _L = 50 pF on all outputs, all										1971
buffers switching)	CURE 2	8			539	UNA YEART	NO LANG	BUT FO	an inch	
Three-State Leakage Current	TL	15	-	± 0.1	-	±0.00001	± 0.1	THEMS	±3.0	μAdc
(AL Device)										
Three-State Leakage Current	ITL	15	-	±1.0	-	+0.00001	±1.0	-	± 7.5	μAdc
(CL/CP Device)										

^{*}Tlow = -55°C for AL Device, -40°C for CL/CP Device.

tTo calculate total supply current at loads other than 50 pF: $I_{\mathsf{T}}(\mathsf{CL}) = I_{\mathsf{T}}(\mathsf{50 pF}) + 6 \times 10^{-3} \, (\mathsf{CL} - \mathsf{50}) \, \mathsf{V_{DD}} \mathsf{f}$ where: I_{T} is in $\mu\mathsf{A}$ (per package), CL in pF, $\mathsf{V_{DD}}$ in Vdc, and f in kHz is input frequency.

**The formulas given are for the typical characteristics only at 25°C.



Thigh = +125°C for AL Device, +85°C for CL/CP Device. #Noise immunity specified for worst-case input combination.

ELECTRICAL CHARACTERISTICS

right C		practarietic				Cumbal	Von	All Types			Unit
	Chara	Cteristic				Symbol	ADD	Min	Тур	Max	Onit
	0.05	. 0	-	0.05		tTLH	Jov	Laval	0"	Voltage	ns
3.0 ns/pF) CL +	30 ns					01	5.0	-	100	200	niV.
1.5 ns/pF) CL +	15 ns					et l	10	-	50	100	
1.1 ns/pF) CL +	10 ns					0.8	15	lava_1	40	80	
Time 88.8		01	8.85		9.98	tTHL				00 V 10 0 -	ns
0.6 ns/pF) CL +	10 ns					81	5.0	-	40	80	
0.3 ns/pF) CL +	5.0 ns						10	eve s "O"	20	40	V ruga
0.27 ns/pF) CL	+ 1.5 ns					8.0	15	-	15	30	nVI
Delay Time Dat	ta to Q	4,68	- 1	0.6	1 - 1	TPHL	5.0	-	135	270	ns
						er	10	-	55	110	OW)
							15	ove#"1"	40	80	
Delay Time, Inl	nibit to Q	2.75	3.6		3.5	tpHI	5.0	-	335	670	ns
						01	10.	-	145	290	DV)
						15	15	-	95	190	DV)
Delay Time Dat	ta to Q, Ini	hibit to Q				tpl H	5.0	_(90	295	590	ns
						0.8	10	_801	130	260	DV?
						0.8	15	-	95	190	OVE
agation Delay,	Output "1"	" to High I	mpedance		6.1 -	tpH7	5.0	-	65	130	ns
						ar	10	-	30	60	DV3
						0.8	15	- 1	25	50	(V/O
agation Delay,	High Impe	dance to "	1" Level		877	tpzH	5.0	-	260	520	ns
						ar I	10	-	105	210	(ACI
							H 15	(ea/vat	80	160	/ usprud
pagation Delay,	Output "(" to High	Impedanc	6	-2.5	tpL7	5.0	_631	150	300	ns
-0.36	-	88.0-	-0.44			0.8	10	-	70	140	(DA)
						10	15	-	55	110	(PA)
agation Delay,	High Impe	dance to "	O" Level		0.6-	tpzi	5.0	-	160	320	ns
- 8.1	-	8.6	1.9			0.8	10	- 1	65	130	(DV)
						. 01	15	-	50	100	(Volt
	Time 3.0 ns/pF) CL + 1.5 ns/pF) CL + 1.5 ns/pF) CL + Time 0.6 ns/pF) CL + 0.3 ns/pF) CL + 0.27 ns/pF) CL - Delay Time Data	Time 3.0 ns/pF) C _L + 30 ns 1.5 ns/pF) C _L + 15 ns 1.1 ns/pF) C _L + 10 ns Time 0.6 ns/pF) C _L + 10 ns 0.3 ns/pF) C _L + 5.0 ns 0.27 ns/pF) C _L + 5.0 ns 0.27 ns/pF) C _L + 1.5 ns Delay Time Data to Q Delay Time Data to Q Delay Time Data to Q, Initiagation Delay, Output "1" Degation Delay, High Imperpagation Delay, Output "(1) Degation Delay, Output "(1) Degation Delay, Output "(1) Degation Delay, High Imperpagation Delay, Hi	Time 3.0 ns/pF) C _L + 30 ns 1.5 ns/pF) C _L + 15 ns 1.1 ns/pF) C _L + 10 ns Time 0.6 ns/pF) C _L + 10 ns 0.3 ns/pF) C _L + 10 ns 0.2 ns/pF) C _L + 15 ns Delay Time Data to Q Delay Time Data to Q Delay Time Data to Q, Inhibit to Q agation Delay, Output "1" to High Inpagation Delay, High Impedance to " pagation Delay, Output "0" to High Inpagation Delay, Output "0" to High Inpagation Delay, High Impedance to "	Time 3.0 ns/pF) C _L + 30 ns 1.5 ns/pF) C _L + 15 ns 1.1 ns/pF) C _L + 10 ns Time 0.3 ns/pF) C _L + 10 ns 0.3 ns/pF) C _L + 5.0 ns 0.27 ns/pF) C _L + 1.5 ns Delay Time Data to Q Delay Time Data to Q Delay Time Data to Q, Inhibit to Q agastion Delay, Output "1" to High Impedance agastion Delay, High Impedance to "1" Level pagation Delay, Output "0" to High Impedance	Time 3.0 ns/pF) C _L + 30 ns 1.5 ns/pF) C _L + 15 ns 1.1 ns/pF) C _L + 10 ns Time 0.3 ns/pF) C _L + 10 ns 0.3 ns/pF) C _L + 5.0 ns 0.27 ns/pF) C _L + 1.5 ns Delay Time Data to Q Delay Time Data to Q Delay Time Data to Q, Inhibit to Q agation Delay, Output "1" to High Impedance agation Delay, High Impedance to "1" Level	Time 3.0 ns/pF) C _L + 30 ns 1.5 ns/pF) C _L + 15 ns 1.1 ns/pF) C _L + 10 ns Time 0.3 ns/pF) C _L + 10 ns 0.3 ns/pF) C _L + 5.0 ns 0.27 ns/pF) C _L + 1.5 ns Delay Time Data to Q Delay Time Data to Q Delay Time Data to Q, Inhibit to Q agastion Delay, Output "1" to High Impedance agastion Delay, High Impedance to "1" Level pagation Delay, Output "0" to High Impedance	Time 3.0 ns/pF) C _L + 30 ns 1.5 ns/pF) C _L + 15 ns 1.1 ns/pF) C _L + 10 ns Time 0.3 ns/pF) C _L + 10 ns Time 0.3 ns/pF) C _L + 10 ns 0.3 ns/pF) C _L + 5.0 ns 0.27 ns/pF) C _L + 1.5 ns Delay Time Data to Q tpHL Delay Time, Inhibit to Q tpHL Delay Time Data to Q, Inhibit to Q tpHL agation Delay, Output "1" to High Impedance tpHZ agation Delay, High Impedance to "1" Level tpZH pagation Delay, Output "0" to High Impedance tpLZ	Time 3.0 ns/pF) C _L + 30 ns 1.5 ns/pF) C _L + 15 ns 1.1 ns/pF) C _L + 10 ns 1.5 ns/pF) C _L + 10 ns 1.6 ns/pF) C _L + 10 ns 1.7 me 1.7 me 1.8 ms/pF) C _L + 10 ns 1.9 ms/pF) C _L + 1.5 ns 1.0 ms/	Time 3.0 ns/pF) C _L + 30 ns 1.5 ns/pF) C _L + 15 ns 1.1 ns/pF) C _L + 10 ns 1.1 ns/pF) C _L + 10 ns 1.2 ns/pF) C _L + 10 ns 1.3 ns/pF) C _L + 10 ns 1.4 ns/pF) C _L + 1.5 ns 1.5 ns/pF) C _L + 1.5 ns 1.6 ns/pF) C _L + 1.5 ns 1.7 ns/pF) C _L + 1.5 ns 1.8 ns/pF) C _L + 1.5 ns 1.9 ns/pF) C _L + 1.5 ns 1.9 ns/pF) C _L + 1.5 ns 1.9 ns/pF) C _L + 1.5 ns 1.0 ns/pF) C _L + 1.5	Characteristic Symbol VDD Min Typ	Time

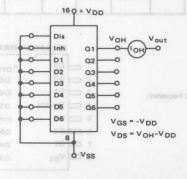
*The formulae given are for the typical characteristics only.

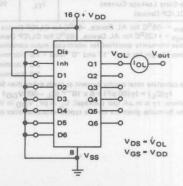
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields: however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leqslant (V_{in} \text{ or } V_{out}) \leqslant V_{DD}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g. either V_{SS} or V_{DD}).

FIGURE 1 - TYPICAL OUTPUT SOURCE CURRENT TEST CIRCUIT (IOH)

T = (6.3 µA/kHz) + + (DD

FIGURE 2 - TYPICAL OUTPUT SINK CURRENT TEST CIRCUIT (IOL)





3

FIGURE 3 - POWER DISSIPATION TEST CIRCUIT
AND WAVEFORM

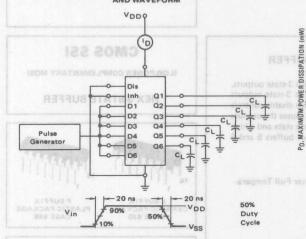


FIGURE 4 - AMBIENT TEMPERATURE

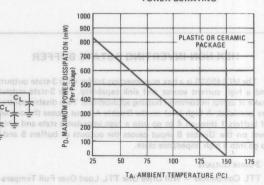


FIGURE 5 — AC TEST CIRCUIT AND WAVEFORMS
(tTLH, tTHL, tpHL, and tpLH)

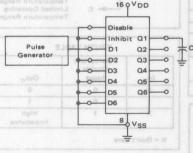
FIGURE 6 - 3-STATE AC TEST CIRCUIT AND WAVEFORMS (tpHz, tpLz, tpzH, tpzL)

16 Q VDD

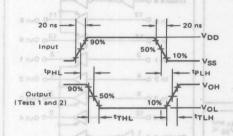
Supply Voltage Range = 3.0 Vdc to 18 Vdc

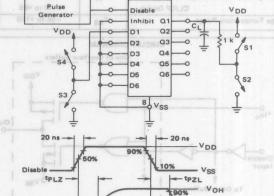
Switch Positions for 3-State Test

			TEST	S1	S2	53	S4
QVDD		out	tPHZ	Open	Closed	Closed	Open
			tPLZ	Closed	Open	Open	Closed
ble			tPZL tPZH	Closed	Open	Open	Closed
bit Q1	mAde		"PZH	Open	Closed	Closed	Open



For all tTLH, tTHL, tpHL, and tpLH measurements V $_{\rm in}$ may be applied to any other $\rm D_n$ input or to Inhibit.





3-229

MC14503B

ATION TEST CIRCUIT

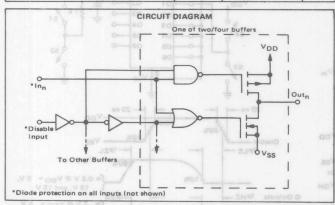
HEX NON-INVERTING 3-STATE BUFFER

The MC14503B is a hex non-inverting buffer with 3-state outputs, and a high current source and sink capability. The 3-state outputs make it useful in common bussing applications. Two disable controls are provided. A high level on the Disable A input causes the outputs of buffers 1 through 4 to go into a high impedance state and a high level on the Disable B input causes the outputs of buffers 5 and 6 to go into a high impedance state.

- 3-State Outputs
- TTL Compatible Will Drive One TTL Load Over Full Temperature Range
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Symmetrical Turn-On and Turn-off Delays
- Symmetrical Output Rise and Fall Times
- Two Disable Controls for Added Versatility
- Pin for Pin Replacement for MM80C97 and 340097

MAXIMUM RATINGS (Voltages referenced to VSS, Pin 8)

Rating best best	Symbol	Value Value	Unit
DC Supply Voltage	VDD	-0.5 to +18	Vdc
Input Voltage, All Inputs	Vin	-0.5 to V _{DD} + 0.5	Vdc
DC Current Drain per Input Pin		10	mAdc
DC Current Drain per Output Pin	1	25	mAdc
Operating Temperature Range — AL Device CL/CP Device	TA	-55 to +125 -40 to +85	°C
Storage Temperature Range	T _{stg}	-65 to +150	°C



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper

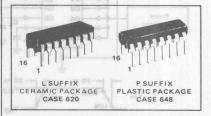
operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in} \text{ or } V_{out}) \le V_{DD}$.

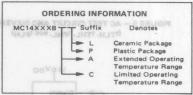
Unused inputs must always be tied on an appropriate logic voltage level (e.g., either VSS or VDD).

CMOS SSI

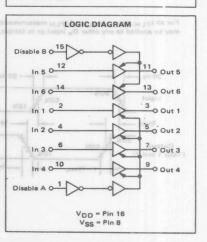
(LOW-POWER COMPLEMENTARY MOS)

HEX 3-STATE BUFFER





Inn	Appropriate Disable Input	Outn
0.0	20 0	0
1	80-0-0	1
×	2 1	High Impedance



ELECTRICAL CHARACTERISTICS

	AB Ty	VDD	Tic	w w		25°C		Thi	-	
Characteristic	Symbol	Vdc	Min	Max	Min	Тур	Max	Min	Max	Unit
Output Voltage "0" Level	VOL	5.0	-	0.05	11	0	0.05	-	0.05	Vdc
Vin = VDD or 0	45	10	-	0.05	-	0	0.05	H C + 20	0.05	- HJT
	1	15		0.05	-	0	0.05		0.05	- 12 199
"1" Level	VOH	5.0	4.95	_	4.95	5.0	-	4.95		Vdc
Vin = 0 or VDD	I On	10	9.95		9.95	10	20	9.95	Idien S.U.	= 147.15
807		15	14.95	- 48	14.95	15		14.95	Time	la 3 Indin
	1 2 1	, 15	14.55	-	14.00	15	-	14.55	man 3.0)	Vdc
	Level VIL	1				0.05	201	18 4 JO 13	(0,3 ns/g	- Vac
(V _O = 3.6 or 1.4 Vdc)	18	5.0	-	1.5		2.25	1.5	8+ 70 (4	1.5	- SHITT
(V _O = 7.2 or 2.8 Vdc) (V _O = 11.5 or 3.5 Vdc)		10	-	3.0	191	4.50	3.0	pore O Ha	3.0	G 190-mic
(*U = 11.5 or 3.5 vac/	Level	15	a - 1	3.75	-	6.75	3.75	00 5 0 1	3.75	Canada.
(VO = 1.4 or 3.6 Vdc)	VIH	5.0	3.5	-	3.5	2.75	871	3.5	Azn 81.0	Vdc
(V _O = 2.8 or 7.2 Vdc)	20	10	7.0	-	7.0	5.5	-	7.0	iglen 1.0	= H_191
(VO = 3.5 or 11.5 Vdc)	100	15	11.25	-	11.25	8.25	- 61	11.25	indices 1 'm	= H7ld1
Output Drive Current (AL Device)*	** Іон		-					a special	gerned, good	mAdc
(VOH = 2.5 Vdc) Source	1000	4.5	-4.3		-3.6	-5.0	- 81	-2.5	Righan E.C	- JHaj
(V _{OH} = 2.5 Vdc)	35	5.0	-5.8	_	-4.80	-6.1	8/5	-3.0	17.5 osfs	11197
	25		1		-1.02	-1.4	. 32	-0.7	Fig\un E.O	" JHR!
(V _{OH} = 4.6 Vdc)	76	5.0	-1.2		1.453		-	deni Torolad	noitegeo	State Pri
(VOH = 9.5 Vdc)	0.0	10	-3.1		-2.60	-3.7	506	-1.8	H or "I"	Cutpur
(V _{OH} = 13.5 Vdc)	36	15	-8.2	-	-6.80	-14.1	-	-4.8	-	
Sink	OL			1	141		996	sheaml ris	H oz "6"	mAdc
(VOL = 0.4 Vdc)	0.6	4.5	2.2	-	1.8	2.1	-	1.2	-	
(VOL = 0.4 Vdc)	36	5.0	2.6	-	2.1	2.3	-	1.3	-	
(VOL = 0.5 Vdc)	80	10	6.5	- 10	5.5	6.2	- 10	3.8	padenos	Hilgh In
(VOL = 1.5 Vdc)	25	15	19.2	_	16.10	25.00	_	11.2	_	
Output Drive Current (CL/CP Device	10н						-			mAdc
(V _{OH} = 2.5 Vdc) Source	OH	4.75	-4.0		-3.60	-5.5	1 10	-2.4	sonabaq	High In
The state of the s	35					-6.1		-3.0		
(V _{OH} = 2.5 Vdc)	28	5.0	-4.6		-4.20	1		-0.7		
(V _{OH} = 4.6 Vdc)	4	5.0	-1.0		-0.88	-1.4	-			
(V _{OH} = 9.5 Vdc)		10	-2.4	-	-2.20	-3.7	oto leoigi	-1.8	is gi y en a	se formula
(V _{OH} = 13.5 Vdc)		15	-6.6		-6.00	-14.1	-	-4.8	-	
Sink	IOT.									mAdc
(V _{OL} = 0.4 Vdc)		4.75	2.1	-	1.95	2.2	-	1.25	-	
(VOL = 0.4 Vdc)		5.0	2.3	-	2.10	2.3	-	1.3	-	
(V _{OL} = 0.5 Vdc)		10	6.0	_	5.45	6.2	_	3.8	_	
(V _{OL} = 1.5 Vdc)		15	15.2	-0	13.80	25.00	20-24	11.2	100.0-	anners
Input Current (AL Device)	lin	15	-	± 0.1	-	±0.00001	±0.1	-	±1.0	μAdc
Input Current (CL/CP Device)	lin	15	-	± 0.3		±0.00001	±0.3		±1.0	μAdc
Input Capacitance (V _{in} = 0)		-	-	±0.3		5.0	7.5		21.0	pF
Quiescent Current (AL Device)	Cin						1.0		-	1200
	اما	5.0	-	1.0	-	0.002			30	μAdc
(Per Package)		10	-	2.0	-	0.004	2.0	- L	60	USS 5
		15	-	4.0	-	0.006	4.0	1-0	120	
Quiescent Current (CL/CP Device)	IDD	5.0	-	4.0	-	0.002	4.0	19-1	30	μAdc
(Per Package)		10	-	8.0	3000	0.004	8.0	3317	60	1
7 Cours Ind 10		15	-	16		0.006	16	-	120	
Total Supply Current **†	I _T	5.0							-	μAdc
(Dynamic plus Quiescent, Per Paci		10				$= (2.5 \mu A/k)$				BOX
(C _L = 50 pF on all outputs)	-0-1	15			IT	$= (6.0 \mu A/k)$	Hz) f +	IDD		1
	(ala)	15			IT	$= (10 \mu A/k)$	+z)f+1	DD		In
All outputs switching, 50% Duty Cy			-	201	631	201	1901	P 11	100	32
3-State Output Leakage Current	1TL	15	-	±0.1	-	±0.0001	±0.1	TA. ARRE	±3.0	μAdc
(AL Device)			-		-			-		
3-State Output Leakage Current	ITL	15	-	±1.0	-	±0.0001	±1.0	-	± 7.5	μAdc
(CL/CP Device)										1

^{*}Tlow = -55°C for AL Device, -40°C for CL/CP Device.

Thigh = +125°C for AL Device, +85°C for CL/CP Device.

**Thigh = +125°C for AL Device, +85°C for CL/CP Device.

**Noise immunity specified for worst-case input combination.

†*To calculate total supply current at loads other than 50 pF;

IT(CL) = IT(50 pF) +6 × 10-3 (CL - 50) VDD f

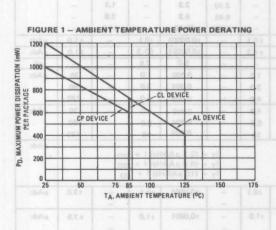
IT is in µA (per package) CL in pF, VDD in Vdc, and f in kHz is input frequency.

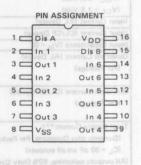
**The formulas given are for the typical characteristics only at 25°C

***Care must be taken not to exceed maximum current ratings (see maximum ratings table and Figure 1).

deid	2500	W	VDD	All T	ypes	
Characteristic		Symbol	Vcc	Тур	Max	Unit
Output Rise Time \$\text{TLH} = (0.5' \text{ ns/pF}) C_L + 20 \text{ ns} \$\text{TLH} = (0.3 \text{ ns/pF}) C_L + 8.0 \text{ ns} \$\text{TLH} = \text{ \left(0.2 \text{ ns/pF}) C_L + 8.0 \text{ ns}}	0 0	**************************************	5.0 TI	45 23 18	90 45 35	ns rough
Output Fall Time \$\text{THL} = (0.5 \text{ ns} \text{PF}) C_{\text{L}} + 20 \text{ ns} \$\text{THL} = (0.3 \text{ ns} \text{PF}) C_{\text{L}} + 8.0 \text{ ns} \$\text{THL} = (0.2 \text{ ns} \text{PF}) C_{\text{L}} + 8.0 \text{ ns}	15 2.28	au thi	5.0 10 15	45 23 18	90 45 35	ns the spatial value of the s
Turn-Off Delay Time, all Outputs tp_H = (0.3 ns/pF) CL + 60 ns tp_H = (0.15 ns/pF) CL + 27 ns tp_H = (0.1 ns/pF) CL + 20 ns	8.75 2.75 6.6	A,S O,V	5.0 10 0.7 15	75 35 25	150 70	(V _O = 2/3 or 3,8 (V _O = 2,8 or 7,2
Turn-On Delay Time, all Outputs tpHL = (0.3 ns/pF) CL + 60 ns tpHL = (0.15 ns/pF) CL + 27 ns tpHL = (0.1 ns/pF) CL + 20 ns	-5.0 -6.1	tpHL 8.5- 88.5-	5.0 10 15	75 35 25	150 70 50	ns unput Drina Curre (VOH = 2.6 Vda) (VOH = 2.6 Vda)
3-State Propagation Delay Time Output "1" to High Impedance	7.6-	tPHZ	5.0 10 15	75 40 35	150 80 70	NON = 13.5 vdc
Output "0" to High Impedance		tPLZ	5.0 10 15	80 40 35	160 80 70	ns (56V 5.0 = 10V) (56V 5.0 = 10V)
High Impedance to "1" Level		tPZH	5.0 st 10 st 15	65 25. 20	130 50 40	(V _{QL} = 1.6 Vdc)
High Impedance to "0" Level		OS.A-	5.0 10 15	100 35 25	200 70 50	(V _{OH} = 2.5 Vdc)

*The formulas given are for the typical characteristics only.







MC14503B

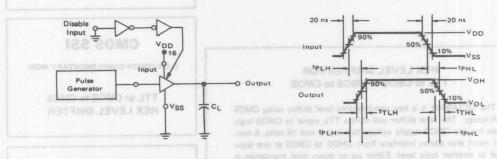
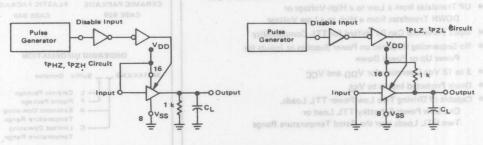
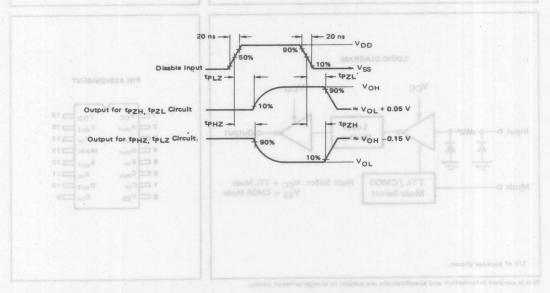


FIGURE 3 – 3 STATE AC TEST CIRCUITS AND WAVEFORMS
(tplz, tphz, tpzh, tpzh)

The VCC level sets the input signal levels while VOD salects the





MC14504B

HEX LEVEL SHIFTER FOR TTL to CMOS or CMOS to CMOS

WITCHING TIME TEST CIRCUIT AND WAVEFORMS

The MC14504B is a hex non-inverting level shifter using CMOS technology. The level shifter will shift a TTL signal to CMOS logic levels for any CMOS supply voltage between 5 and 15 volts. A control input also allows interface from CMOS to CMOS at one logic level to another logic level: Either up or down level translating is accomplished by selection of power supply levels VDD and VCC. The VCC level sets the input signal levels while VDD selects the output voltage levels.

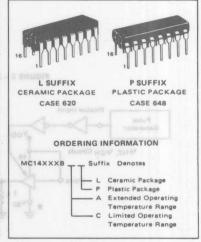
Supply current is typically 1 nA @ VDD = 10 V for CMOS to CMOS operation. When translating from TTL to CMOS supply current is typically 2.5 mA taken from VCC.

- UP Translates from a Low to a High Voltage.or DOWN Translates from a High to a Low Voltage
- Input Threshold Can Be Shifted for TTL Compatibility
- No Sequencing Required on Power Supplies or Inputs for Power Up or Power Down
- 3 to 18 Vdc Operation for VDD and VCC
- Diode Protected Inputs to VSS
- Capable of Driving Two Low Power TTL Loads, One Low Power Schottky TTL Load or Two HTL Loads over the Rated Temperature Range

CMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

TTL or CMOS to CMOS HEX LEVEL SHIFTER



PIN ASSIGNMENT

Vcc

Ain

4 Bout

2 = Aout

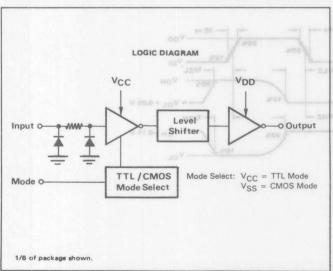
3 [

VDD 16

-14

Fout ____ 15

ocF_{in} Mode 13



Bin Eout 12 5 0 6 Cout Ein | 11 Dout 10 7 Cin Din 9

This is advance information and specifications are subject to change without notice.

MAXIMUM RATINGS (Voltages referenced to VSS)

Rating		Symbol	Value	Unit
DC Supply Voltage	rulu bluv	Vcc	-0.5 to +18	Vdc
DC Supply Voltage	- 01	VDD	-0.5 to +18	Vdc
Input Voltage, All Inputs		Vin	-0.5 to V _{CC} + 0.5	Vdc
DC Current Drain per Pin	- 81	laal	10	mAdd
Operating Temperature Range		ÚΤΑ	-55 to +125	°C
189 370	CL/CP Device	91 .	-40 to +85	
Storage Temperature Range		T _{stg}	-65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that Vin and Vout be constrained to the range VSS \leq Vin \leq VCC and VSS \leq Vout \leq VDD.

Vin < VCC and VSS < Vout < VDD.
Unused inputs must always be tied to an appropriate logic level (e.g., either VSS or VCC).

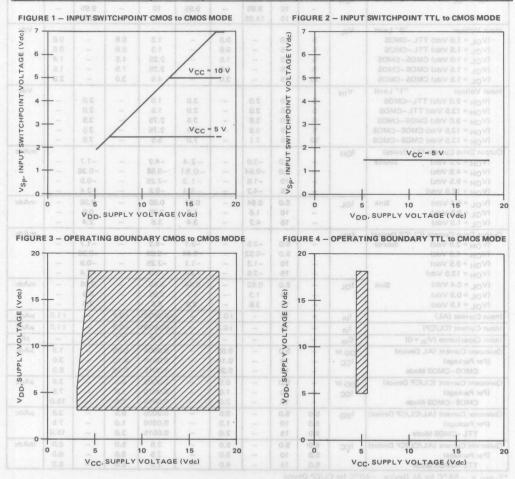
ELECTRICAL CHARACTERISTICS

0.00 1081	0.8	Vcc	VDD	Tio	w*		25°C		Thi	gh*	
Characteristic	Symbol	Vdc	Vdc	Min	Max	Min	Тур	Max	Min	Max	Unit
Output Voltage "0" Level	VOL	91	5.0		0.05		0	0.05	-	0.05	Vdd
Vin = 0 V	0.8	=	10	114	0.05	JMT	0	0.05	Fell Ties	0.05	andan)
- B0 100 -	01	=	15	-	0.05	-	0	0.05	-	0.05	- × -
Vin = VCC "1" Level	VOH		5.0	4.95		4.95	5.0		4.95	_	Vdd
00	0	_	10	9.95	-	9.95	10	_	9.95	-	
BUITCHPUINT TYL 16 CMOS MODE	TURKE -	GUEE F	15	14.95	3401	14.95	15	TOMPOR	14.95	MI 13	BUDE
Input Voltage "0" Level	VIL	- T									Vdd
(VOL = 1.0 Vdc) TTL-CMOS	12	5	10	-	0.8	-	1.3	0.8	-	0.8	8
(VOL = 1.5 Vdc) TTL-CMOS		5	15	-	0.8	1-	1.3	0.8	-	0.8	2
(VOL = 1.0 Vdc) CMOS-CMOS		5	10	-	1.5	7	2.25	1.5	-	1.4	
(VOL = 1.5 Vdc) CMOS-CMOS		5	15	-	1.5	007	2.25	1.5	-	1.5	1
(VOL = 1.5 Vdc) CMOS-CMOS		10	15	-	3.0	-	4.5	3.0	-	2.9	-8 5
Input Voltage "1" Level	VIH		< .								Vdd
(VOH = 9.0 Vdc) TTL-CMOS		5	10	2.0	-	2.0	1.5	_	2.0		P 5
(VOH = 13.5 Vdc) TTL-CMOS		5	15	2.0	-	2.0	1.5	-	2.0	-	1
(VOH = 9.0 Vdc) CMOS-CMOS		5	10	3.6	-	3.5	2.75	1-	3.5	-	. 9
(VOH = 13.5 Vdc) CMOS-CMOS		5	15	3.6	7, S	3.5	2.75	-	3.5	-	
(VOH = 13.5 Vdc) CMOS-CMOS		10	15	7.1		7.0	5.5	-	7.0	-	1 5
Output Drive Current (AL Device)	ІОН	1	2						7		mAd
(V _{OH} = 2.5 Vdc) Source	-011	-	5.0	-3.0	_	-2.4	-4.2	-	-1.7	-	. 5
(V _{OH} = 4.6 Vdc)		1	5.0	-0.64	-	-0.51	-0.88	_	-0.36		- 3
(V _{OH} = 9.5 Vdc)		_	10	-1.6	-	-1.3	-2.25	-	-0.9	-	5
(V _{OH} = 13.5 Vdc)	1	1.0	15	-4.2	-	-3.4	-8.8	_	-2.4	-	- 3
(VOL = 0.4 Vdc) Sink	loL	- U	5.0	0.64	de -	0.51	0.88	_	0.36	- 0	mAd
(VOL = 0.5 Vdc)	.OL	0	10	1.6	_	1.3	2.25	Y.139111	0.9	- 4	111110
(V _{OL} = 1.5 Vdc)	30V	-	15	4.2	_	3.4	8.8	4.7-4401	2.4	_	1000
Output Drive Current (CL/CP Device)	Іон										mAd
(VOH = 2.5 Vdc) Source	·On	THE 4 -	5.0	-2.5	DOW SO	-2.1	-42	Nnos s	-1.7	3 - 08	RUDE
(V _{OH} = 4.6 Vdc)		- 05	5.0	-0.52	_	-0.44	-0.88	_	-0.36		20
(V _{OH} = 9.5 Vdc)		1	10	-1.3	-	-1.1	-2.25	_	-0.9	_	
(V _{OH} = 13.5 Vdc)	50	1	15	-3.6	-15	-3.0	-8.8	reserve	-2.4	_	
(VOL = 0.4 Vdc) Sink	lQL	-	5.0	0.52	-10	0.44	0.88	477	0.36	-	mAd
(VOL = 0.5 Vdc)	.QL	1	10	1.3	-13	1.1	2.25	977	0.9	_	111111
(VOL = 1.5 Vdc)	8	1 3	15	3.6	- 12	3.0	8.8	1177	2.4		8.0
Input Current (AL)	lin	_	15	-	±0.1	47277	±0.00001	±0.1	112	± 1.0	μAd
Input Current (CL/CP)			15	_	±0.3	424	± 0.00001	±0.3	177	± 1.0	μAd
	lin				100	77777		112.	7777	10000	-
Input Capacitance (V _{in} = 0)	Cin	+	0	-	1-8	11211	5.0	7.5	27.4	-	pF
Quiescent Current (AL Device)	IDD or	-	5.0	-	0.05	11/2/1	0.0005	0.05	11-1	1.5	μAd
(Per Package)	Icc	-	10	-	0.10	11/2/1	0.0010	0.10	117	3.0	1
CMOS-CMOS Mode	0	+	15	-	0.20	11211	0.0015	0.20	11/2	6.0	
Quiescent Current (CL/CP Device)	IDD or	+	5.0	-	0.5	1151	0.0005	0.5	1151	3.8	μAd
(Per Package)	Icc		10	-	1.0	117-11	0.0010	1.0	117	7.5	1 8
CMOS-CMOS Mode		+	15	-	2.0	11-11	0.0015	2.0	77-7	15.0	
Quiescent Current (AL/CL/CP Device)	IDD	5.0	5.0	-	0.5	-	0.0005	0.5	-	3.8	μAd
(Per Package)		5.0	10	-	1.0	-	0.0010	1.0	-	7.5	
TTL-CMOS Mode	1	5.0	15		2.0	-	0.0015	2.0	-	15.0	1
Quiescent Current (AL/CL/CP Device)	Icc	5.0	5.0	-	5.0		2.5	5.0	1-	6.0	mAd
(Per Package)	00	5.0	10	-	5.0	15	2.5	5.0	8_	6.0	
TTL-CMOS Mode	929 V	5.0	15		5.0	(abV)	2.5	5.0	Yeer	6.0	

 $^{^*}T_{LOW} = -55\,^{\circ}\text{C}$ for AL Device, $-40\,^{\circ}\text{C}$ for CL/CP Device THIGH = $+125\,^{\circ}\text{C}$ for AL Device, $+85\,^{\circ}\text{C}$ for CL/CP Device

SWITCHING CHARACTERISTICS (C1 = 50 pF, TA = 25°C)

device conteins circuitry to protect	Unit Int	T Value	Vcc	VDD		Limits		
Characteristic	Symbol	Shifting Mode	Vdc	Vdc	Min	Тур	Max	Units
Propagation Delay, High to Low	tPHL .	TTL-CMOS	5.0	10	-	120	280	ns
	amion - or	V _{DD} > V _{CC}	5.0	15	-	120	280	1000
		CMOS-CMOS	5.0	10	_	100	240	A Indus
t to this high impadance circuit.		V _{DD} > V _{CC}	5.0	15	-	120	240	m3 30
operation it is recommended that	1 227	-55 to +125	10	150 vs	0.12-9	50	140	Operation
		CMOS-CMOS	10	5.0	O/13	160	370	
OC and VSS < Vout < VDD		Vcc > Vpp	15	5.0	-	160	370	Storage
sed inputs must always be tied to	UNIO L	00 00	15	10		160	-	-
Propagation Delay, Low to High tplh		TTL-CMOS	5.0	10	-	200	340	ns
	100	V _{DD} > V _{CC}	5.0	15	_	160	320	
		CMOS-CMOS	5.0	10	-	100	340	1
		V _{DD} > V _{CC}	5.0	15		120	340	-
			10	15	IL LOINS	50	200	1 325,01
	2800	CMOS-CMOS	10	5.0	-	160	550	
Max Min Max Unit	NUT T NIM	VCC > VDD	15	5.0	-	160	550	
	n l	300 03	15	10	Jan. 19	65	290	1
Output Rise and Fall Time	tTLH, tTHL	age ALL of	-	5.0	-	100	200	ns
	0	80.0 - 81	-	10	-	50	100	1
	N. 1 20.8	20.6	-	15		40	80	





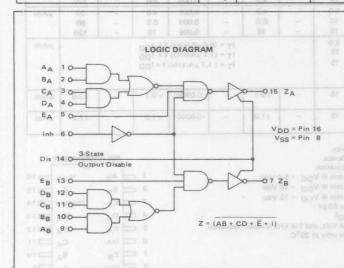
DUAL 2-WIDE, 2-INPUT EXPANDABLE AND-OR-INVERT GATE

The MC14506UB is an expandable AND-OR-INVERT gate with inhibit and 3-state output. The expand option allows cascading with any other gate, which may be carried as far as desired as long as the propagation delay added with each gate is considered. For example, the second AOI gate in this device may be used to expand the first gate, giving an expanded 4-wide, 2-input AOI gate. This device is useful in data control and digital multiplexing applications.

- Quiescent Current = 2.0 nA/Package typical @ 5 Vdc
- 3-State Output
- Separate Inhibit Line
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Lowpower Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range

MAXIMUM RATINGS (Voltages referenced to VSS)

Rating	Symbol	Value	Unit
DC Supply Voltage	VDD	-0.5 to +18	Vdc
Input Voltage, All Inputs	Vin	-0.5 to V _{DD} + 0.5	Vdc
DC Current Drain per Pin	1	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	TA	-55 to +125 -40 to +85	°C
Storage Temperature Range	T _{stg}	-65 to +150	°C



MC14506UB

CMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

DUAL EXPANDABLE



L SUFFIX CERAMIC PACKAGE CASE 620 P SUFFIX PLASTIC PACKAGE CASE 648

ORDERING INFORMATION

MC14XXXB Suffix Denotes

L Ceramic Package
P Plastic Package
A Extended Operating
Temperature Range
C Limited Operating

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum reted voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range V_{SS} < (V_{in} or V_{out}) < V_{DD}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD).

TRUTH TABLE

A	В	C	D	E	INHIBIT	DISABLE	Z
0	0	0	0	1	0	0	900-1-
0	X	0	X	1	0	0	upin.
0	X	X	0.	1	0	0	II estolue
X	0	0	X	1	0.10	101 0 ig18	if strong
X	0	X	0	1	0	0	1
1	1	X	X	X	X	0	0
X	X	1	1	X	X	0	0
X	X	X	X	0	X	0	0
X	X	X	X	X	000 101 /	0	0
×	×	×	×	X	X	ovig altum	High

X = Don't Care

MOTOROLA

ELECTRICAL CHARACTERISTICS

		VDD	-	w*		25°C			gh °	
Characteristic	Symbol	Vdc	Min	Max	Min	Тур	Max	Min	Max	Unit
Output Voltage "0" Level	VOL	5.0	-	0.05	-	0	0.05	-	0.05	Vdc
V _{in} - V _{DD} or 0		10	-	0.05	-	0	0.05	-	0.05	
		15	-	0.05	-	0	0.05	-	0.05	
"1" Level	VOH	5.0	4.95		4.95	5.0		4.95		Vdc
Vin - 0 or VDD		10	9.95	BABAG	9.95	10	S JON	9.95	ng_	
PROWER COMPLEMENTARY HOES	1071	15	14.95	-	14.95	15	-RQ-QV	14.95	_	100
Input Voltage# "0" Level	VIL		-							Vdc
(V _O = 4.5 or 0.5 Vdc)	-11	5.0	RT gate	10	QIA S	2.25	1.0	150gua	1.0	400
(V _O = 9.0 or 1.0 Vdc)		10	awalls r	2.0	в ехрал	4.50	20	and 3-	2.0	7197
(V _O = 13.5 or 1.5 Vdc)		15	वड हिंद के	2.5	nd vaim	6.75	2.5	yres risi	2.5	028
"1" Level	VIH	10	n gate in	iss ithw	v added	stals motse	080010	107 88 DO	red as to	995
(V _O = 0.5 or 4.5 Vdc)	VIH	5.0	4.0	ab sids de	4.0	2.75	eriz ele	4.0	.beasbir	Vdc
(V _O = 1.0 or 9.0 Vdc)		10	8.0	habeanx	8.0	5.50	ne feet	8.0	01-0000	Vuc
(VO = 1.5 or 13.5 Vdc)		15	12.5	a marian and a	12.5	8.25	JUNE DIN	12.5	(10) A tuo	die.
		15	12.5	e kontnes	12.5	8.25	SOLLISS S	12.5		
Output Drive Current (AL Device)	ІОН		2.0		2.4	1.0	eno.	applicat		mAdd
(VOH = 2.5 Vdc) Source	800 1	5.0	-3.0	a a fac	-2.4 -0.51	-4.2	= 2.0	-1.7	nsozajuí	0
(V _{OH} = 4.6 Vdc)	FT 3: 1	5.0	-0.64	U 20 100	7. 17. 17. 17.	-0.88		-0.36		
(V _{OH} = 9.5 Vdc)		10	-1.6	-	-1.3 -3.4	-2.25	-	-0.9	3-State C	- 00.
(V _{OH} = 13.5 Vdc)		15	-4.2	-		-8.8	-	-2.4	-	-
(VOL = 0.4 Vdc) Sink	IOL	5.0	0.64	-	0.51	0.88	-	0.36	-	mAdd
(VOL = 0.5 Vdc)	ARBO	10	1.6	-	1.3	2.25	ni ILA no	0.9	Diod & Pro	.0
(VOL = 1.5 Vdc)		15	4.2	- at	3.4	8.8	e fabris	2.4	V vitigué	0
Output Drive Current (CL/CP Device)	ГОН	1	wal an	osds, C	177 -	ALESSE AND	a Twe	sincial la	aldone	mAdd
(VOH = 2.5 Vdc) Source	-	5.0	-2.5		-2.1	-4.2	Own 1 B	-1.7	olubqb.	
(VOH = 4.6 Vdc)		5.0	-0.52	s Over t	-0.44	-0.88	2807 71	-0.36	DS JEWOI	
(VOH = 9.5 Vdc)	CATOM !	10	-1.3	-	-1.1	-2.25	- 01	-0.9	emperat	
(V _{OH} = 13.5 Vdc)	1	15	-3.6	_	-3.0	-8.8	-	-2.4	_	
(VOL = 0.4 Vdc) Sink	IOL	5.0	0.52	_	0.44	0.88	_	0.36	_	mAdo
(VOL = 0.5 Vdc)	-OL	10	1.3	_	1.1	2.25	salve-vacas	0.9	M RATIS	UMIX
(VOL = 1.5 Vdc)	1	15	3.6		3.0	8.8	-	2.4		-
Input Current (AL Device)	lin	15	- 01	±0.1	20000	±0.00001	±0.1	Greek	±1.0	μAdo
		1973.55	-	121-02:02	1 anv				DDD. 1 F.O. II.	-
Input Current (CL/CP Device)	lin	15	[80 to	± 0.3	- aiV	±0.00001	± 0.3	- 270	±1.0	μAdo
Input Capacitance	Cin	:55Am		01 -	- 1	5.0	7.5	707	Draim per	pF
(V _{in} = 0)		20	201	23	1.5		AL Gavis	s sans R s	wrenechts'	Logiter
Quiescent Current (AL Device)	IDD	5.0	- 88	1.0	-	0.002	1.0	10 -	30	μAdo
(Per Package)	disp	10	-	2.0		0.004	2.0	Toprigit	60	oT one
c voltages or electric fields; however,	1932	15	_001	4.0	211	0.006	4.0	Shrake	120	-
Quiescent Current (CL/CP Device)	Ipp	5.0		4.0	_	0.002	4.0		30	μAdo
(Per Package)	Control Control	10	_	8.0	2	0.004	8.0	_	60	Arto
high impedence circuit. For proper	mints:	15	-	16	_	0.006	16	_	120	
Total Supply Current**†	sgo IT	5.0	1		1 10					μAde
(Dynamic plus Quiescent,	voV 1	10			T = (0	.6 μA/kHz)	DD			ида
Per Package)	NV9	15	1			.1 μA/kHz)				
(C _L = 50 pF on all outputs, all	UnU I	,15			11 = (1.7 μA/kHz	1+1DD			AA
buffers switching)	idde								-0.5	AB
	Vot	15	-	1		T 0 0000:	0.4			2.0
Three-State Leakage Current	ITL	15	-00	± 0.1	1	+0.00001	± 0.1		±3.0	μAdd
(AL Device)			-					-		A.
Three-State Leakage Current		15		±1.0		+0.00001	± 1.0		± 7.5	MAdo

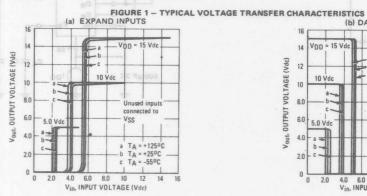
*T_{Iow} = -55°C for AL Device, -40°C for CL/CP Device.
Thigh = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-ease input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc PIN ASSIGNMENT VDD 16 2 = BA ZA = 15 2.5 Vdc min @ V_{DD} = 15 Vdc 3 - CA Disable 14 †To calculate total supply current at loads other than 50 pF: $|_{T}(C_{L}) = |_{T}(50 \text{ pF}) + 2 \times 10^{-3} (C_{L} - 50) \text{ V}_{DD} f$ where: $|_{T}$ is in μ A (per package), C_{L} in pF, V_{DD} in Vdc, and f in kHz is input frequency. *The formulas given are for the typical characteristics only at 25°C. 4 DA 13 5 EA DB 12 CB ____11 ZB 10 88 8 - VSS AB □9

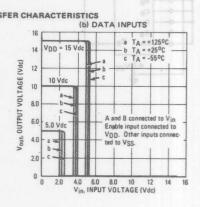
3

SWITCHING	CHARACTERISTICS*	$(C_1 = 50 \text{ pF}, T_A = 25^{\circ}\text{C})$

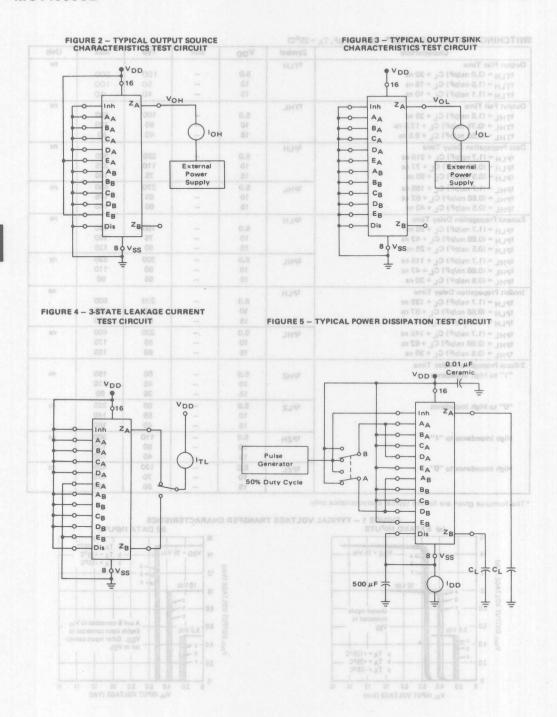
Characteristic	Symbol	VDD	Min	Тур	Max	Unit
Output Rise Time t _{TLH} = (3.0 ns/pF) C _L + 30 ns	tTLH	5.0	_	100 ac	200	ns
t _{TLH} = (1.5 ns/pF) C _L + 15 ns		10	_	50	100	
t _{TLH} = (1.1 ns/pF) C _L + 10 ns		15	-	40	80	
Output Fall Time	†THL		T-25	-0-A	dn1 o	ns
tTHL = (1.5 ns/pF) CL + 25 ns		5.0	-	100	200	46
t _{THL} = (0.75 ns/pF) C _L + 12.5 ns		10	1	50	100	4
t _{THL} = (0.55 ns/pF) C _L + 9.5 ns		15	10:(-)	40	80	
Data Propagation Delay Time	tPLH				AB 0	ns
tpLH = (1.7 ns/pF) CL + 210 ns		5.0	-	295	580	
tpLH = (0.66 ns/pF) CL + 77 ns		10	harr—coll	110	225	
tpLH = (0.5 ns/pF) CL + 50 ns		15	160291	75	180	
tpHL = (1.7 ns/pF) CL + 185 ns	tPHL	5.0	-	270	480	ns
tout = (0.66 ns/pF) Ct + 62 ns		10	-	95	175	
tpHL = (0.5 ns/pF) CL + 40 ns		15	-	65	140	
Expand Propagation Delay Time	tPLH				84 . 9	ns
tpLH = (1.7 ns/pF) CL + 95 ns		5.0	-	180	430	
tpLH = (0.66 ns/pF) CL + 42 ns		10	-	75	160	1
tpLH = (0.5 ns/pF) CL + 25 ns		15	-	50	125	
tpHL = (1.7 ns/pF) CL + 115 ns	tPHL	5.0	-	200	330	ns
tpHL = (0.66 ns/pF) CL + 47 ns		10	-	80	110	
tpHL = (0.5 ns/pF) CL + 30 ns		15	-	55	90	
Inhibit Propagation Delay Time	tPLH					ns
tpLH = (1.7 ns/pF) CL + 135 ns		5.0	-	220	500	
tpLH = (0.66 ns/pF) CL + 67 ns		10	THEREW	100	225	BRUDE
tpLH = (0.5 ns/pF) CL + 40 ns	- dishupin	15	-	65	160	
tpHL = (1.7 ns/pF) CL + 145 ns	tPHL	5.0	-	230	400	ns
tpHL = (0.66 ns/pF) CL + 62 ns		10	-	95	175	A SUMPLY OF
tpHL = (0.5 ns/pF) CL + 35 ns		15	-	60	150	
3-State Propagation Delay Time						
"1" to High Impedance	tPHZ	5.0	-	60	150	ns
1 7 616	1	10	-	45	00110	
		15		35	90	-
"0" to High Impedance	tPLZ	5.0	-aav	90	225	ns
		10	- 9	55	140	
AA CO		15	-	40	100	-
High Impedance to "1"	tPZH	5.0	-	110	300	ns
A3 0	-	10	1 -1	50	125	-
Authorities	salu1	15	- T-	40	100	
High Impedance to "0"	tPZL	5.0		170	425	ns
gA O Agely	elay Dysue	10	-	70	175	
8 -0-1		15		50	125	

*The formulae given are for the typical characteristics only.









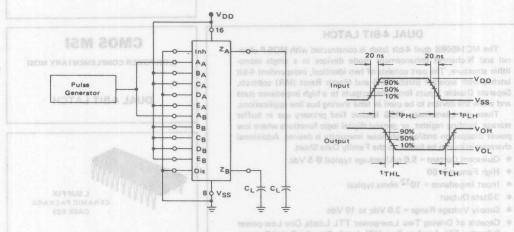
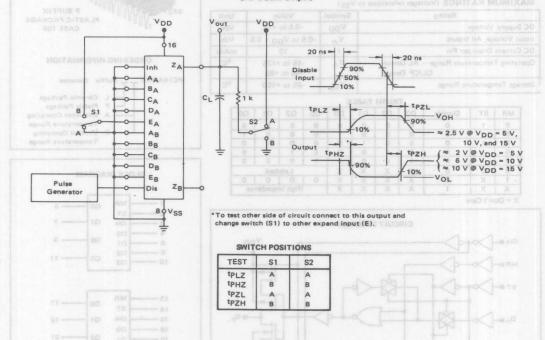


FIGURE 7 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS
(For 3-State Output)



DUAL 4-BIT LATCH

FIGURE 6 - TWITCHING TIME TEST CHICUIT AND WAVEL

The MC14508B dual 4-bit latch is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. The part consists of two identical, independent 4-bit latches with separate Strobe (ST) and Master Reset (MR) controls. Separate Disable inputs force the outputs to a high impedance state and allow the devices to be used in time sharing bus line applications.

These complementary MOS latches find primary use in buffer storage, holding register, or general digital logic functions where low power dissipation and/or high noise immunity is desired. Additional characteristics can be found on the Family Data Sheet.

- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- High Fanout > 50
- Input Impedance = 10¹² ohms typical
- 3-State Output
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load to Two HTL Loads Over the Rated Temperature Range.

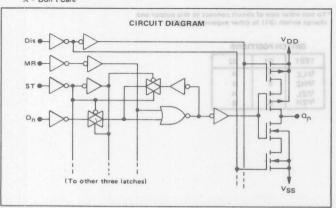
MAXIMUM RATINGS (Voltages referenced to VSS)

Rating	Symbol	Value	Unit
DC Supply Voltage	VDD	-0.5 to +18	Vdc
Input Voltage, All Inputs	Vin	-0.5 to V _{DD} + 0.5	Vdc
DC Current Drain per Pin		02 10	mAdd
Operating Temperature Range AL Device CL/CP Device	TA	-55 to +125 -40 to +85	°C
Storage Temperature Range	T _{stg}	-65 to +150	°C

	-			_
TRI	ITH	TA	RI	F

			property and the							
MR	ST	Disable	D3	D2	D1	D0	Q3	Q2	Q1	00
0	1	0	0	0	0	0	0	0	0	0
0	od V	0	0	0	0	1	0	0	0	1
0	boot.V	0	0	0	1	0	0	.0	1	0
0	101/18	V 2 0	0	1	0	0	0	1	0	0
0	not/®	A 9 0 3 -	1	0	0 .	0	1	0	0	0
0	0	0	X	X	X	X		Late	ched	
1	X	0	X	X	X	X	0	0	0	0
X	X	1	X	X	X	X		High I	mpedar	ice

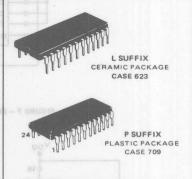
X = Don't Care



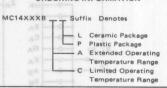
CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

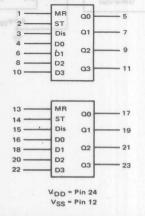
DUAL 4-BIT LATCH



ORDERING INFORMATION



BLOCK DIAGRAM



3

ELECTRICAL CHARACTERISTICS

		VDD	Tic	w*		25°C		Th	igh *	
Characteristic	Symbol	Vdc	Min	Max	Min	Тур	Max	Min	Max	Unit
Output Voltage "0" Level	VOL	5.0	-	0.05		0	0.05	_	0.05	Vdc
Vin - VDD or 0	OL.	10	_	0.05	-	0	0.05	_	0.05	JugzuC
100 200	0.8	15	_	0.05	_	0	0.05	+ 12(3d	0.05	1777
OOT OF "1" Level	Van	5.0	4.95	-	4.95	5.0	En 87	4.95	an (I,1) = 1	Vdc
Vin = 0 or VDD	VOH	10	9.95		9.95	10	En 01	9.95	an full wi	Vac
IN OSI ADD		15	14.95	_	14.95	15		14.95	pro-F lie i	
Input Voltage# "0" Level	1/	13	14.55		14.55	. 15			- UNIX D. V. STEE	1111111111
bar . arrage	VIL					0.05	1.5	12 17q	an d.1) = _	Vdc
(V _O = 4.5 or 0.5 Vdc)	10	5.0	-	1.5	_ ,	2.25	3.0	and the second	1.5	STI
(V _O = 9.0 or 1.0 Vdc)	61	10		3.0		4.50	4.0	JO +Tela	3.0	HTZ
(V _O = 13.5 or 1.5 Vdc)		15	-	4.0	-	6.75	4.0	- serial	4.0	-
094 "1" Level	VIH					gry.	Ct + 13	Rolen T.	1 10007	1 107
(V _O = 0.5 or 4.5 Vdc)	01	5.0	3.5	-	3.5	2.75	10 17 5	3.5	1 × 11497 .	Vdc
(V _O = 1.0 or 9.0 Vdc)	15	10	7.0	-	7.0	5.50	Ci 735	7.0	- Bent	1,150
(V _O = 1.5 or 13.5 Vdc)	0.2	15	11.0	-	11.0	8.25	-	11.0	-	
Output Drive Current (AL Device)	ГОН	Zarkarah.						510 (51.2.0	COLUMN XCC	mAdc
(V _{OH} = 2.5 Vdc) Source	aı	5.0	-3.0	-	-2.4	-4.2	-	-1.7	-	Mark.
(V _{OH} = 4.6 Vdc)	01	5.0	-0.64		-0.51	-0.88	_	-0.36		
(V _{OH} = 9.5 Vdc)	0.8	10	-1.6	_	-1.3	-2.25	-	-0.9	filbi@ selp	adous
(VOH = 13.5 Vdc)	01	15	-4.2	-	-3.4	-8.8	-	-2.4	-	
(V _{OL} = 0.4 Vdc) Sink	IOL	5.0	0.64		0.51	0.88	_	0.36	_	mAdc
(VOL = 0.5 Vdc)	, OL	10	1.6	_	1.3	2.25	_	0.9	- 8675	1117100
(V _{OL} = 1.5 Vdc)	01	15	4.2	_	3.4	8.8	_	2.4	_	a debar
		. 13	7.2		3.4	0.0		2.7		
Output Drive Current (CL/CP Device)	ЮН		0.5							mAdc
(V _{OH} = 2.5 Vdc) Source	0.0	5.0	-2.5	-	-2.1	-4.2	-	-1.7	on on	IT blot
(V _{OH} = 4.6 Vdc)	01	5.0	-0.52	-	-0.44	-0.88	-	-0.36	-	
(V _{OH} = 9.5 Vdc)	31	10	-1.3	-	-1.1	-2.25	-	-0.9	-	100
(V _{OH} = 13.5 Vdc)		15	-3.6	-	-3.0	-8.8	-	-2.4	-	
(VOL = 0.4 Vdc) Sink	IOL	5.0	0.52	-	0.44	0.88	- describe	0.36	of The se	mAdc
(VOL = 0.5 Vdc)	0.8	10	1.3	_	1.1	2.25	1000	0.9	D) = SHS	2
(V _{OL} = 1.5 Vdc)	0.6	15	3.6	-	3.0	8.8	1.80 4 40	2.4	D) = 5120	
Input Current (AL Device)	1 _{in}	15	-	± 0.1	-	±0.00001	±0.1	(Botto PI	± 1.0	μAdc
Input Current (CL/CP Device)	lin	15	-	± 0.3	-	±0.00001	±0.3	and the state of	±1.0	μAdc
Input Capacitance	Cin	_		_	-	5.0	7.5	(Reiso S	E0 = 5 IS	pF
(V _{in} = 0)	Cin					3.0	7.5	Figure 65	20 - 27,	Pi
1.111		5.0		5.0	-		5.0		100 2 22	
Quiescent Current (AL Device)	IDD	5.0	-	5.0	-	0.005	5.0	14d75u 92	150	μAde
(Per Package)		10	-	10	-	0.010	10	I WIT OIL	300	rigiti
- 85 170	0.8	15		20	-	0.015	20	(Rotan 14	600	7
Quiescent Current (CL/CP Device)	IDD	5.0	-	20	-	0.005	20	(Sq <u>\s</u> n 18	150	μAdc
(Per Package)	-01	10	->	40	-	0.010	40	Ladino of	300	2
60		15	-	80	-	0.015	80	"0" ot 6	600	dgild
Total Supply Current**†	IT	5.0			IT = (1	.46 μA/kHz) f + Ipp	(Fig)an 68	(0) = 32:	μAdc
(Dynamic plus Quiescent,	07	10	in the		IT = (2	.91 μA/kHz) f + IDD			7
Per Package)	. 81	15				.37 μA/kHz				2
(C ₁ = 50 pF on all outputs, all			-							
buffers switching)			1 1 10 1							not and
Three-State Leakage Current	In.	15		± 0.1		±0.00001	101		. 2.0	
(AL Device)	ITL	15	-	± 0.1	_	1,00001	± 0.1	_	±3.0	μAdc
Three-State Leakage Current			-		-			71075	101000	
	ITL	15	-	±1.0		±0.00001	±1.0	TREM	±7.5	μAdc

ar Em aro

STB TA

 $^{^{\}circ}T_{1OW}$ = $^{-55}{}^{\circ}C$ for AL Device, $^{-40}{}^{\circ}C$ for CL/CP Device. $^{\top}T_{high}$ = $^{+125}{}^{\circ}C$ for AL Device, $^{+85}{}^{\circ}C$ for CL/CP Device. #Noise immunity specified for worst-case input combination.

Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc

Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc 2.0 Vdc min @ V_{DD} = 10 Vdc 2.5 Vdc min @ V_{DD} = 15 Vdc 1 To calculate total supply current at loads other than 50 pF: $I_T(C_L) = I_T(50 \text{ pF}) + 8 \times 10^{-3} \text{ (C}_L - 50) V_{DD}$ where: I_T is in μ A (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency. *The formulas given are for the typical characteristics only at 25° C.

SWITCHING CHARACTERISTICS* (CL = 50 pF, TA = 25°C)

							-dgV	tedanio 2		All Types		
	0.00		cteristic				Symbol	VDD	Min	Тур	Max	Unit
Output Rise Tim		80.0	9		80.0		******	40			0 10 000	ns
tTLH = (3.0 r							TEH	5.0	-	100	200	
tTLH = (1.5 r							-	10	1	50	100	
tTLH = (1.1 r							0.0	15	100 a.	40	80	1000
	To the same	0 115	01	9.95		98.6	01	10		10	1000	nev-
Output Fall Time			15				THL					ns
THL = (1.5								5.0	land,	100	200	tleV tuge
tTHL = (0.75							0.6	10	-	50		- ovi
THL = (0.55	ns/pF) CL +	9.5 ns	4,50		3.0		01	15	-	40	80	= OV)
Propagation Dela	y Time		67.8		0.A		tPLH,			(dbV)	1 10 6 6	ns
tPLH, tPHL =	(1.7 ns/pF) (CL + 135	ns				tPHL	5.0	lave	220	440	
tPLH, tPHL	(0.66 ns/pF)	CL + 57	ns				0.6	10	-	90	180	- avi
tPLH, tPHL	(0.5 ns/pF) (CL + 35	ns Da.a				10	15	-	60	120	(OV)
Master Reset Pul			-010	97.11		0.11	twH(R)	5.0	200	100	100	ns
SOAM I TOSOL I GI								10	100	50	un Curren	O region
							5.0	15	70	35	2.5 Vdd	HOVE
	ar.o.	-	88.0	120-		0.64	0.3		-	-	ANV SA	110 ^{N3}
Strobe Pulse Wid							tWH(S)	5.0	140	70	155 VT6.8	ns)
							at I	10	70	35	anv attr	HOW:
abAm -	0.36					0.64	9.0	15	40	20	DEV ED	(VOL
Setup Time	6.0		2.25	6.1			tsu	5.0	50	25	0.84Vdt	ns
							el l	10	20	10	1,64/dg	130V)
								15	10	5.0	entiti se	O toglet
Hold Time	17.1-1	-	-4.2	-2.1	-	-2.5	th	5.0	0	0	2.1LVdd	ns
							5.0	10	0	0	(bbV_8.5)	HOV)
	-0.9						10	15	0	0	(bbV_8.8	HOVI
3-State Propaga	ation Delay T	ime	0.0	9.5		0.0	tPHZ				30 A 0'51	ns
	o High Imped						PHZ	101		Sink	0.4 Vdc	HJOVE
	0.49 ns/pF) C		2.25 an				7.0	5.0	-	85	170	(VOL)
	0.29 ns/pF) C						15	10	_	50	100	JON)
	0.19 ns/pF) C				1.0 ±		1 16	15	_	35	70	TUO TURO
Output "0" t		-					tou =	nil		Device)	(LJ3) 1/8	ns
	0.32 ns/pF) C ₁		5.0				tPLZ	5.0	-	65	130	G=0.1000
	0.29 ns/pF) C							10		40	80	3 = ni VI
	0.28 ns/pF) C						6.0	15	-	30	60	THE ST
The state of the s	nce to "1" Le	-					-	0.00	-	180,00	1100105	A Tribozolui
	0.41 ns/pF) C		0.010				^t PZH	E0		85	170	ns
tPZH = (61	5.0	-	50	100	
							5.0	10	- 1	35	70) the assiul
	0.30 ns/pF) C	-					10	15	-	30	70	(Por Pag
	nce to "0" Le						TPZL		-	-		ns
	0.49 ns/pF) C						0.6	5.0	-	85	170	otal Supp
	0.29 ns/pF) C						01	10	-	50	100	many(3)
tPZL = (0.19 ns/pF) C	L + 25.5	ns				31	15	-	35	70	Par Pac

*The formulae given are for the typical characteristics only.

PIN ASSIGNMENT MRA VDD 24 Q3_B 23 2 STA 3 DisA D3_B 22 4 DOA Q2B = 21 5 00A D2B = 20 Q1_B 19 D1_B 18 6 - D1A 7 01A 00_B 17 00_B 16 Dis_B 15 8 - D2A 9 = Q2A 10 D3A STB 14 MRB 13 11 = Q3A 12 VSS

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields: however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this 'high impedance circuit. For proper operation it is recommended that V_{In} and V_{out} be constrained to the range V_{SS} < (V_{In} or V_{out}) < V_{DD}.
Unused inputs must always be tied to an

Unused inputs must always be tied to an appropriate logic voltage level (e.g. either VSS or VDD).



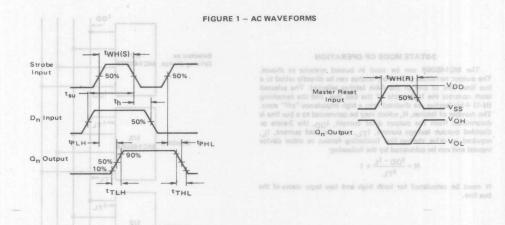
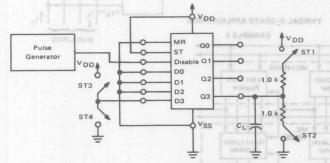
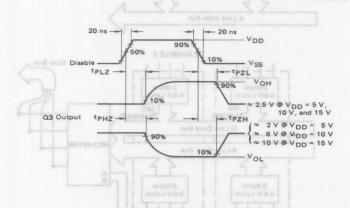


FIGURE 2 - 3-STATE AC TEST CIRCUIT AND WAVEFORMS



TEST	ST1	ST2	ST3	ST4
^t PHZ	OPEN	CLOSE	CLOSE	OPEN
TPLZ	CLOSE	OPEN	OPEN	CLOSE
tPZL	CLOSE	OPEN	OPEN	CLOSE
tPZH	OPEN	CLOSE	CLOSE	OPEN

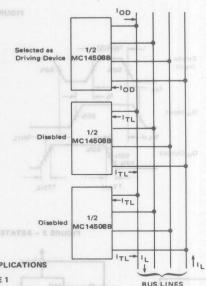


3-STATE MODE OF OPERATION

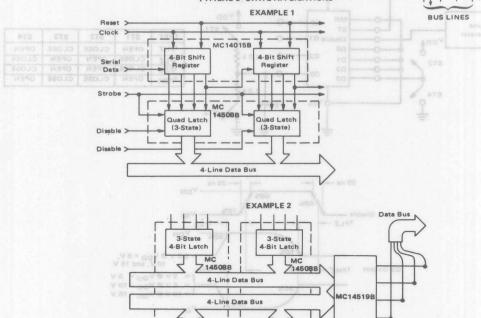
The MC14508B can be used in bussed systems as shown. The output terminals of N 4-bit latches can be directly wired to a bus line, and to one of the 4-bit latches selected. The selected latch controls the logic state of the bus line, and the remaining (N-1) 4-bit latches are disabled into a high impedance "off" state. The number of latches, N, which may be connected to a bus line is determined from the output drive current, I_{OD}, the 3-tate or disabled output leakage current, I_{TL}, and the load current, I_L, required to drive the bus line (including fanout to other device inputs) and can be calculated by the following:

$$N = \frac{I_{OD} - I_{L}}{I_{TL}} + 1$$

N must be calculated for both high and low logic states of the



TYPICAL 3-STATE APPLICATIONS



3-State

4-Bit Latch

3

3-State

4-Bit Latch



BCD UP/DOWN COUNTER

MOTOROLA

The MC14510B BCD up/down counter is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. The counter consists of type D flip-flop stages with a gating structure to provide type T flip-flop capability. The counter can be cleared by applying a high level on the Reset line. This complementary MOS counter finds primary use in up/down and difference counting and frequency synthesizer applications where low power dissipation and/or high noise immunity is desired. It is also useful in A/D and D/A conversion and for magnitude and sign generation.

- Quiescent Current = 5.0 nA/package typical @ 5.0 Vdc
- Noise Immunity = 45% of VDD typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Low Input Capacitance 5.0 pF typical
- Internally Synchronous for High Speed
- Logic Edge-Clocked Design Count Occurs on Positive Going Edge of Clock
- 5.0-MHz Counting Rate
- Asynchronous Preset Enable Operation
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range.

MAXIMUM RATINGS (Voltages referenced to VSS)

DOE Rating DA DE	Symbol	Value	Unit
DC Supply Voltage	V _{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	Vin	-0.5 to V _{DD} + 0.5	Vdc
DC Current Drain per Pin	AM 27 10 L. 34	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	TA	-55 to +125 -40 to +85	°C
Storage Temperature Range	T _{stg}	-65 to +150	°C

TRUTH TABLE

CARRY IN	UP/DOWN	PRESET	RESET	ACTION
1	X	0	0	No Count
0	1	0	0	Count Up
0	0	0	0	Count Down
X	×	000001 000	0	Preset
X	X	X	100	Reset

X = Don't Care

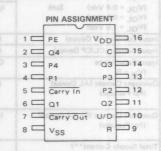
CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

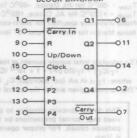
BCD UP/DOWN COUNTER



L SUFFIX CERAMIC PACKAGE CASE 620 PSUFFIX
PLASTIC PACKAGE
CASE 648



BLOCK DIAGRAM



V_{DD} = Pin 16 V_{SS} = Pin 8 3

MOTOROLA

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V _{DD} Vdc	T _{low} *		25°C			Thigh*		
			Min	Max	Min	Тур	Max	Min	Max	Unit
Output Voltage "0" Level	VOL	5.0	-	0.05		0	0.05	-	0.05	Vdc
Vin = VDD or 0		10	-	0.05	-	0	0.05		0.05	
		15	-	0.05	-	0	0.05	-	0.05	
"1" Level	VOH	5.0	4.95	- 8	4.95	5.0	G\4U 0	4.95	-	Vdc
Vin = 0 or VDD		10	9.95	-	9.95	10	-	9.95	-	
Annual volumentary standary or complete		15	14.95	hastates	14.95	15	48 T. (1)	14.95	MORE and	
nput Voltage# "0" Level	VIL	- 0	nia a ni	analusk	ebozn	a a material	line to me	Sales Ed. 1st	in lama	Vdc
(VO = 4.5 or 0.5 Vdc)		5.0	1116 6 11	1.5	NZ TO ES	2.25	1.5	MINORY IN	1.5	
(VO = 9.0 or 1.0 Vdc)		10	ents done	3.0	A3 10 101	4.50	3.0	,0103301	3.0	iom
(V _O = 13.5 or 1.5 Vdc)		15	bilitys. T	4.0	equit_1	6.75	4.0	napruss I	4.0	CHAM
"1" Level	VIH	19	11 105013	OIL HO	avai rigir	a Sankad	क राज य	MAN AN	LINE AND	000
(V _O = 0.5 or 4.5 Vdc)	- 111	5.0	3.5	gu ni azu	3.5	2.75	105 cou	3.5	complet	Vdc
(V _O = 1.0 or 9.0 Vdc)		10	7.0	applicat	7.0	5.50	paul bn	7.0	nence or	trib
(V _O = 1.5 or 13.5 Vdc)		15	11.0	b aL yth	11.0	8.25	no\bns	11.0	0 19400	reol
Output Drive Current (AL Device)	lau	10	2 DOS 5	UZ IT DIST	107 0/18	ricialeyne	D AND B	na UNA	SI HUTSSU	mAdc
(VOH = 2.5 Vdc) Source	ІОН	5.0	-3.0		-2.4	-4.2	-	-1.7	neitien.	THE
(V _{OH} = 4.6 Vdc)		5.0	-0.64		-0.51	-0.88	_	-0.36		Tring.
(VOH = 9.5 Vdc)		10	-1.6	5.04/dd	-1.3	-2.25	An-0.8 :	-0.9	aniasaiu)	0
(VOH = 13.5 Vdc)	Nan I	15	-4.2	000	-3.4	-8.8	Will Prin	-2.4	311936911/1	
			-		-	-	7 30 1031	0.36	man seich	mAdc
(V _{OL} = 0.4 Vdc) Sink	OL	5.0	0.64	-	0.51	0.88	n All Ing	0.36	Hode Pro	mAdd
(VOL = 0.5 Vdc)	" Ver	10	1.6	-	1.3	2.25			_	
(VOL = 1.5 Vdc)		15	4.2	-	3.4	8.8	1.0= 3.6	2.4	appig Ve	. 0
Output Drive Current (CL/CP Device)	ЮН				liso	ayt Rg 0	nce - 6	Capacit	ugn) we.	mAdc
(VOH = 2.5 Vdc) Source	ARED	5.0	-2.5	-	-2.1	-4.2	-	-1.70		
(V _{OH} = 4.6 Vdc)		5.0	-0.52	-	-0.44	-0.88	10/13/10/	-0.36	ylightern	1
(V _{OH} = 9.5 Vdc)	السنا	10 01	-1.3	ea9-no	m=101;	-2.25	d Dasig	-0.9	ogic-Edg	1.0
(V _{OH} = 13.5 Vdc)		15	-3.6	-	-3.0	-8.8	-	-2.4	J. lσ enb.	
(VOL = 0.4 Vdc) Sink	IOL	5.0	0.52	-	0.44	0.88	ToneF	0.36	0-MHz 0	mAdc
(VOL = 0.5 Vdc)		10	1.3	-	1.1	2.25		0.9	-	
(V _{OL} = 1.5 Vdc)		15	3.6	-	3.0	8.8	leen3 to	2.4	Syndino	0
nput Current (AL Device)	lin	15	vog-wo.	± 0.1	oJ-ITT	±0.00001	±0.1	Drifelins	±1.0	μAdc
nput Current (CL/CP Device)	lin	15 -5	egras T t	± 0.3	TrevQ s5	±0.00001	±0.3	so.LJT	±1.0	μAdc
C	Cin	-	-	-	-	5.0	7.5	- 1	ons2l shi	pF
(Vin = 0)	Cin					3.0	7.5			pr
Quiescent Current (AL Device)	IDD	5.0	-	5.0	-	0.005	5.0	-	150	μAdc
(Per Package)	.00	10	-	10	-	0.010	10	-	300	
6 01 Q2 11		15	-	20	-	0.015	20	-	600	1 1 1
Quiescent Current (CL/CP Device)	IDD	5.0	-	20	_ 12	0.005	20	ION IND	150	μAdc
(Per Package)	טטי	10	- 3	40	Linging	0.005	40	paineR	300	млис
(rei rackager		15	-81+	80	11	0.015	80	-	600	urlinas is
Total Supply Current**†	IT	5.0	-		1== 10				gnl IIA .so	μAdc
(Dynamic plus Quiescent,	- 1	10	$I_T = (0.58 \mu\text{A/kHz}) f + I_T$ $I_T = (1.2 \mu\text{A/kHz}) f + I_T$					-170/10/10		
Per Package)	-	15	$I_T = (1.2 \mu\text{A/kHz}) f + I_{DD}$ $I_T = (1.7 \mu\text{A/kHz}) f + I_{DD}$					Current		
(C ₁ = 50 pF on all outputs, all		10	17 = (1.7 μΑ/κΗ2/ T+ 10D		e Range -		rating 1			
buffers switching)			28÷							
Daniel Strikening,		-								

^{*}T_{IOW} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that Vin and Vout be constrained to the range VSS < (Vin or Vout) < VDD.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD).

Noise Margin for both "1" and "0" level = 1.0 Vdc min @ VDD = 5.0 Vdc 2.0 Vdc min @ V_{DD} = 10 Vdc

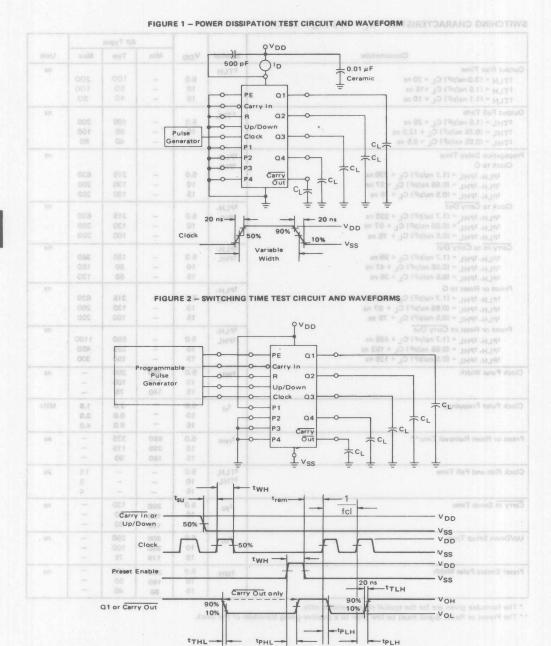
^{2.5} Vdc min @ V_{DD} = 15 Vdc

SWITCHING CHARACTERISTICS* (CL = 50 pF, TA = 25°C)

	ggVQ		All Types			
Characteristic	Symbol	VDD	Min	Тур	Мах	Unit
Output Rise Time	TTLH					ns
tTLH = (3.0 ns/pF) CL + 30 ns	0	5.0	-	100	200	
tTLH = (1.5 ns/pF) CL +15 ns		10	-	50	100	
tTLH = (1.1 ns/pF) CL + 10 ns	10 31	15	-	40	80	
Output Fall Time		-				ns
	SD THL	5.0		100	200	
t _{THL} = (1.5 ns/pF) C _L + 25 ns	nwoglqt 0	10		50	100	
tTHL = (0.75 ns/pF) CL + 12.5 ns	CO KIND OS	15	0 -	40	80	
t _{THL} = (0.55 ns/pF) C _L + 9.5 ns	100000	15	2 -	40	80	
Propagation Delay Time	tPLH.					ns
Clock to Q	tPHL			045	000	
tpLH, tpHL = (1.7 ns/pF) CL + 230 ns	V3/82 6 0-	5.0	-	315	630	
TPLH, TPHL = (0.00 ns/pr) CL + 97 ns	1300	10	-	130	260	
tpLH, tpHL = (0.5 ns/pF) CL + 75 ns	+	15	-	100	200	
Clock to Carry Out	tpLH,					ns
tpLH, tpHL = (1.7 ns/pF) CL + 230 ns	tPHL	5.0	-	315	630	
to u tour = (0.66 ns/pF) Cr + 97 ns		10	-	130	260	
tpLH, tpHL = (0.5 ns/pF) CL + 75 ns	406 904 P	15	-	100	200	
Carry In to Carry Out	******	-	-			ńs
	tPLH,	5.0	-	180	360	113
tplH, tpHL = (1.7 ns/pF) CL + 95 ns	tPHL tPHL		-	80	160	
tpLH, tpHL = (0.66 ns/pF) CL + 47 ns		10	-	100.00		
tpLH, tpHL = (0.5 ns/pF) CL + 35 ns		15	-	60	120	
Preset or Reset to Q	tPLH,					ns
tpLH, tpHL = (1.7 ns/pF) CL + 230 ns AM GMA THUBMO	tPHL	5.0	UDI 1	315	630	
tpLH, tpHL = (0.66 ns/pF) CL + 97 ns		10	-	130	260	
tpLH, tpHL = (0.5 ns/pF) CL + 75 ns		15	-	100.	200	
Preset or Reset ot Carry Out	tPLH,	-	-			ns
tp_H, tpHL = (1.7 ns/pF) CL + 465 ns	tPHL	5.0		550	1100	
tpLH, tpHL = (0.66 ns/pF) CL + 192 ns	THE	10	-	225	450	
tp[H, tpH[- (0.00 hs/pF) C[+ 132 hs	29-0-0	15		150	300	
tpLH, tpHL = (0.5 ns/pF) CL + 125 ns	مملك مطميد				300	
Clock Pulse Width	tWH	5.0	350	200	-	ns
	2011	10	170	100	- 1	
03-0	000	15	140	75	-	
Clock Pulse Frequency	fol fol	5.0	-	3.0	1.5	MHz
	29-0-02	10	-	6.0	3.0	
	£9	15	-	8.0	4.0	
Preset or Reset Removal Time**	19 trem	5.0	650	325	-	ns
	Tem	10	230	115	- 1	
		15	180	90	-	
Clock Rise and Fall Time	tTLH.	5.0	-	-	15	μs
	THL	10		-	5	
	HW7	15		_	4	
Ó I C. T	must	-	-	-	-	
Carry In Setup Time	t _{su}	5.0	200	130		ns
		10	120	60	- 1	
and the second s		15	100	50	-	
Up/Down Setup Time	tsu	5.0	500	250	-	ns
1 + 1 +	100	10	200	100	-	
	from pourt	15	175	75	-	
Preset Enable Pulse Width		FO	-	100	-	
Preser Phanie Pulse WIGTO	1 twh	5.0	200	100		ns
NUTT OF STEEL		10	100	50	_	

^{*} The formulae given are for the typical characteristics only.

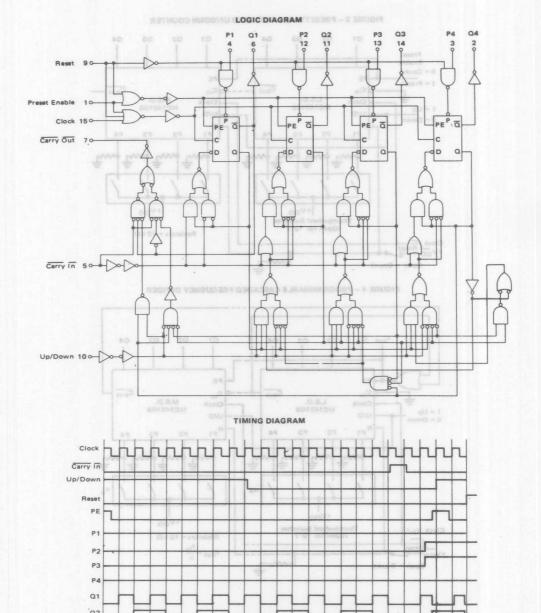
* The Preset or Reset Signal must be low prior to a positive-going transition of the clock.



Q3 Q4

Count 0

2 3 4 5 6



9 8 7

6 5 4 3 2 1 0

9

0

.7

8



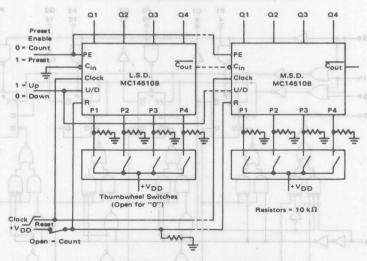
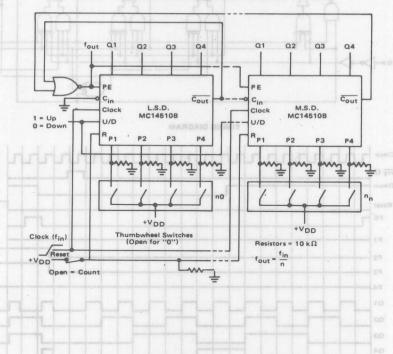


FIGURE 4 - PROGRAMMABLE CASCADED FREQUENCY DIVIDER





8-CHANNEL DATA SELECTOR

The MC14512B is an 8-channel data selector constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. This data selector finds primary application in signal multiplexing functions. It may also be used for data routing, digital signal switching, signal gating, and number sequence generation.

- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- Noise Immunity = 45% of Vpp typical
- Diode Protection on All Inputs
- High Fanout > 50
- Single Supply Operation Positive or Negative
- 3-State Output (Logic "1", Logic "0", High Impedance)
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range

MAXIMUM RATINGS (Voltages referenced to VSS)

Rating	Symbol	Value	Unit
DC Supply Voltage	V.DD	-0.5 to +18	Vdc
Input Voltage, All Inputs	Vin	-0.5 to V _{DD} + 0.5	Vdc
DC Current Drain per Pin		10	mAdo
Operating Temperature Range – AL Device CL/CP Device	_ TA	-55 to +125 -40 to +85	°C
Storage Temperature Range	Tstg	-65 to +150	°C

TRUTH TABLE

C	В	A	INHIBIT	DISABLE	1 . Z -
0	0	0	0	0	X0
0	0	1	0	0	X1
0	1	0	0	0	X2
0	1	1	0	0	Х3
1	0	0	0	0	X4
1	0	1	0	0	X5
1	1	0	0	0	X6
1	1	1	0	0	X7
φ	Φ	Φ	1	0	0
φ	0	φ	0	1 1000	High

 ϕ = Don't Care

CMOS MSI

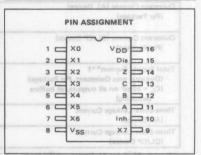
(LOW-POWER COMPLEMENTARY MOS)

8-CHANNEL DATA SELECTOR



Extended Operating Temperature Range Limited Operating

Temperature Range



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields: however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range V_{SS} (V_{in} of V_{out}) \(V_{OUT} \).

Voir or V_{out}) ≤ V_{DD}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g. either V_{SS} or V_{DD}).

an @ Vog v 16 V



ELECTRICAL CHARACTERISTICS

		VDD	Tio	w*		25°C		This	The same of the sa	
Characteristic	Symbol	Vdc	Min	Max	Min	Тур	Max	Min	Max	Unit
Output Voltage "0" Level	VOL	5.0	-	0.05	-	0	0.05	-	0.05	Vdc
Vin = VDD or 0	-	10	-	0.05	-	0	0.05	- 4	0.05	
		15	_	0.05	-	0	0.05	-	0.05	
"1" Level	VOH	5.0	4.95	-	4.95	5.0	-	4.95	-	Vdc
Vin = 0 or VDD		10	9.95	O'FOS	9.95	TA10	MIMAR	9.95	-	
		15	14.95		14.95	15	-	14.95	-	
Input Voltage# "0" Level	VIL	w batt	intonos	yesteel	data sa	fannada 3	ma ai I	14512	Ne MC	Vdc
(V _O = 4.5 or 0.5 Vdc)		5.0	- also	1.5	meonari	2.25	1.5	s lann	1.5	OM
(V _O = 9.0 or 1.0 Vdc)		10	00 000	3.0	-	4.50	3.0	-	3.0	
(V _O = 13.5 or 1.5 Vdc)	41	15	de grin	4.0	ita <u>n</u> efet	6.75	4.0	Distinc	4.0	grale
Level "1" Level	VIH	0.9871	80 0816	ABIN	-3/101	tount but	eeldriin	it intige	mi no	Vdc
(VO = 0.5 or 4.5 Vdc)	16	5.0	3.5	reg_lan	3.5	2.75	ngia_ lat	3.5	ETHAT I	data
(VO = 1.0 or 9.0 Vdc)		10	7.0	-	7.0	5.50	0	7.0	p tens	1000
(VO = 1.5 or 13.5 Vdc)		15	11.0	-	11.0	8.25	-	11.0	-	
Output Drive Current (AL Device)	ТОН	1								mAdo
(VOH = 2.5 Vdc) Source	-On	5.0	-3.0	_	-2.4	-4.2		-1.7		
(V _{OH} = 4.6 Vdc)	L	5.0	-0.64		-0.51	-0.88		-0.36	-	
(VOH = 9.5 Vdc)		10	-1.6	a <u>9</u> 1s:	-1.3	-2.25	0.8 = sn	-0.9	reageius	0
(VOH = 13.5 Vdc)		15	-4.2	-	-3.4	-8.8	20 ST	-2.4	oise In	6 8
(VOI = 0.4 Vdc) Sink	IOL	5.0	0.64	-	0.51	0.88	IIA eo a	0.36	9 shot	mAdd
(VOL = 0.5 Vdc)	.OL	10	1.6	_	1.3	2.25	- 00	0.9	is R7lpi	
(VOI = 1.5 Vdc)		15	4.2	_	3.4	8.8	-	2.4	6.5 (10)	
Output Drive Current (CL/CP Device)	ІОН	-	-	SPRING.	ON TO B	191001	100	3 3199	o nign	mAdo
(VOH = 2.5 Vdc) Source	10H	5.0	-2.5	gral ris	-2.1	-4.2	Logic "	-1.7	State (9
(V _{OH} = 4.6 Vdc)	1	5.0	-0.52	- 51	-0.44	-0.88	an-ex S	-0.36	visco:	2 0
(VOH = 9.5 Vdc)		10	-1.3		-1.1	-2.25	-	-0.9	elcisos	
(VOH = 13.5 Vdc)	10	15	-3.6	SDBO.J	-3.0	-8.8	DAK 1 BUT	-2.4	Sucrecte.	2 19
(V _{OL} = 0.4 Vdc) Sink	IOL	5.0	0.52		0.44	0.88	-	0.36	aR Sau	mAdo
(VOL = 0.5 Vdc)	,OL	10	1.3	-	1.1	2.25	-	0.9	675 516	
(VOL = 1.5 Vdc)		15	3.6	_	3.0	8:8	_	2.4	_	
Input Current (AL Device)	lin	15	-	±0.1	-	±0.00001	±0.1	-	±1.0	μAdo
Input Current (CL/CP Device)	lin	15	-	±0.3		±0.00001	±0.3	-	±1.0	μAdo
		-			Lank o	5.0	7.5	7 2211/1	TALITY	pF
Input Capacitance	Cin	-	-	-	(S=V 0	5.0	7.5			pr
(V _{in} = 0)	Upit		state's	1.100	my8	0.000		Ration	450	
Quiescent Current (AL Device)	IDD	5.0	01 B.0-	5.0	DV-	0.005	5.0	-	150 300	μAdo
(Per Package)	Vide	10	go V or d	10	v -	0.010	20	EFUIÇA	600	HOV 1
	- DOMEST	-	101	-	-	0.015			-	-
Quiescent Current (CL/CP Device)	IDD	5.0	01.88	20	1-1	0.005	20	ons Rang	150	μAdo
(Per Package)		10	OJ OB-	40	1 -	0.010	40	-	300	
at coluge at X column 8		15	-	80	1 -	0.015	. 80	-	600	
Total Supply Current**†	1T	5.0	00 00			.8 μA/kHz)				μAdd
(Dynamic plus Quiescent, Per Package)		10				.6 μA/kHz)				
(C _L = 50 pF on all outputs, all buffers		15			IT = (2	.4 μA/kHz)	f+IDD			
switching)		1								
Three-State Leakage Current	ITL	15	-	±0.1	3 (6	±0.00001	±0.1	-	±3.0	μAdd
(AL Device)				-	0,20				25	
Three-State Leakage Current	1	15	_ 3	±1.0	BARIO	±0.00001	±1.0	-0	±7.5	μAdo
Three-State Leakage Current	ITL	10	1	71.0	A COLUMN TOWN	1 0.00001	71.0	1	I / .D	MMOC

^{*}T_{low} = -55°C for AL Device, -40°C for CL/CP Device. Thigh = +125°C for AL Device, +85°C for CL/CP Device. #Noise immunity specified for worst-case input combination.

Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc 2.0 Vdc min @ V_{DD} = 10 Vdc 2.5 Vdc min @ V_{DD} = 15 Vdc

To calculate total supply current at loads other than 50 pF:

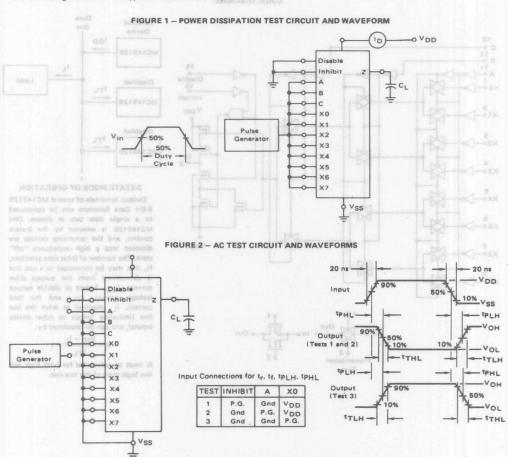
 $I_T(C_L) = I_T(50 \text{ pF}) + 1 \times 10^{-3} (C_L - 50) \text{ V}_{DD}f$

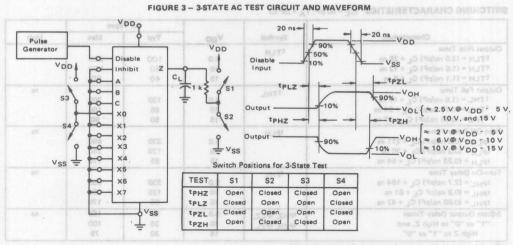
where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency. *The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS* (CL = 50 pF, TA = 25°C)

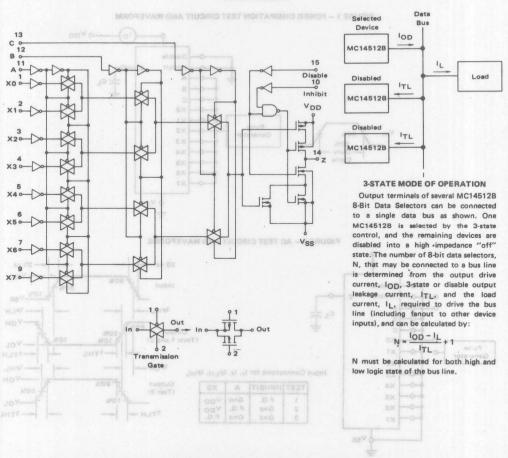
		20 news		All Ty	/pes	
Characteristic	-	Symbol	V _{DD}	Тур	Max	Unit
Output Rise Time ttlh = (3.0 ns/pF) CL + 25 ns ttlh = (1.5 ns/pF) CL + 12 ns ttlh = (1.1 ns/pF) CL + 8 ns	×08	TLH Dissole	5.0 10 15	100 stds 50 std 40	200 100 80	o V
Output Fall Time [†] THL = (1.5 ns/pF) C _L + 47 ns [‡] THL = (0.75 ns/pF) C _L + 24 ns [‡] THL = (0.55 ns/pF) C _L + 17 ns	100	tTHL regree	5.0 10 15	130 65 50	200 100 80	ns
Turn-Off Delay Time tp_H = (0.9 ns/pF) C _L + 211 ns tp_H = (0.3 ns/pF) C _L + 70 ns tp_H = (0.23 ns/pF) C _L + 54 ns	200-	tPLH	5.0 10 15	330 125 85	650 250 170	ns
Turn-On Delay Time tpHL = (2.7 ns/pF) C _L + 184 ns tpHL = (0.9 ns/pF C _L + 61 ns tpHL = (0.68 ns/pF) C _L + 47 ns	SA Dyan od Opan	tPHL and	5.0 10 15	330 125 85	650 250 170	ns
3-State Output Delay Times "1" or "0" to High Z, and High Z to "1" or "0"	in Closed ed Open	tPHZ, tPLZ, tPZH, tPZL	5.0 10 15	60 35 30	150 100 75	ns

^{*} The formulae given are for the typical characteristics only.





LOGIC DIAGRAM





MC14514B MC14515B

NOT ANT ABOUND TANTED

4-BIT TRANSPARENT LATCH/4-TO-16 LINE DECODER

The MC14514B and MC14515B are two output options of a 4 to 16 line decoder with latched inputs. The MC14514B (output active high option) presents a logical "1" at the selected output, whereas the MC14515B (output active low option) presents a logical "0" at the selected output. The latches are R-S type flip-flops which hold the last input data presented prior to the strobe transition from "1" to "0". These high and low options of a 4-bit latch/4 to 16 line decoder are constructed with N-channel and P-channel enhancement mode devices in a single monolithic structure. The latches are R-S type flip-flops and data is admitted upon a signal incident at the strobe input, decoded, and presented at the output.

These complementary circuits find primary use in decoding applications where low power dissipation and/or high noise immunity is desired.

- Quiescent Current = 5.0 nA package typical @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range
 - Single Supply Operation Positive or Negative
 - Input Impedance = 1012 ohms typical

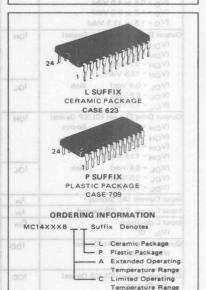
MAXIMUM RATINGS (Voltages referenced to VSS)

Rating	Symbol	Value	Unit
DC Supply Voltage	VDD.	-0.5 to +18	Vdc
Input Voltage, All Inputs	Vin	-0.5 to V _{DD} + 0.5	Vdc
DC Current Drain per Pin	1	0 = 10	mAdc
Operating Temperature Range - AL Device - CL/CP Device	TA	-55 to +125 -40 to +85	00
Storage Temperature Range	T _{stg}	-65 to +150	°C

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

4-BIT TRANSPARENT LATCH/4-TO-16 LINE DECODER



BLOCK	DIAGRAM			so	11 o Ā Ē	7.7
BLUCK	DIAGNAM				0	
To V.	D = Pin 24	danol (6.7)	supply curre	SI	10 A B	
	SS = Pin 12		10 pF) +2 ×	S2	OAB	
.00	Volacy.	Ct in pf	lugadosq 100	S3	OAB	c i
			. traquency.	S4	OAB	Ci
Data 1 0 2	o collected	A	re for the ty	S5	6 OAB	ci
	ransparent	B		S6 -	OAB	c ī
Data 2 0		В	4 to 16	S71	4 OAB	ci
Data 3 0 21-	Latch	C	Decoder	S8	18 O A B	5 1
	1	pitetic i	pid of sub si	59	17 O A B	7.7
Data 4 0 22		D	ed anoitus	\$10	20 A B	2
		is high.	of angerto	510	19 O A B	= .
L		ad zno	/ bns niV i	S11	14	CI
Strobe 0-1				S12	14 0 Ā B	CI
		radhie .	p.el tevel op	S13	13 O A B	CI
				S14	OAB	CI
				S15	15 O A B	CI

	1	ATA	NPUT	S	SELECTED OUTPUT
INHIBIT	D	С	В	A	MC14514 = Logic "1" MC14515 = Logic "0"
0	1 0	0	0	0	S0
0 90149	0	0	0	1	Thigh S1
000500	0	0	so pro	0	and some state of the state of
0	0	0	9 10	brid "	Noise Macan for lor barn I
5.0 V.O.	0	v d ni	0.0	0	54
Obv or	0	1	0	- 1	S5
		1	1	0	\$6
0 PA 91	0	7	Mark Mark	1	S7
0	1	0	0	0	S8
tong co vitius	lo1 an	0	0	Pais	\$9
s; howOver, it	1	0	10 100	0	S10
0		0		1.	S11
0 5000	-1	diam'r.	0	0	S12
0				1.	\$13
0	1	1	1	0	S14
beit od sym	1100	m 170	ani 10si	ont?	S15
1	×	X	X.	×	All Outputs = 0, MC14514 All Outputs = 1, MC14515

x = Don't Care
*Strobe = 0, Data is latched



ELECTRICAL CHARACTERISTICS

		VDD	Tic	w*		25°C		Thi	igh "	
Characteristic	Symbol	Vdc	Min	Max	Min	Тур	Max	Min	Max	Unit
Output Voltage "0" Level	VOL	5.0	-	0.05	-	0	0.05	-	0.05	Vdc
V _{in} = V _{DD} or 0		10	-	0.05	-	0	0.05	-	0.05	
		15 🖪	ECODE	0.05	81-01	0	0.05	NSPAR	0.05	1-B
"1" Level	VOH	5.0	4.95		4.95	5.0	MC14	4.95	POST AN	Vdc
Vin = 0 or VDD	011	10	9.95	orado an	9.95	10	81 ON 0	9.95	ne deco	18
OW-POWER COMPLEMENTARY MOST	40	15	14.95	10) 8017	14.95	15	latched	14.95	ine decor	OI.
Input Voltage# "0" Level	VIL	- 66	LOTHER 'T	Spino tea	point at	10 1 1	saigot a	NATION OF THE	(Lincing)	Vdc
(VO = 4.5 or 0.5 Vdc)	-15	5.0	"O" Ispi	1.5	paero_(n	2.25	1.5	dano) Bi	1.5	810
(V _O = 9.0 or 1.0 Vdc)		10	orl doidy	3.0	f egyt	4.50	3.0	Jugino	3.0	orb
(V _O = 13.5 or 1.5 Vdc)	4-81	15	" mont i	4.0	adezta e	6.75	4.0	data pa	4.0	artt
"1" Level	VIH	15	enil al	4.0	1121.5	0.75	a wor b	is rigin s	BBIT U	GI-7
(V _O = 0.5 or 4.5 Vdc)	VIH	5.0	3.5	no lanco	3.5	2.75	A driw	3.5	00 516 1	Vdc
(V _O = 1.0 or 9.0 Vdc)		10		10 -1010 5 -1010		5.50	sor - sta	7.0	ominach a	om
•			7.0	235 T 257 I	7.0	8.25		11.0	noth-sitt	Louis
(V _O = 1.5 or 13.5 Vdc)		15	11.0	Hotel Iso	11.0					MAN.
Output Drive Current (AL Device)	ІОН				dine au	sented at t	and bna	babasab	'andura	mAdd
(V _{OH} = 2.5 Vdc) Source		5.0	-1.2	poel s ei e	-1.0	-1.7 ati	NY CHES	-0.7	ROO-DEED	
(V _{OH} = 4.6 Vdc)		5.0	-0.25	notee in	-0.2	-0.36	wer diss	-0.14	nerior an	1160
(V _{OH} = 9.5 Vdc)		10	-0.62	-	-0.5	-0.9	-	-0.35	- ,be	desir
(V _{OH} = 13.5 Vdc)		15	-1.8		-1.5	-3.5	4-00	-1.1	-	-
(VOL = 0.4 Vdc) Sink	IOL	5.0	0.64	201.0	0.51	0.88	C 3 - 1070	0.36	-	mAdd
(V _{OL} = 0.5 Vdc)		10	1.6	-	1.3	2.25	/ to_3021	0.9	nmi_9210	1
(VOL = 1.5 Vdc)		15	4.2	-	3.4	8.8),E - epr	2.4	aV ₩gqs	0
Output Drive Current (CL/CP Device)	ГОН	-	unnawn.	ds, Orie	ol IT	sewon-wa	J owT	Driving 1	o sidada	mAdd
(VOH = 2.5 Vdc) Source	0	5.0	-1.0	ta/Farit	-0.8	-1.7	wTho I	-0.6	valmods	
(V _{OH} = 4.6 Vdc)		5.0	-0.2	-	-0.16	-0.36	-	-0.12	ere St. com	
(Vou = 9.5 Vdc)		10	-0.5	-	-0.4	-0.9	-	-0.3	-	1
(V _{OH} = 13.5 Vdc)		15	-1.4	- 1	-1.2	-3.5	- Topite	-1.0	dag albu	8 9
(VOL = 0.4 Vdc) Sink	IOL	5.0	0.52	-	0.44	0.88	10 STUT	0.36	gmuruq	mAdd
(VOL = 0.5 Vdc)	·OL	10	1.3	-	1.1	2.25	-	0.9	_	-
(VOL = 1.5 Vdc)		15	3.6	_	3.0	8.8	-	2.4		
Input Current (AL Device)	1.	15	-	± 0.1	- 10	±0.00001	± 0.1	1.071.20	±1.0	μAdo
	lin	15	-	± 0.3	1000	±0.00001	±0.3	greater	±1.0	#Add
Input Current (CL/CP Device)	lin	15	01	₹0.3	1 00				₹1.0	1
Input Capacitance (Vin = 0)	Cin	obV	8.0 + c	gV ara 0	njV	5.0	7.5	eti	get IIA .s	pF
Quiescent Current (AL Device)	IDD	5.0	-	5.0	-	0.005	5.0	- 100	150	μAdo
(Per Package)		10	125-	10	-p.T	0.010	10 A	Rauge -	300	at Suits
		15	- 88	20	-	0.015	20	UD -	600	
Quiescent Current (CL/CP Device)	IDD	5.0	150_	20	maT.	0.005	20	_sgns	150	μAdd
(Per Package)	00	10	-	40	-	0.010	40		300	1
	-	15	-	80	-"	0.015	80	-	600	
Total Supply Current**1	1 _T	5.0			I== (1	.35 μA/kHz) f + 1e =			LAdd
(Dynamic plus Quiescent,	т апоэзо	10	1 11		IT = (2	.70 μA/kHz) f + loo			MAGG
Per Package)	1 300331	15				.05 µA/kHz				
(C ₁ = 50 pF on all outputs, all	TAG	10			. 1 . (**)	.OJ MAIKINZ	שטי			
buffers switching)	TAU.		1 11							

^{*}T_{Iow} = -55°C for AL Device, -40°C for CL/CP Device. Thigh = +125°C for AL Device, +85°C for CL/CP Device. #Noise immunity specified for worst-case input combination. Noise Margin for both "1" and "0" level =

1.0 Vdc min @ V_{DD} = 5.0 Vdc 2.0 Vdc min @ V_{DD} = 10 Vdc 2.5 Vdc min @ V_{DD} = 15 Vdc TTo calculate total supply current at loads other than 50 pF: $\frac{1}{17}(C_L) = \frac{1}{17}(50 \text{ pF}) + 2 \times 10^{-3} \ (C_L - 50) \ \text{V}_{DD}f$ where: $\frac{1}{17}$ is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.

**The formulas given are for the typical characteristics only at 25°C.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{Out}) \leq V_{DD}$.

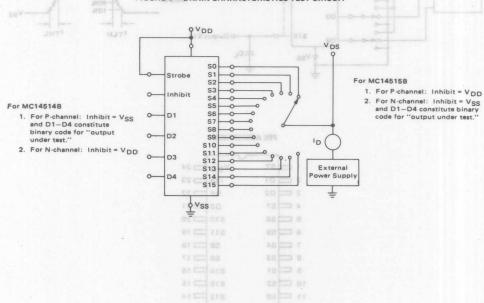
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or $V_{\mbox{DD}}$).

SWITCHING CHARACTERISTICS* (CL = 50 pF, TA = 25°C)

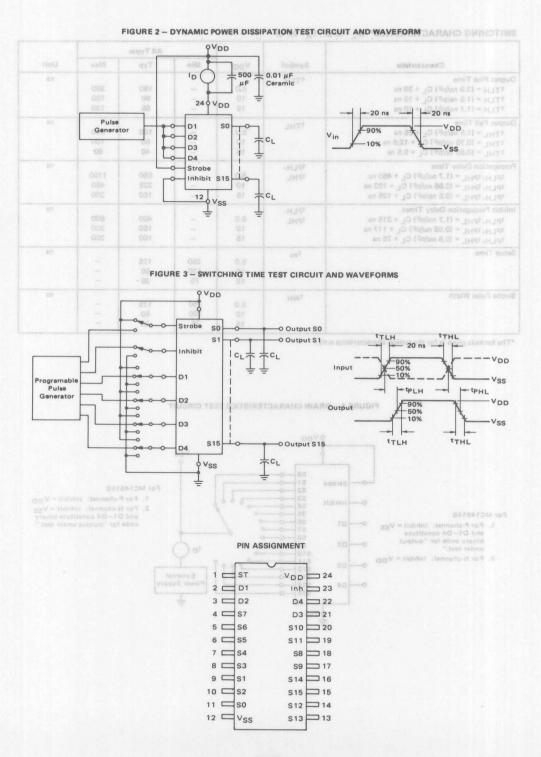
		130	V9	All Types		
Characteristic	Symbol	VDD	Min	Тур	Max	Unit
Output Rise Time	tTLH	市等等	001			ns
tTLH = (3.0 ns/pF) CL + 30 ns		5.0	-	180	360	
tTLH = (1.5 ns/pF) C1 + 15 ns		10	Library I	90	180	
tTLH = (1.1 ns/pF) CL + 10 ns		15	LY-	65	130	
Output Fall Time	tTHL	-0-100	10		Pulsa	ns
t _{THL} = (1.5 ns/pF) C _L + 25 ns	1111	5.0	50-	100	200	
tTHL = (0.75 ns/pF) CL + 12.5 ns		10		50	100	
t _{THL} = (0.55 ns/pF) C _L + 9.5 ns		15	50	40	80	
Propagation Delay Time	tPLH,		ede118			ns
tpLH, tpHL = (1.7 ns/pF) CL + 465 ns	tPHL	5.0	ateliates -	550	1100	
tpLH, tpHL = (0.66 ns/pF) CL + 192 ns		10	-	225	450	
tpLH, tpHL = (0.5 ns/pF) CL + 125 ns		15	1, 51-	150	300	
Inhibit Propagation Delay Times	tPLH,		1	DESTRUCTION OF THE PARTY OF THE		ns
tpLH, tpHL = (1.7 ns/pF) CL + 315 ns	tPHL	5.0	-	400	800	
tpLH, tpHL = (0.66 ns/pF) CL + 117 ns		10	-	150	300	
tpLH, tpHL = (0.5 ns/pF) CL + 75 ns		15	-	100	200	
Setup Time	t _{su}					ns
		5.0	250	125	-	
AND WAVEFORMS		10	100	50	-	
		15	75	38	-	
Strobe Pulse Width	tWH		dove			ns
		5.0	350	175	-	
		10	100	50	-	
		15	75	38	-	

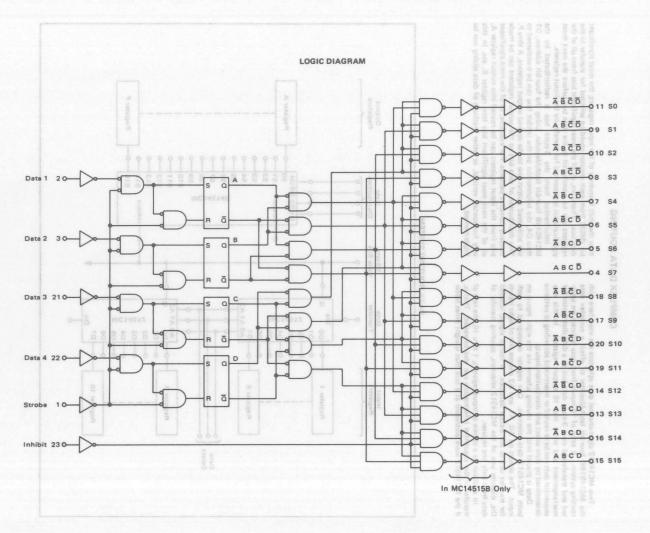
^{*}The formula given is for the typical characteristics only.

FIGURE 1 - DRAIN CHARACTERISTICS TEST CIRCUIT









COMPLEX DATA ROUTING

Two MC14512 eight-channel data selectors are used here with the MC14514B four-bit latch/decoder to effect a complex data routing system. A total of 16 inputs from data registers are selected and transferred via a 3-state data bus to a data distributor for rearrangement and entry into 16 output registers. In this way sequential data can be re-routed or intermixed according to patterns determined by data select and distribution inputs.

Data is placed into the routing scheme via the eight inputs on both MC14512 data selectors. One register is assigned to each input. The signals on AO, A1, and A2 choose one of eight inputs for transfer out to the 3-state data bus. A fourth signal, labelled Dis, disables one of the MC14512 selectors, assuring transfer of data from only one register.

In addition to a choice of input registers, 1 thru 16, the rate of transfer of the sequential information can also be varied. That is, if the MC14512 were addressed at a rate that is eight times faster

than the shift frequency of the input registers, the most significant bit (MSB) from each register could be selected for transfer to the data bus. Therefore, all of the most significant bits from all of the registers can be transferred to the data bus before the next most significant bit is presented for transfer by the input registers.

Information from the 3-state bus is redistributed by the MC14514B four-bit latch/decoder. Using the four-bit address, D1 thru D4, the information on the inhibit line can be transferred to the addressed output line to the desired output registers, A thru P. This distribution of data bits to the output registers can be made in many complex patterns. For example, all of the most significant bits from the input registers can be routed into output register A, all of the next most significant bits into register B, etc. In this way horizontal, vertical, or other methods of data slicing can be implemented.

DATA ROUTING SYSTEM Input Data 3-State Output Data Registers Distribution Registers Register 1 DO 0 0-D1 0-D2 4512 0-D3 D1 D2 D3 D4 Register A SO 0-D4 S1 0 D5 S2 -0 0 D6 S3 -0 D7 Register 8 S4 A0 A1 A2 -0 55 -0 56 0 Data S7 -0 Select **S8** -0 S9 S10 -0 AO A1 S11 -0 Register 9 DO -0 0-D1 -0 \$13 D2 4512 nhibit S14 0 D3 Register P \$15 D4 MC1 0-D5 D6 D7 Register 16

3



MC14516B

BINARY UP/DOWN COUNTER

The MC14516B is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. This complementary MOS circuit finds primary use where low power dissipation and/or high noise immunity is desired.

This binary presettable up/down counter may be used as a counting/frequency synthesizer, in A/D and D/A conversion, for up/down counting, for magnitude and sign generation, and for difference counting.

- Quiescent Current = 5.0 nA/package typical @ 5.0 Vdc
- Noise immunity = 45% of VDD typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Low Input Capacitance 5.0 pF typical
- Internally Synchronous for High Speed
- Logic Edge-Clocked Design Count Occurs on Positive Going Edge of Clock
- 5.0-MHz Counting Rate
- Single Pin Reset
- Asynchronous Preset Enable Operation
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range

MAXIMUM RATINGS (Voltages referenced to VSS)

LobAu Ger Rating 00 800	Symbol	Value	Unit
DC Supply Voltage — 04 04	V _{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	Vin	-0.5 to V _{DD} + 0.5	Vdc
DC Current Drain per Pin	# 88.01 = 11	10	mAdd
Operating Temperature Range — AL Device CL/CP Device	TA	-55 to +125 -40 to +85	°C
Storage Temperature Range	T _{stg}	-65 to +150	°C

TRUTH TABLE

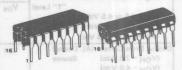
CARRY IN	UP/DOWN	PRESET ENABLE	RESET	ACTION
1	×	0	0	No Count
0	1	0	0	Count Up
0	0	0	0	Count Down
×	X	1	0	Preset
×	×	×	1 -	Reset

X = Don't Care

CMOS MSI

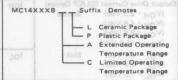
(LOW-POWER COMPLEMENTARY MOS)

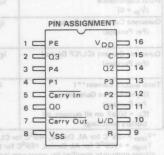
BINARY UP/DOWN COUNTER



L SUFFIX CERAMIC PACKAGE CASE 620 P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION





This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD).

MOTOROLA

ELECTRICAL CHARACTERISTICS

		VDD	Tic	ow*		25°C		Thi	igh *	
Characteristic	Symbol	Vdc	Min	Max	Min	Тур	Max	Min	Max	Unit
Output Voltage "0" Level	VOL	5.0	-	0.05	-	0	0.05	-	0.05	Vdc
Vin = VDD or 0		10	-	0.05	-	0	0.05	-	0.05	
CMOS MS1		15	-	0.05	-	0	0.05	-	0.05	
"1" Level	VOH	5.0	4.95		4.95	5.0	VAC AL	4.95	-	Vdc
Vin = 0 or VDD	(1.1)	10	9.95		9.95	10	110 11	9.95	-	
		15	14.95	_	14.95	15	_	14.95		
Input Voltage# "0" Level	VIL		THE PROPERTY.	pula jairi	511319 6	NAME OF TAXABLE PARTY.	BUUDDEN	3.51 0.01	ONE OWN O	Vdc
(V _O = 4.5 or 0.5 Vdc)	418	5.0	ure_This	1.5	rilogom	2.25	1.5	b sbam	1.5	enina
(V _O = 9.0 or 1.0 Vdc)	-	10	aib rewor	3.0	W 920 Y	4.50	3.0	MDS d	3.0	comp
(V _O = 13.5 or 1.5 Vdc)		15	_	4.0	,best	6.75	4.0	on daid t	4.0	sipet
"1" Level	VIH		g 86 558	ad vs	ก าอโกเ	down co	gu sige	fessing a	nanid ai	T
(Vo = 0.5 or 4.5 Vdc)	1	5.0	3.5	avnos A	0 3.5	2.75	esizerin	3.5	ing/frequ	Vdc
(V _O = 1.0 or 9.0 Vdc)	E305	10	7.0	ns .eoits	7.0	5.50	dinesm	7.0	ntro - nwe	p/an
(V _O = 1.5 or 13.5 Vdc)		15	11.0		11.0	8.25	-	11.0	itm a o es	naret
Output Drive Current (AL Device)	Tarre 1	10	11.0		11.0	0.25		11.0	BHIDOD BS	mAdc
(VOH = 2.5 Vdc) Source	ІОН	5.0	-3.0	- CONTROL	-2.4	-4.2		-1.7		
(V _{OH} = 4.6 Vdc)	1	5.0	-0.64	obtV 0.	-0.51	-0.88	5.0 mA/g	-0.36) sh o sasii	0.0
(V _{OH} = 9.5 Vdc)		10	-1.6		-1.3	-2.25	V 10 378	-0.36	ise imme	M.e.
(V _{OH} = 13.5 Vdc)	CERA	15	-4.2		-3.4	-8.8	mmi IIA	-2.4	ode Prote	0.0
The same and the s		-	-				pqra un			-
(VOL = 0.4 Vdc) Sink	IOL	5.0	0.64	-	0.51	0.88	ge = 5.0	0.36	lo V-yiqq	mAdc
$(V_{OL} = 0.5 \text{ Vdc})$		10	1.6		1.3	2.25	nce 5.1	0.9	Jugal ve	10
1101 1.0 1007		15	4.2	_	3.4	8.8	_	2.4	-	
Output Drive Current (CL/CP Device)	IOH					gaade ubs	TOT BUG	ynenrony	e Aneura	mAdc
(V _{OH} = 2.5 Vdc) Source	100	5.0	-2.5	tizofi no	-2.1	-4.2	Design	-1.7	gic Edge	10
(V _{OH} = 4.6 Vdc)	1	5.0	-0.52	-	-0.44	-0.88	-	-0.36	ge of Cld	18
(V _{OH} = 9.5 Vdc)		10	-1.3	-	-1.1	-2.25	-	-0.9	O-MHz Co	3 0
(V _{OH} = 13.5 Vdc)		15	-3.6	-	-3.0	-8.8	_ 918	-2.4	SPI ZELISIA	0 9
(VOL = 0.4 Vdc) Sink	IOL	5.0	0.52	-	0.44	0.88	-	0.36	i ni2 sigi	mAdc
(V _{OL} = 0.5 Vdc)		10	1.3	-	1.1	2.25	Enable	0.9	nomony	AO
(V _{OL} = 1.5 Vdc)		15	3.6		3.0	8.8	-	2.4	-	-
Input Current (AL Device)	lin	15		± 0.1	200	±0.00001	±0.1	011111111111111111111111111111111111111	±1.0	μAdc
Input Current (CL/CP Device)	lin	15	sdino.	± 0.3	101010	±0.00001	±0.3	-	±1.0	μAdc
Input Capacitance	Cin	-	-	-	_	5.0	7.5	-	-	pF
(V _{in} = 0)	oin					0.0	7.5			
Quiescent Current (AL Device)	1	5.0	-	5.0	-	0.005	5.0	-	150	μAdc
(Per Package)	IDD	10	1 -	10		0.005	10		300	μΑας
		15		20	- 10	0.015	20	Hava 22	600	UMIX
1 CE PE Van 16	-	_	-		1 Taillan					
Quiescent Current (CL/CP Device)	IDD	5.0		20	1048min	0.005	20	211/10/1	150	μAdc
(Per Paçkage)		10	-879	40	40,	0.010	40	-	300	Supply
		15	3010	80	- 9	0.015	80	- 10	600	stloV to
Total Supply Current**†	IT	5.0			IT = (0	.58 µA/kHz	f + IDD			μAdc
(Dynamic plus Quiescent,		10	801			.2 µA/kHz)				T pnine
Per Package)		15			T = (1	.7: µA/kHz)	f + IDD			-
(C _L = 50 pF on all outputs, all			-							
buffers switching)			087							119 1 996

^{*}Tlow = -55°C for AL Device, -40°C for CL/CP Device.

Thigh = +125°C for AL Device, +85°C for CL/CP Device.

#Noise immunity specified for worst-case input combination.

Noise Margin for both "1" and "0" level = 1.0 Vdc min @ VDD = 5.0 Vdc

than maximum rated voltages to this high impactance gircuit. For proper operation it is recommended that $V_{\rm in}$ and $V_{\rm out}$ be constrained to the range $V_{\rm SS} \leqslant |V_{\rm in}|$ or

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^{2.0} Vdc min @ V_{DD} = 10 Vdc 2.5 Vdc min @ V_{DD} = 15 Vdc

^{2.5} Vdc min @ V_{DD} = 15 Vdc

†To calculate total supply current at loads other than 50 pF: $|\tau(C_L)| = |\tau(50 \text{ pF}) + 1 \times 10^{-3} \text{ (}C_L - 50) \text{ V}_{DD}$ where: $|\tau|$ is in μ A (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.

*The formulas given are for the typical characteristics only at 25°C.

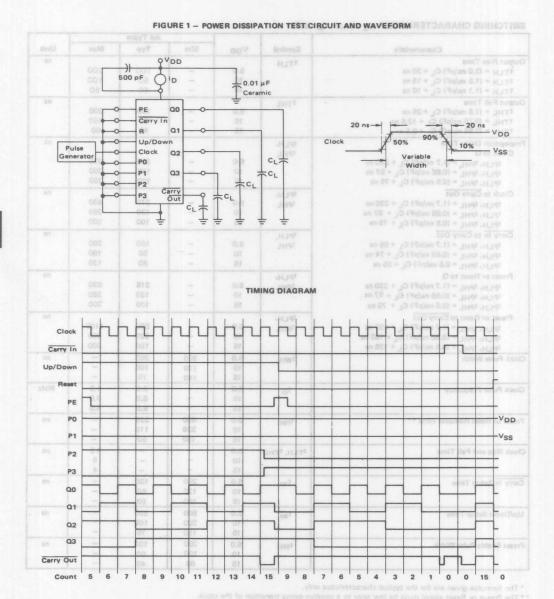
SWITCHING CHARACTERISTICS* (CL = 50 pF, TA = 25°C) MORTANDARD MEMORA - 1 3 FUGA

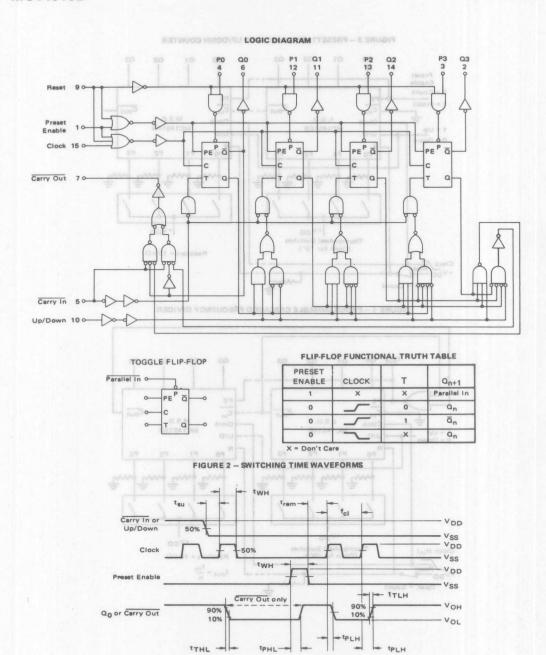
				All Types		-
Characteristic	Symbol	VDD	Min	Тур	Max	Unit
Output Rise Time	†TLH		99	10		ns
tTLH = (3.0 ns/pF) CL + 30 ns	1	5.0	-	100	200	
tTLH = (1.5 ns/pF) CL + 15 ns		10	- 0	50	100	
tTLH = (1.1 ns/pF) CL + 10 ns	olo	15	-	40	80	
Output Fall Time	†THL					ns
tTHL = (1.5 ns/pF) CL + 25 ns		5.0	-0	100	200	
tTHL = (0.75 ns/pF) CL + 12.5 ns		10	-	50	100	
tTHL = (0.55 ns/pF) CL + 9.5 ns		15	0	40	80	
Propagation Delay Time	tPLH,			wed/qu/	2-4	ns
Clock to Q	tPHL		0	2000	0	-5
tpLH, tpHL = (1.7 ns/pF) CL + 230 ns	75.75	5.0	-	315	630	100
tpLH, tpHL = (0.66 ns/pF) CL + 97 ns	107	10	-0 80	130	260	
tpLH, tpHL = (0.5 ns/pF) CL + 75 ns		15	-	100	200	
Clock to Carry Out	tPLH,	1997	C	10 pe		ns
tpLH, tpHL = (1.7 ns/pF) CL + 230 ns	tPHL	5.0	790	315	630	
tpLH, tpHL = (0.66 ns/pF) CL + 97 ns	THE	10	不足	130	260	
tplH, tpHL = (0.5 ns/pF) CL + 75 ns	4 4	15	+-	100	200	
Carry In to Carry Out	to u		-			ns
	tPLH,	5.0	_	180	360	113
tpLH, tpHL = (1.7 ns/pF) CL + 95 ns	tPHL				160	
tPLH, tPHL = (0.66 ns/pF) CL + 74 ns		10	-	80		
tpLH, tpHL = 0.5 ns/pF) CL + 35 ns		15	_	60	120	
Preset or Reset to Q	tPLH.					ns
tpLH, tpHL = (1.7 ns/pF) CL + 230 ns	tPHL	5.0	-	315	630	1 3
tPLH, tPHL = (0.66 ns/pF) CL + 97 ns	desirente par	10	-	130	360	108
tpLH, tpHL = (0.5 ns/pF) CL + 75 ns		15	-	100	200	
Preset or Reset to Carry Out	ФLH,	1 1				ns
tpLH, tpHL = (1.7 ns/pF) CL + 465 ns	TPHL	5.0		550	1100	100
tpLH, tpHL = (0.66 ns/pF) CL + 192 ns		10		225	450	and the same
tpLH, tpHL = (0.5 ns/pF) CL + 125 ns		15	-	150	300	JE 19965
Clock Pulse Width	twH	5.0	350	200	-	ns
		10	170	100		We/Stown
		15	140	75	-	
Clock Pulse Frequency	fci	5.0		3.0	1.5	MHz
		10	-	6.0	3.0	
		15	-	8.0	4.0	
Preset or Reset Removal Time **	trem	5.0	650	325		ns
	10111	10	230	115	-	
se ^V		15	180	90		9
Clock Rise and Fall Time	TLH, THE	5.0			15	μs
	Ten, The	10	-	_	5	
		15	-	-	4	
Carry In Setup Time	tsu	5.0	260	130	- 1	ns
Curry in Octob Time	`su	10	120	60		110
		15	100	50		
Ha (David Satura Time				-		-
Up/Down Setup Time	t _{su}	5.0	500	250		ns
		10	200	100		2
		15	150	75		-
Preset Enable Pulse Width	twH	5.0	200	100		ns
		10	100	50		
		15	80	40	-	Comy St

^{*} The formulae given are for the typical characteristics only.

**The Preset or Reset signal must be low prior to a positive-going transition of the clock.









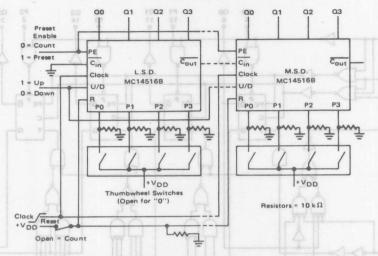
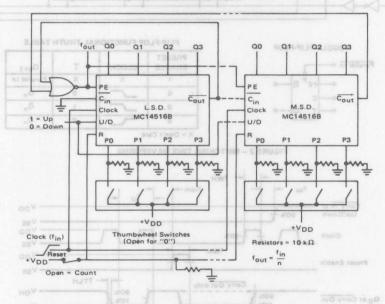


FIGURE 4 - PROGRAMMABLE CASCADED FREQUENCY DIVIDER





DUAL 64-BIT STATIC SHIFT REGISTER

The MC14517B dual 64-bit static shift register consists of two identical, independent, 64-bit registers. Each register has separate clock and write enable inputs, as well as outputs at bits 16, 32, 48, and 64. Data at the data input is entered by clocking, regardless of the state of the write enable input. An output is disabled (open circuited) when the write enable input is high. During this time, data appearing at the data input as well as the 16-bit, 32-bit, and 48-bit taps may be entered into the device by application of a clock pulse. This feature permits the register to be loaded with 64 bits in 16 clock periods, and also permits bus logic to be used. This device is useful in time delay circuits, temporary memory storage circuits, and other serial shift register applications,

- Quiescent Current = 10 nA/package typical @ 5 Vdc
- Noise Immunity = 45% of VDD typical
- Diode Protection on All Inputs
- Fully Static Operation
- Output Transitions Occur on the Rising Edge of the Clock Pulse
- 6.7 MHz Operation @ VDD = 10 Vdc
- Exceedingly Slow Input Transition Rates May Be Applied to the Clock Input
- 3-State Output at 64th-Bit Allows Use in Bus Logic Applications
- Shift Registers of any Length may be Fully Loaded with 16 Clock Pulses
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range

MAXIMUM RATINGS (Voltages referenced to Vss)

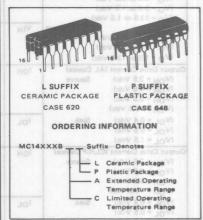
Rating	Symbol	Value	Unit
DC Supply Voltage	VDD	-0.5 to +18	Vdc
Input Voltage, All Inputs	Vin	-0.5 to V _{DD} + 0.5	Vdc
DC Current Drain per Pin	Au 7.871- yi	10	mAdo
Operating Temperature Range — AL Device CL/CP Device	TA	-55 to +125 -40 to +85	°C
Storage Temperature Range	T _{stg}	-65 to +150	°C

CMOS LSI

MC14517B

(LOW-POWER COMPLEMENTARY MOS)

DUAL 64-BIT STATIC SHIFT REGISTER



Cin		IN ASSI	GNMENT	nput Capacit (V = niV)
		tonesol.	-	
	1 =	Q16A	VDD	16
	2 🖂	Q48A	Q16 _B	15
	3 🖂	WEA	Q48 _B	14
	4 🗆	CA	WEB	13
-	5 🖂	Q64A	CB	1 2
	6 🖂	Q32A		11
	7 =		Q32B	□ 10
	8 🖂	Vss	DB	9 0

	01.0014	WRITE	DATA	16-BIT TAP	32-BIT TAP	48-BIT TAP	64-BIT TAP
	CLOCK	ENABLE	DATA	16-BIT TAP	32-BITTAP	48-BITTAP	04-BII IAP
	0	0	×	Content of 16-Bit Displayed	Content of 32-Bit Displayed	Content of 48-Bit Displayed	Content of 64-Bi Displayed
	0	1	×	High Impedance	High Impedance	High Impedance	High Impedance
FUNCTIONAL	1	0	×	Content of 16-Bit Displayed	Content of 32-Bit Displayed	Content of 48-Bit Displayed	Content of 64-B Displayed
TRUTH TABLE	1	1	×	High Impedance	High Impedance	High Impedance	High Impedance
	5	0	Data entered into 1st Bit	Content of 16-Bit Displayed	Content of 32-Bit Displayed	Content of 48-Bit Displayed	Content of 64-B Displayed
	5	1	Data entered into 1st Bit	Data at tap entered into 17-Bit	Data at tap entered into 33-Bit	Data at tap entered into 49-Bit	High Impedance
	~	0	×	Content of 16-Bit Displayed	Content of 32-Bit Displayed	Content of 48-Bit Displayed	Content of 64-B Displayed
	~	1	X	High Impedance	High Impedance	High Impedance	High Impedance

ELECTRICAL CHARACTERISTICS

Symbol	Vdc	Min	Max	Min	Тур	Max	Min	Max	Unit
VOL					. 16		141111	IVBIVI	Unit
	5.0	-	0.05	-	0	0.05	-	0.05	Vdc
	10	-	0.05	-	0	0.05	-	0.05	-
	15	-	0.05	-	0	0.05	-	0.05	
VOH	5.0	4.95	AND POLICE	4.95	5.0	415 11	4.95	UU	Vdc
0	10	9.95	_	9.95	10	_	9.95	-	
	15	14.95	tiengo te	14.95	15	rid <u>4</u> 8 h	14.95	to MEC 14	T
VII		\$16Q00 B	BUT TRANS	en maka	xogratiens,	Jitt-Pit.	risoneq	ical, lad	Vdc
	5.0	6, 32, 4	1.5	santano.	2.25	1.5	ddage et	1.5	isola
	10	elbuger	3.0	yd-by	4.50	3.0	07f= 76	3.0	bre
	15	edoù-bal	4.0	uante a	6.75	4.0	may exity 1	4.0	12.10
VIH		enir side	iminud	riold al	tucini shi	ine etin	r metr res	dus (bari	circu
300	5.0	Action Services			2.75	uni-costs	3.5	nin-one	Vdc
1200		100 30000 100	- 10 - 10 - 10 - 10 - 10 - 10 - 10 - 10		The second second	-	1	and the second	d-Ra
971	15	A 100 LOG 25 LOG	AND THE PARTY OF T	100 July 100	Find Display of	bus maren		101 - OUEST 3	uror.
lou	10		relie be	11.0	1 1000000000000000000000000000000000000	SHY FAIR	11.0	97 2171	mAdo
1 OH	5.0	_30	Desp. 8	-24		mag call	-17	string stop	19.00
			Stoketh Au			circuits		ill ni luh	en si
CERM		1000000		1		qs tereig		lage soria	bns
								Ingresio	0 0
		-		-	-			estant only	mAdo
OL									
		100000		1	The second second	ignTIIA.		1017 sbo	0 0
Carrier 1	15	4.2		3.4	8.8	- 50	2.4	Star 2 oth	3.8
ІОН		Indi daol	Charle to	notal no	tel Blade -		annisten.		mAdo
			-	1		100000		No. America	
		100000000000000000000000000000000000000				GBA 4		O SHIM	10
		March 1975 - 1975 (MICH.)	Be App	THE RESERVED	OF A STREET, SELLING	in Thugs	ALL CHARLES IN	pribeeo	3 0
	15	-3.6	-	-3.0	-8.8	-	-2.4	ock frau	0
IOL	5.0	0.52	A Sinn	0.44	0.88	9157.7593	0.36	of Trees	mAdo
	10	1.3	-	1.1	2.25	_	0.9	= -	2 0
	15	3.6	TOSICIO	3.0	8.8	mrt Aut	2.4	Minto 111	-
lin	15	-	± 0.1	-	±0.00001	±0.1	-	±1.0	μAdo
lin	15	-	± 0.3	Day	±0.00001	± 0.3	1971_9993	±1.0	μAdo
	-	WOD-WO	a migga ja	80.LJ1	5.0	7.5	gnight	10 12000	DF
-111		eqmaT t	the Rapa	de Over	MTL LOS	OF Twee	Bood JT		25
lan	5.0	-	5.0	_	0.010	5.0	-	150	μAdo
100		_	1000000	-			-		
1 11		_	1 2 2	_			_		
1									μAdo
1DD				- 18	A COLUMN TO SECURE	CARL DE COR	10 A 2 S S	WILL EVENT A	μΑσο
			100000000000000000000000000000000000000	Topics			griftel		-
	-	217	200					1000	YOUR
I IT		3000							μAdd
1		Din A O		10					20100
				T = (1:	3.7 µA/kHz) 1 + 1DD			TRETTLE
	20	125	or 66-	AT		AL Device CP Device	- sgoott s	nutsiegmi	off gnite
ITL	15	-081	± 0.1	Total T	±0.00001	± 0.1	Tigns	±3.0	μAdd
ITL	15	-	±1.0		±0.00001	±1.0	-	± 7.5	μAdd
	VIH IOH IOL IOH IOL IOH IT ITL	15 VIL 5.0 10 15 10 10	15	15	15	15	VIL 5.0 - 14.95 15 -	V _{IL} 15	VIL 5.0 - 14.95 - 14.95 15 - 14.95 - VIL 5.0 - 1.5 - 2.25 1.5 - 1.5

*Tlow = -55°C for AL Device, -40°C for CL/CP Device.

Thigh = +125°C for AL Device, +85°C for CL/CP Device.

#Noise immunity specified for worst-case input combination.

Noise Margin for both "1" and "0" level = 1.0 Vdc min @ VDD = 5.0 Vdc

2.0 Vdc min @ VDD = 10 Vdc

2.5 Vdc min @ VDD = 15 Vdc

†To calculate total supply current at loads other than 50 pF:

IT(CL) = IT(50 pF) + 4|x 10⁻³ (CL -50) VDDf

where: IT is in µA (per package), CL in pF, VDD in Vdc, and f in kHz is input frequency.

*The formulas given are for the typical characteristics only at 25°C.

3-270

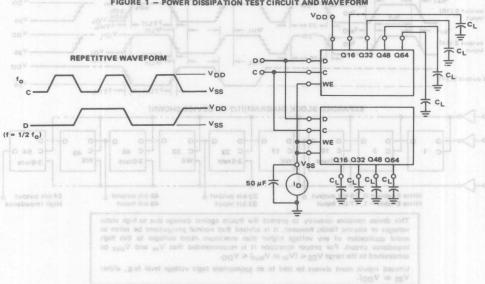
SWITCHING C	CHARACTERISTICS*	(C. = 50 of T. = 250C)

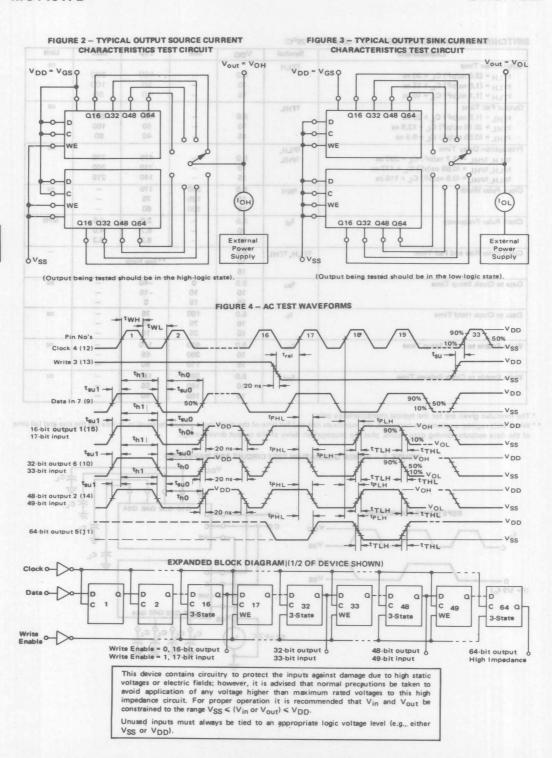
Characteristic	Symbol	VDD	Min	Тур	Max	Unit
Output Rise Time	†TLH	Veut + You				ns
t _{TLH} = (3.0 ns/pF) C _L + 30 ns	4 . 00 a	5.0	-	100	200	
tTLH = (1.5 ns/pF) CL + 15 ns		10	F	50	100	
tTLH = (1.1 ns/pF) CL + 10 ns		15	- 1	40	80	
Output Fall Time	tTHL		11111			ns
tTHL = (1.5 ns/pF) CL + 25 ns	-	5.0	- 1	100	200	
t _{THL} = (0.75 ns/pF) C _L + 12.5 ns		10	- 1	50	100	
t _{THL} = (0.55 ns/pF) C _L + 9.5 ns	10-9	15	60	40	80	
Propagation Delay Time	tPLH,		6 6		- 8/	ns
tpLH, tpHL = (1.7 ns/pF) CL + 390 ns	tPHL	5.0	-	475	770	
tpLH, tpHL = (0.66 ns/pF) CL + 177 ns		10		210	300	
tpLH, tpHL = (0.5 ns/pF) CL + 115 ns	-0-4	15	9 - 9	140	215	
Clock Pulse Width	twH	5.0	330	170	-	ns
		10	125	75	-	
		15	100	60	- 3	
Clock Pulse Frequency	fcl	5.0		3.0	1.5	MHz
		10	- 1	6.7	4.0	
lentification of the second		15/3	-	8.3	5.3	
Clock Pulse Rise and Fall Time	tTLH, tTHL	5.0				-
	Tann T	10	-	** See Note	-	
totara seases should be in the low-land state!	ch.	15	and the state of the state of	A		
Data to Clock Setup Time	t _{su}	5.0	0	-40		ns
		10	10	-15	-	
216903	SCREET SAVE	15	15	0	-	
Data to Clock Hold Time	th	5.0	150	75	-	ns
		10	75	25	-	
18 (18 MIN 13 CANA	181 /0	15	35	10	- 2015.6	
Write Enable to Clock Setup Time	t _{su}	5.0	400	170	-121124	ns
		10	200	65	-	
	1	15	110	50	= (E/1) E	colong.
Write Enable to Clock Release Time	t _{rel}	5.0	380	160	-	ns
		10	180	55	ter-Tust	
	-	15	100	40	100	

* The formulae given are for the typical characteristics only.

* * When shift register sections are cascaded, the maximum rise and fall time of the clock input should be equal to or less tha the rise and fall time of the data outputs, driving data inputs, plus the propagation delay of the output driving stage.

FIGURE 1 - POWER DISSIPATION TEST CIRCUIT AND WAVEFORM







DUAL UP COUNTERS

The MC14518B dual BCD counter and the MC14520B dual binary counter are constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. Each consists of two identical, independent, internally synchronous 4-stage counters. The counter stages are type D flip-flops, with interchangeable Clock and Enable lines for incrementing on either the positive-going or negative-going transition as required when cascading multiple stages. Each counter can be cleared by applying a high level on the Reset line. In addition, the MC14518B will count out of all undefined states within two clock periods. These complementary MOS up counters find primary use in multi-stage synchronous or ripple counting applications requiring low power dissipation and/or high noise immunity.

- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- Noise Immunity = 45% of VDD typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Low Input Capacitance = 5.0 pF typical
- Internally Synchronous for High Internal and External Speeds
- Logic Edge-Clocked Design Incremented on Positive Transition of Clock or Negative Transition on Enable
- 6.0 MHz Counting Rate
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range

MAXIMUM RATINGS (Voltages referenced to Vss.)

1 000 1 1 04 1 040	00		
about one Rating oc 300	Symbol	Value	Unit
DC Supply Voltage _ 010	V _{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	Vin	-0.5 to V _{DD} + 0.5	Vdc
DC Current Drain per Pin	3.01 × 1)	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	TA	-55 to +125 -40 to +85	°C
Storage Temperature Range	T _{stg}	-65 to +150	°C

TRUTH TABLE

CLOCK	ENABLE	RESET	ACTION
_	1	0	Increment Counter
0	7	0	Increment Counter
~	X	0	No Change
×	5	0	No Change
5	0	0	No Change
1	~	0	No Change
×	×	1	Q0 thru Q3 = 0

X = Don't Care

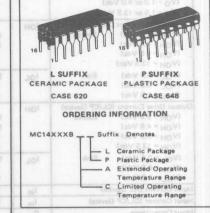
MC14518B MC14520B

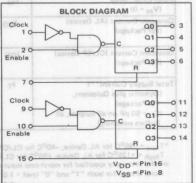
HUTASTER MICTARDE

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

DUAL BCD UP COUNTER (MC14518B) DUAL BINARY UP COUNTER (MC14520B)

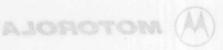




This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields: however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{OUt}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD).

min @ Vgg = 5.0 Vdc



ELECTRICAL CHARACTERISTICS

		VDD	Tio	w*		25°C	2	Thi		
Characteristic	Symbol	Vdc	Min	Max	Min	Тур	Max	Min	Max	Unit
Output Voltage "0" Level	VOL	5.0	-	0.05	-	0	0.05	-	0.05	Vdc
Vin = VDD or 0	- 00	10	-	0.05	-	0	0.05	-	0.05	
" CHINE HICE		15	-	0.05	-	0	0.05	_	0.05	
"1" Level	VOH	5.0	4.95	-	4.95	5.0	U JAU	4.95	_	Vdc
Vin = 0 or VDD	*OH	10	9.95		9.95	10		9.95		Vac
VIN OCI VDD		15	14.95	1014520	14.95	15	at BCD	14.95	to MC14	1
Input Voltage# "0" Level		10	14.55	Ditto terr	14.00	010 1010	D92012121	14.30	102111UUS	Vdc
A SAME OF WELL OF CHILDREN	VIL		and own	more ni	followner	plants o	1.5	o abom	1.5	Vdc
(V _O = 4.5 or 0.5 Vdc)	10	5.0		1.5		2.25	3.0	enobi os	3.0	2000
(v0 - 9.0 or 1.0 vdc)		10	2000000	3.0	17 (Lea	4.50		o edT		inch.
(V _O = 13.5 or 1.5 Vdc)		15	10701-0710	4.0	15 14 151	6.75	4.0	10 to 1	4.0	10000
"1" Level	VIH		10. 79/17/1	un dun	norremen	101 55011		009 200		Deus.
(V _O = 0.5 or 4.5 Vdc)		5.0	3.5	rive -beni	3.5	2.75	nieg-ewi	3.5	fulo6-an	Vdc
(V _O = 1.0 or 9.0 Vdc)		10	7.0	riggs yo	7.0	5.50	ou e o rio	7.0	o si q itiu	TING OF
(V _O = 1.5 or 13.5 Vdc)		15	11.0	oo Hisy E	11.0	8.25	ribbo nt	11.0	Red no	laval
Output Drive Current (AL Device)	ІОН		atnemo	mnen en	HT abo	tsa xbolo	thin two	xy 091510	beniteb	mAdo
(VOH = 2.5 Vdc) Source	011	5.0	-3.0	-	-2.4	-4.2	mer-mark	-1.7	tues- cau	SOM
(VOH = 4.6 Vdc)	PR 1	5.0	-0.64	The state of	-0.51	-0.88	er moin	-0.36	din-m	rippie
(VOH = 9.5 Vdc)	Har	10	-1.6	nedissin	-1.3	-2.25	D1 SHOW	-0.9	emi Selec	nioin
(V _{OH} = 13.5 Vdc)		15	-4.2	_	-3.4	-8.8	_	-2.4	HIN SHOE	ingus.
	1	5.0	0.64		0.51	0.88		0.36		mAdo
. OL	IOL			5 Vdc	THE THREE PLANS	Mark Company of the C	5.0 nA/	E 223 PLT 11	descent (mAdd
(V _{OL} = 0.5 Vdc)	1	10	1.6		1.3	2.25	V to atta	0.9	ise Irimi	di 0
(V _{OL} = 1.5 Vdc)		15	4.2	-	3.4	8.8	A 70.000	2.4		
Output Drive Current (CL/CP Device)	!он					031	Ignt HA	SO MOLTOS		mAdd
(VOH = 2.5 Vdc) Source		5.0	-2.5	-	-2.1	-4.2	0.8-90	-1.7	toV-yigg	6 3
(VOH = 4.6 Vdc)		5.0	-0.52	-	-0.44	-0.88	1 T- 000	-0.36	**************************************	110
(V _{OH} = 9.5 Vdc)	META	10	-1.3	-	-1.1	-2.25	-	-0.9	-	
(V _{OH} = 13.5 Vdc)		15	-3.6	leanni	-3.0	-8.8	103 200	-2.4	S Aspenso	101 0
(VOL = 0.4 Vdc) Sink	IOL	5.0	0.52	ovisioo ⁰	0.44	0.88	предел	0.36	gic Edge	mAdo
(VOL = 0.5 Vdc)	.OL	10	1.3	_	1.1	2.25	rises T	0.9	to should	10
(VOI = 1.5 Vdc)		15	3.6		3.0	8.8		2.4	0.4000	10 0
nout Current (AL Device)		15	-	±0.1	0.0	±0.00001	±0.1	1 (54.7)	110	иAdd
	lin			1.62543 0	wo.T. I'l		THE RESIDENCE	Dateton	±1.0	
nput Current (CL/CP Device)	lin	15	nomaT.	± 0.3	tavT/zb	±0.00001	±0.3	mod JT	±1.0	μAdd
Input Capacitance (V _{in} = 0)	Cin	-	-			5.0	7.5	-	igne f i er	pF
Quiescent Current (AL Device)	IDD	5.0	-	5.0	-	0.005	5.0	-	150	μAdo
(Per Package)	טטי	10	-	10	-	0.010	10	-	300	1
-10		15	-	20	- 12	0.015	20	10 VI 38	600	WUND
2 10 100		_	-	-	-					1
Quiescent Current (CL/CP Device)	IDD	5.0	- 1	20	louim v	0.005	20	Enter	150	μAdd
(Per Package)		10	-81+	40	BOY	0.010	40	-	300	Alddn
		15	18.00	80	1 - V	0.015	80	- 11	600	district i
Total Supply Current**†	IT	5.0	1		IT = (0).6 µA/kHz)	f + Ipp			μAdd
(Dynamic plus Quiescent,		10	-			.2 µA/kHz)				-
Per Package)	Chooks 9-d	15				.7 µA/kHz)				1
(CL = 50 pF on all outputs, all			-							neT en
buffers switching)	0.01	19	001	- 0) 00-	1005			all one	T STORE ST	

appropriate logic voltage level (e.g., eicher Vog

^{*}T_{IOW} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc

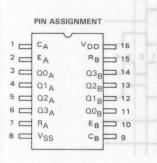
^{2.0} Vdc min @ V_{DD} = 10 Vdc 2.5 Vdc min @ V_{DD} = 15 Vdc

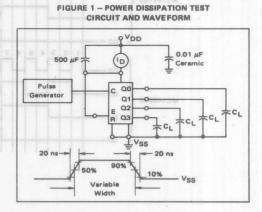
[†]To calculate total supply current at loads other than 50 pF: $\frac{1}{17}(C_L) = \frac{1}{17}(50 \text{ pF}) + 2\frac{1}{2} \times 10^{-3} (C_L - 50) \text{ V}_{DD}$ where: $\frac{1}{7} \text{ is in } \mu \text{A (per package)}, C_L \text{ in pF, V}_{DD} \text{ in Vdc, and f in kHz is input frequency.}$ "The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS* (CL = 50 pF, TA = 25°C)

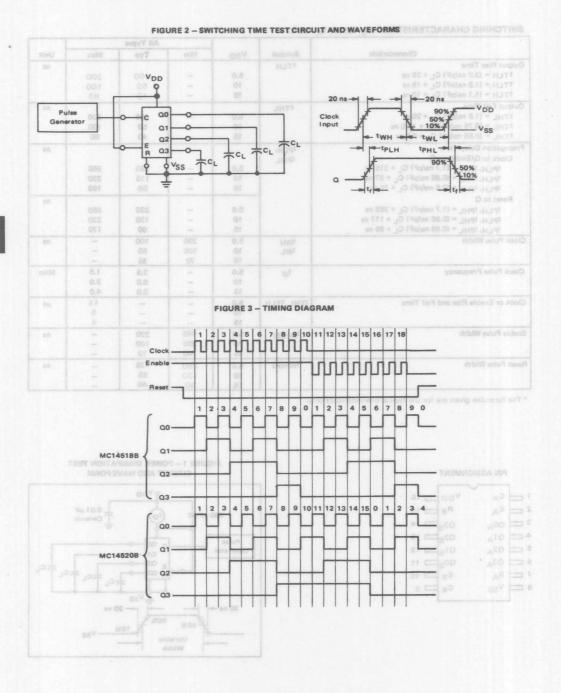
				All Types		
Characteristic	Symbol	VDD	Min	Тур	Max	Unit
Output Rise Time tTLH = (3.0 ns/pF) C _L + 30 ns tTLH = (1.5 ns/pF) C _L + 15 ns tTLH = (1.1 ns/pF) C _L + 10 ns	^t TLH	5.0 10 15	=	100 50 40	200 100 80	ns
Output Fall Time t_HL = (1.5 ns/pF) CL + 25 ns t_HL = (0.75 ns/pF) CL + 12,5 ns t_HL = (0.55 ns/pF) CL + 9.5 ns	tTHL	5.0 10 15	9 + 9	100 50 40	200 100 80	ns neces
Propagation Delay Time Clock to Q/Enable to Q tp_H, tpHL = (1.7 ns/pF) C _L + 215 ns tp_H, tpHL = (0.66 ns/pF) C _L + 97 ns tp_H, tpH_ = (0.5 ns/pF) C _L + 75 ns	tPLH, tPHL	5.0 10 15	- 18 ^V	280 115 80	560 230 160	ns
Reset to Q tp_H, tpHL = (1.7 ns/pF) C _L + 265 ns tp_H, tpHL = (0.66 ns/pF) C _L + 117 ns tp_H, tpHL = (0.66 ns/pF) C _L + 95 ns		5.0 10 15		330 130 90	650 230 170	ns
Clock Pulse Width	₩H ₩L	5.0 10 15	200 100 70	100 50 35	-	ns
Clock Pulse Frequency	fcl	5.0 10 15	-	2.5 6.0 8.0	1.5 3.0 4.0	МН
Clock or Enable Rise and Fall Time	THL, TLH	5,0 10 15	=		15 5 4	με
Enable Pulse Width	tWH(E)	5.0 10 15	440 200 140	220 100 70	Ξ	ns
Reset Pulse Width	tWH(R)	5.0 10 15	280 120 90	125 55 40	Ξ	ns

^{*} The formulae given are for the typical characteristics only.



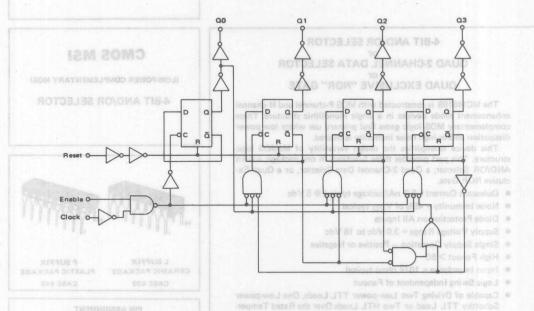




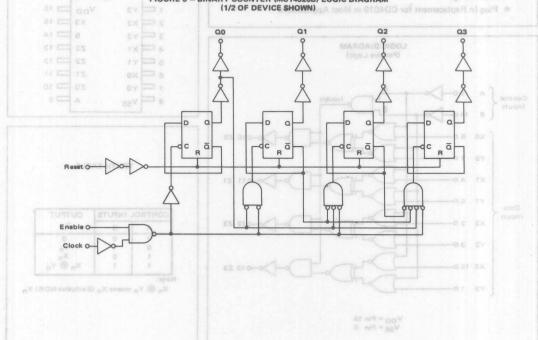


MOTOROLA

FIGURE 4 - DECADE COUNTER (MC14618B) LOGIC DIAGRAM (1/2 OF DEVICE SHOWN)







MC14519B

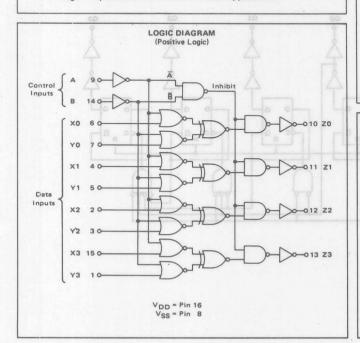
CIASISSEMCIASZUM

4-BIT AND/OR SELECTOR OR QUAD 2-CHANNEL DATA SELECTOR OR QUAD EXCLUSIVE "NOR" GATE

The MC14519B is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These complementary MOS logic gates find primary use where low power dissipation and/or high noise immunity is desired.

This device exemplifies the design versatility of McMOS logic structure. This part provides three functions in one package; a 4-Bit AND/OR Selector, a Quad 2-Channel Data Selector, or a Quad Exclusive NOR Gate.

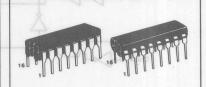
- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- Noise Immunity = 45% of VDD typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Single Supply Operation Positive or Negative
- High Fanout > 50
- Input Impedance = 1012 ohms typical
- Logic Swing Independent of Fanout
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range
- Plug-In Replacement for CD4019 in Most Applications



CMOS MSI

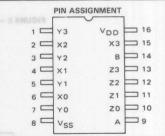
(LOW-POWER COMPLEMENTARY MOS)

4-BIT AND/OR SELECTOR



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648



TRUTH TABLE

CONTRO	INPUTS	OUTPUT
А	В	o ole Z _n
0	0	0
0	1	O WOYn
1	0	Xn
1	1	Xn @ Yn

X_n Y_n means X_n (Exclusive-NOR) Y_n

3

MAXIMUM RATINGS (Voltages referenced to VSS)

Rating	Symbol	Value	Unit	0
DC Supply Voltage	V _{DD}	-0.5 to +18	Vdc	emiT se
Input Voltage, All Inputs	Vin	-0.5 to V _{DD} + 0.5	Vdc	(Rg\an 0,8) - (Rg\an 8,1) -
DC Current Drain per Pin	1	10	mAdc	(Rglan (LT)
Operating Temperature Range – AL Device CL/CP Device	TA	-55 to +125 -40 to +85	°C	f Time
Storage Temperature Range	T _{stg}	-65 to +150	°C	Re\m 85.0) -

ELECTRICAL CHARACTERISTICS

800	200	-	VDD	Tio	w*		25°C		Thi	gh*	HTIGE
Characteristic	115	Symbol	Vdc	Min	Max	Min	Тур	Max	Min	Max	Unit
Output Voltage	"0" Level	VOL	5.0	-	0.05	-	0	0.05	-	0:05	Vdc
Vin - VDD or 0		. 00	10	-	0.05	no soltal	stos o do le	0.05	n are for	0.05	hot en
			15	-	0.05	-	0	0.05	-	0.05	
	"1" Level	VOH	5.0	4.95	_	4.95	5.0	_	4.95	_	Vdc
Vin = 0 or VDD			10	9.95	_	9.95	10	_	9.95		
	MACHEN	N CINA TIL	15	14.95	MISSIG I	14.95	15	r shup	14.95	-	
Input Voltage#	"0" Level	V _{IL}									Vdc
(Vo = 4.5 or 0.5 Vdc)			5.0	-	1.5	- oav	2.25	1.5	-	1.5	
(VO = 9.0 or 1.0 Vdc)			10	-	3.0	-00	4.50	3.0	- 1	3.0	
(VO = 13.5 or 1.5 Vdc)		- 1	15	-	4.0	-	6.75	4.0	-	4.0	
	"1" Level	VIH				-0 05	DOY AL	0-1		-	
$(V_0 = 0.5 \text{ or } 4.5 \text{ Vdc})$			5.0	3.5	万未	3.5	2.75	Ini*	3.5	9 _	Vdc
$(V_0 = 1.0 \text{ or } 9.0 \text{ Vdc})$			10	7.0	-1	7.0	5.50	-	7.0	- Gen	
(V _O = 1.5 or 13.5 Vdc)	20.02	20 05	15	11.0	- 1	11.0	8.25	1	11.0	-	
Output Drive Current (AL D	Device)	ІОН			-		10				mAdc
	Source	200%	5.0	-3.0	學事	-2.4	-4.2	4	-1.7	-	
(VOH = 4.6 Vdc)	/	201	5.0	-0.64	- 7	-0.51	-0.88	-	-0.36	-	
(VOH = 9.5 Vdc)	2	MULT	10	-1.6	- [-1.3	-2.25	7	-0.9	-	
(VOH = 13.5 Vdc)	atey Cycle	0.000	15	-4.2	型下	-3.4	-8.8	-11	-2.4	-	
(VOI = 0.4 Vdc)	Sink	IOL	5.0	0.64	_ =	0.51	0.88	-	0.36		mAdc
(V _{OL} = 0.5 Vdc)		-OL	10	1.6	- 1	1.3	2.25	-	0.9	-	
(V _{OL} = 1.5 Vdc)			15	4.2	迎赤	3.4	8.8	-	2.4	-	
Output Drive Current (CL/C	P Device)	ГОН			-		I				mAdc
	Source	'OH	5.0	-2.5	-	-2.1	-4.2	_	-1.7		1111144
(V _{OH} = 4.6 Vdc)	Source	200	5.0	-0.52	_ "	-0.44	-0.88	_	-0.36	_	
(V _{OH} = 9.5 Vdc)	200		10	-1.3	_	-1.1	-2.25	_	-0.9	_	
(V _{OH} = 13.5 Vdc)			15	-3.6	_	-3.0	-8.8	-	-2.4	-	
	Sink	la	5.0	0.52		0.44	0.88		0.36		mAdc
$(V_{OL} = 0.5 \text{ Vdc})$	-EMS	IOL	10	1.3	TRUIT	1.1	2.25	216	0.9	_	made
$(V_{OL} = 1.5 \text{ Vdc})$			15	3.6	_	3.0	8.8		2.4		1 5-5
Input Current (AL Device)		1.	15	-	± 0.1	-	±0.00001	±0.1	-	±1.0	μAdc
Input Current (CL/CP Device)	100	lin	15	-	±0.1	-	±0.00001	± 0.3	-	±1.0	μAdc
	ce)	lin		-	± 0.3	-			-		-
Input Capacitance		Cin	-	-	- (-	-	5.0	7.5	-	Putter	pF
(V _{in} = 0)					19		143	Aller		hotemann	
Quiescent Current (AL Devi	ice)	IDD	5.0	-	5.0	1-4	0.005	5.0	11	150	μAdc
(Per Package)		Tarrier .	10	- 1	10	=	0.010	10		300	
12	3606 -3	7 115	15	-	20		0.015	20	17 -	600	
Quiescent Current (CL/CP [Device)	IDD	5.0	- 300	20	102	0.005	20	11-	150	μAdc
(Per Package)	- marie	JH97	10	-	40	=	0.010	40	-	300	
No. of the last of		2777	15	-	80	7	0.015	80	11-	600	
Total Supply Current**†	W05 - K	IT	5.0			IT = (1	.2 µA/kHz	f + Ipp			μAdc
(Dynamic plus Quiescen	1001 - 1		10			IT = (2	2.4 µA/kHz) f + IDD			
Per Package)	400		15			IT = (3	1.6 µA/kHz) f + IDD			
(CL = 50 pF on all outpo	uts, all										
buffers switching)						4	9-				
Three-State Leakage Curren	t	ITL	15	-	± 0.1	-	±0.00001	± 0.1		±3.0	μAdc
(AL Device)											
Three-State Leakage Curren	t	ITL	15	-	±1.0	-	+0.00001	±1.0	-	± 7.5	μAdc
(CL/CP Device)		1.0							100		
- 0-			7.6								1

^{*}T_{IOW} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination. Noise Margin for both "1" and "0" level =

^{1.0} Vdc min @ V_{DD} = 5.0 Vdc 2.0 Vdc min @ V_{DD} = 10 Vdc 2.5 Vdc min @ V_{DD} = 15 Vdc

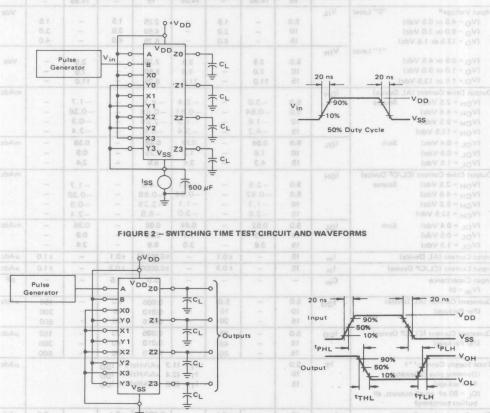
[†]To calculate total supply current at loads other than 50 pF: $\frac{1}{1}(C_L) = \frac{1}{1}(50 \text{ pF}) + 4 \times 10^{-3} (C_L - 50) \text{ V}_{DD} \text{f}$ where: $\frac{1}{1} \text{ is in } \mu \text{A} \text{ (per package), } C_L \text{ in pF, V}_{DD} \text{ in Vdc, }$ and f in kHz is input frequency.
*The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS* (CL = 50 pF, TA = 25°C)

Characteristic and V lode	Symbol	VDD	Min	Тур	Max	Unit
Output Rise Time 25V 81+ 018.0- 00	V TLH		egar c	C Supply Ve	3 1	ns
.tTLH = (3.0 ns/pF) CL + 30 ns	7	5.0	Artiford it &	100	200	
tTLH = (1.5 ns/pF) CL + 15 ns		10	-	50	100	
tTLH = (1.1 ns/pF) CL + 10 ns	-	15	min ted was	40	80	
Output Fall Time	tTHL	ALLER GEN PE	The same of	has furnaced		ns
THL = (1.5 ns/pr) CL + 25 ns	-	5.0		100	200	
t _{THL} = (0.75 ns/pF) C _L + 12.5 ns		10	egnedi dange	50	100	
t _{THL} = (0.55 ns/pF) C _L + 9.5 ns		15	- 1	40	80	
Propagation Delay Time	tPLH,		83	FTEIRSTO.	ARAHO JA	ns
tplH, tpHL = (1.7 ns/pF) CL + 165 hs	tPHL T	5.0	-	250	500	
tPLH, tPHL = (0.66 ns/pF) CL + 82	rubl t	10		115	225	
tpLH, tpHL = (0.5 ns/pF) CL + 65 ns		15	1 manufacture	90	165	

^{*}The formulae given are for the typical characteristics only.

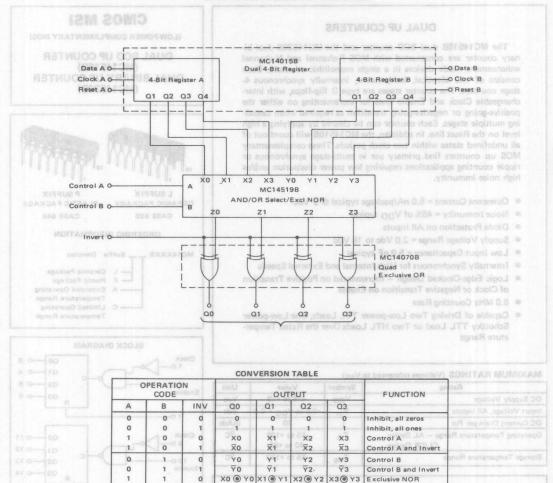
FIGURE 1 - DYNAMIC POWER DISSIPATION TEST CIRCUIT AND WAVEFORM





TYPICAL CIRCUIT APPLICATIONS

DATA REGISTER SELECTION COMPARISON



This device contains circuitry to protect the
ages or electric fields: however, it is advised
that normal precautions be taken to avoid
mum rated voltages to this high impedance
VSS < (Vin or Vour) < VDD-

		-
Increment Counter		
		×
G = SQ unitr GD		×

sum 1 years -

X0 + Y0 X1+ Y1 X2+ Y2 X3+ Y3 Exclusive OR



MC14520B

FOR COMPLETE DATA SEE MC14518B

DUAL UP COUNTERS

The MC14518B dual BCD counter and the MC14520B dual binary counter are constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. Each consists of two identical, independent, internally synchronous 4-stage counters. The counter stages are type D flip-flops, with interchangeable Clock and Enable lines for incrementing on either the positive-going or negative-going transition as required when cascading multiple stages. Each counter can be cleared by applying a high level on the Reset line. In addition, the MC14518B will count out of all undefined states within two clock periods. These complementary MOS up counters find primary use in multi-stage synchronous or ripple counting applications requiring low power dissipation and/or high noise immunity.

- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- Noise Immunity = 45% of Vnn typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Low Input Capacitance = 5.0 pF typical
- Internally Synchronous for High Internal and External Speeds
- Logic Edge-Clocked Design Incremented on Positive Transition of Clock or Negative Transition on Enable
- 6.0 MHz Counting Rate
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range

MAXIMUM RATINGS (Voltages referenced to Voc.)

Rating	Symbol	Value	Unit
DC Supply Voltage	V _{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	Vin	-0.5 to V _{DD} + 0.5	Vdc
DC Current Drain per Pin	1	10	mAdo
Operating Temperature Range — AL Device CL/CP Device	TA	-55 to +125 -40 to +85	°C
Storage Temperature Range	T _{stg}	-65 to +150	°C

TRUTH TABLE

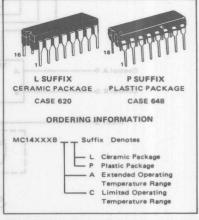
CLOCK	ENABLE	RESET	ACTION
5	- 1	0	Increment Counter
. 0	7	0	Increment Counter
7	×	0	No Change
×	5	0	No Change
5	0	0	No Change
1	~	0	No Change
×	×	1	Q0 thru Q3 = 0

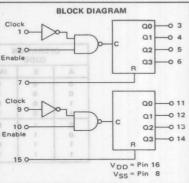
X = Don't Care

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

DUAL BCD UP COUNTER (MC14518B) DUAL BINARY UP COUNTER (MC14520B)





This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields: however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in} \text{ or } v_{out}) \leq V_{DD}$. Unused inputs must always be tied to an

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD).



MC14521B

24-STAGE FREQUENCY DIVIDER

The MC14521B consists of a chain of 24 flip-flops with an input circuit that allows three modes of operation. The input will function as a crystal oscillator, an RC oscillator, or as an input buffer for an external oscillator. Each flip-flop divides the frequency of the previous flip-flop by two, consequently this part will count up to 2²⁴ = 16,777,216. The count advances on the negative going edge of the clock. The outputs of the last seven-stages are available for added flexibility.

- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- f(max) = 9.0 MHz typical @ VDD = 10V
- All Stages are Resettable
- Reset Disables the RC Oscillator for Low Standby Power Drain
- RC and Crystal Oscillator Outputs Are Capable of Driving External Loads
- Test Mode to Reduce Test Time
- VDD' and VSS' Pins Brought Out on Crystal Oscillator Inverter to Allow the Connection of External Resistors for Low-Power Operation
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range.

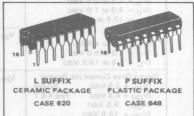
MAXIMUM RATINGS (Voltages referenced to VSS)

Rating	Symbol	Value	Unit
DC Supply Voltage	V _{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	Vin	-0.5 to V _{DD} + 0.5	Vdc
DC Current Drain per Pin	180 194.0	10 58.0	mAdc
Operating Temperature Range — AL Device CL/CP Device	TA	-55 to +125 -40 to +85	°C
Storage Temperature Range	T _{stg}	-65 to +150	°C

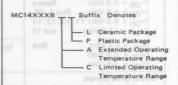
CMOS MSI

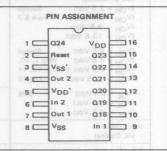
(LOW-POWER COMPLEMENTARY MOS)

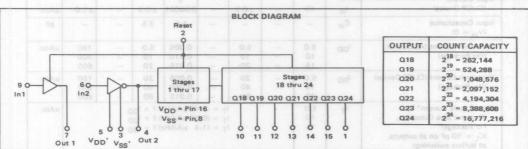
24-STAGE FREQUENCY DIVIDER



ORDERING INFORMATION







This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leqslant (V_{in} \text{ or } V_{out}) \leqslant V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

MOTOROLA

ELECTRICAL CHARACTERISTICS

		V _{DD}	T _{lo}	w		25°C		h	igh *		
Characteristic	Symbol	Vdc	Min	Max	Min	Тур	Max	Min	Max	Unit	
Output Voltage "0" Level	VOL	5.0	-	0.05	_	0	0.05	-	0.05	Vdc	
$V_{in} = V_{DD}$ or O		10 15	_	0.05	VIELV	0	0.05	- BITATE	0.05		
"1" Level	VOH	5.0	4.95	-	4.95	5.0	_	4.95	-	Vdc	
$V_{in} = 0 \text{ or } V_{DD}$	OII	10 15	9.95 14.95	iw aqott	9.95 14.95	10 15	s 10 es	9.95 14.95	MC1#52	The	
THE RESERVE OF THE PROPERTY OF		110	EGREAT RE	er Jugin	903 .00	13 E 7 SU(U.)	0.200001	os untel	Communication		1
Input Voltage # "O" Level (VO = 4.5 or 0.5 Vdc)	VIL	5.0	affer for	1.5	ITE 25 7	2.25	1.5	ne con or Faci	1.5	Vdc 2	
$(V_0 = 9.0 \text{ or } 1.0 \text{ Vdc})$		10	to you	3.0	ed the	4.50	3.0		3.0	anterxe	
$(V_0 = 13.5 \text{ or } 1.5 \text{ Vdc})$	- 11	15	qu Thuo	4.0	this par	6.75	4.0	rest yd c	4.0	previous	
Sixter Telescopies Proposition (Sept. 1997)	9	to	spire pri	attivo ge	en edt	to risher	rbs inus	b. The o	777770	-	-
"1" Level	VIH	bs	a for add	Idaliava	are topu	13-USABS		to stugti	k. Fire of	Vdc	
$(V_0 = 0.5 \text{ or } 4.5 \text{ Vdc})$	8 11	5.0	3.5	-	3.5	2.75	-	3.5	- 49	flexibili	
$(V_0 = 1.0 \text{ or } 9.0 \text{ Vdc})$	Doc -	10	7.0	-	7.0	5.50		7.0	-	CONT. IN	
$(V_0 = 1.5 \text{ or } 13.5 \text{ Vdc})$		15	11.0	56 ¥dc	11.0	8.25	gNAm O.	11.0	scent_Cur	e Quis	
Output Drive Current (AL Device)	Іон				V	D1 = GG		GA1 ZHIN	B.S (N	mAdc	
(V _{OH} = 2.5 Vdc) Source	190	5.0	-1.2	-	-1.0	-1.7	- 68	-0.7	ME-10051	BIIA .	
(V _{OH} = 4.6 Vdc) Pins 4 & 7		5.0	-0.25	g vebri	-0.2	-0.36	History of	-0.14	eld <u>a</u> ziG 1	page R asa	1
(V _{OH} = 9.5 Vdc)		10	-0.62	A Annui	-0.5	-0.9	unneo .	-0.35			
$(V_{OH} = 13.5 \text{ Vdc})$		15	-1.8	of Driv	-1.5	-3.5	unG-101	041210 lo	nd Cepst	W RC	
(V _{OH} = 2.5 Vdc) Source		5.0	-3.0		-2.4	-4.2	_	-1.7	mai Load	mAdc	1
(V _{OH} = 4.6 Vdc) Pins 1, 10,	NC.	5.0	-0.64	_	-0.51	-0.88	niT-rap	-0.36	nt-should	Jast 0	
(V _{OH} = 9.5 Vdc) 11, 12, 13, 14	349	10	-1.6	_	-1.3	-2.25	-	-0.9			
(V _{OH} = 13.5 Vdc) and 15	11	15	-4.2	rsiti <u>n</u> eO	-3.4	-8.8	Mguora	-2.4	V bns	adA a	
0.1		101	rog wo.	107 011	Seizo SI	CATRING.	To noi	Corined	Aria woll	0.01	1
$(V_{OL} = 0.4 \text{ Vdc})$ Sink	OL	5.0	0.64	-	0.51	0.88	_	0.36	Thoise	mAdc	
$(V_{OL} = 0.5 \text{ Vdc})$		10	1.6	_	1.3	2.25	V 0.E =	0.9	outleV vites	o Supp	
$(V_{OL} = 1.5 \text{ Vdc})$		15	4.2		3.4	8.8	-	2.4	_		
Output Drive Current		181	Loss-box	enc) ,si	leoJ J1	1 198700	Will D	W. I. BILLIAN	TT - 150	District P	1
(CL/CP Device)	10Н	-51	I Femipa	eseri on	s Oyer t	Tt Load		to bebut	TT VXII	mAdc	
(V _{OH} = 2.5 Vdc) Source		5.0	-1.0	-	-0.8	-1.7	-	-0.6	agner	enut	
(V _{OH} = 4.6 Vdc) Pins 4 & 7	1.7	5.0	-0.2	-	-0.16	-0.36	-	-0.12	-		
$(V_{OH} = 9.5 \text{ Vdc})$		10	-0.5	-	-0.4	-0.9	-	-0.3	-		
$(V_{OH} = 13.5 \text{ Vdc})$		15	-1.4	-	-1.2	-3.5	-	-1.0	-		
(V _{OH} = 2.5 Vdc) Source		5.0	-2.5	_	-2.1	-4.2	obenatos	-1.7	DEMAIN A	mAdc	Kå
(V _{OH} = 4.6 Vdc) Pins 1, 10,	1.1	5.0	-0.52	day_	-0.44	-0.88	_	-0.36	2200		
(V _{OH} = 9.5 Vdc) 11, 12, 13, 14	117	10	-1.3	nr 8-6	-1.1	-2.25	-	-0.9	- 1904	doV vies	12
(V _{OH} = 13.5 Vdc) and 15	1 1	15	-3.6	1.5 to V.	-3.0	-8.8	-	-2.4	rtonal fil	100 x 1/////	711
(V _{OL} = 0.4 Vdc) Sink	la.	5.0	0.52	14 -	0.44	0.88		0.36	n ser Pin	mAdc	1
$(V_{OL} = 0.4 \text{ Vdc})$ Sink $(V_{OL} = 0.5 \text{ Vdc})$	OL	10	1.3	100	1.1	2.25		0.36			10
$(V_{OL} = 1.5 \text{ Vdc})$	71364	15	3.6	or <u>18</u> -	3.0	8.8	Davice	2.4	aff gaussia	ama Tanin	ine
			657	of UR-	1		Device	4000			-
Input Current (AL Device)		15	0811	± 0.1	grz T	± 0.00001	±0.1	. 9	± 1.0	sameT o	60
(AL Device)	lin	15		±0.1		0.00001	±0.1		11.0	μAdc	
Input Current	-					±					
(CL/CP Device)	lin	15		±0.3	-	0.00001	±0.3	-	±1.0	μAdc	
Input Capacitance	C _{in}	_	-	-		5.0	7.5	_	_	pF	1
(V _{in} = 0)	-in					5	7.0			P.	
	1			5.0		0.005	5.0		150		-
Quiescent Current (AL Device)	DD	5.0	-	5.0	-	0.005	5.0	-	150	μAdc	
(Per Package)		10		10	_	0.010	10	_	300	The Prince	
210 22 010		15	-	20		0.015	20	-	600		-
Quiescent Current (CL/CP Device)	IDD	5.0	918 -	20		0.005	20	-1	150	μAdc	00
(Per Package)		10	NU ST	40	179	0.010	40	7	300	V	110
022 2" - 4,194,30	22 024	15	10 ax 0	80		0.015	80	1 +	600		1
Total Supply Current * * †	IT	5.0			$I_{T} = (0.$	42 μA/kH	z) f + 1 _D	D		μAdc	
		10			$I_{-} = 10$	85 μA/kH	z) f + lo	0			1
(Dynamic plus Quiescent,	1 3				100	or be die.		U			
(Dynamic plus Quiescent, Per Package) (C ₁ = 50 pF on all outputs,	6 6	15	1 ST		$I_{T} = (1.$	4 μA/kH	z) f + 10	Doo			

^{*} T_{low} = -55°C for AL Device, -40°C for CL/CP Device.

Thigh = +125°C for AL Device, +85°C for CL/CP Device.

Noise immunity specified for worst-case input combination.

Noise Margin for both "1" and "0" level =

1.0 Vdc min @ V_{DD} = 5.0 Vdc

2.0 Vdc min @ V_{DD} = 10 Vdc

2.5 Vdc min @ V_{DD} = 15 Vdc

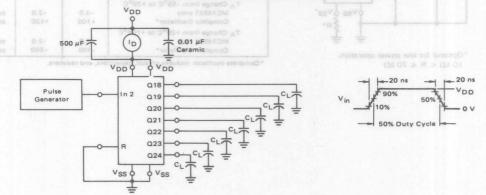
^{0°}C for CL/CP Device. 7 To calculate total supply current at loads other than 50 pF: I_T (C_L) = I_T (50 pf) + 3×10^{-3} (C_L-50) V_{DD}f. where: I_T is in μ A (Per Package) C_L in pF, V_{DD} in Vdc and f in kHz is input frequency. * The formulae given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS*	$(C_1 = 50 pF')$	$\Delta = 25$ °C)

	Characteristic		Symbol	V _{DD} Vdc	Min	Тур	Max	Unit
Output Rise Time (C			^t TLH	5.0	,00	100	200	ns
t _{TLH} = (1.5 ns/pF t _{TLH} = (1.1 ns/pF		Jin 2	F,5-	10 15	-0	50 40	100	Putra
Output Fall Time (Co		101/108	^t THL			iso l		ns
tTHL = (1.5 ns/pF			1 4	5.0	- 0	100	200	
tTHL = (0.75 ns/p			- 1	10	- 0	50	110	
tTHL = (0.55 ns/p		Fig. 1	-	15		40	80	
Propagation Delay Ti Clock to Q18	me		tPLH,		×12-0-	80		μs
tPHL tPLH = (1.7	7 ns/pF) C1 + 4	415 ns	7112	5.0	中本的"	4.5	9.0	
tpHL, tpLH = (0.6	66 ns/pF) CL +	1667 ns		10	T , ss	1.7	3.5	
tpHL, tpLH = (0.5	5 ns/pF) CL + 1:	275 ns		15	-	1.3	2.7	
Clock to Q24								μs
tPHL tPLH = (1.7	7 ns/pF) CL + 5	915 ns		5.0	-	6.0	12	
tPHL, tPLH = (0.6				10	-	2.2	4.5	
tpHL, tpHL = (0.5	5 ns/pF) CL + 10	675 ns		15	-	1.7	3.5	
Propagation Delay Ti	me		tPHL					ns
tpHL = (1.7 ns/pF	Cı + 1215 ns			5.0		1300	2600	1 4 1 1 1
tpHL = (0.66 ns/p				10		500	1000	No. 578 to
tpHL = (0.5 ns/pF				15	_	375	750	1.
Clock Pulse Width		a comment a nation	tWH(cl)	5.0	385	140	_	ns
JAIS			-will(CI)	10		TA55 (580 .	ATEKRO -	1
				15	120	40	-	
Clock Pulse Frequenc	y Maria Good	A CONTRACTOR OF THE CONTRACTOR	fcl	5.0	-	3.5	2.0	MHz
TIMU TIUDAID	TIUDRID		2	10	- 00	9.0	5.0	
			nead Characteria	15		12	6.5	Day 1500
Clock Rise and Fall T		yantau	tTLH.	5.0	-185	_	15	μs
6.2 8.02			THL	10	'any on	wh-	5	
			wrost Rusinter	15	50. 10	M 8	4	
Reset Pulse Width	82		tWH(R)	5.0	1400	700	-	ns
20 PF	20		70	10	600	300	-	
				15	450	225	-	1

^{*}The formulae given are for the typical characteristics only. To younger 1

FIGURE 1 - POWER DISSIPATION TEST CIRCUIT AND WAVEFORM







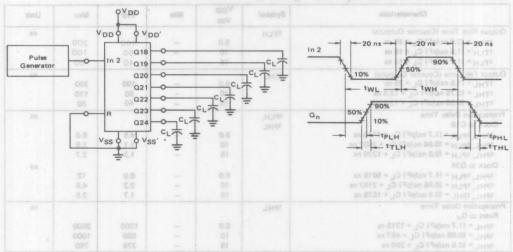


FIGURE 3 - CRYSTAL OSCILLATOR CIRCUIT

· VDD ONDD VDD 18 M Out 1 Out 2 -0-018 0 019 -0 99 In 2 020 021 022-0 023-0 市cs 市cr R 024 0 14 TUS ovss ovss'

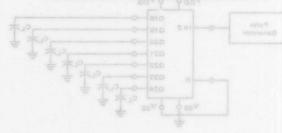
*Optional for low power operation. 10 k Ω \leq R \leq 70 k Ω

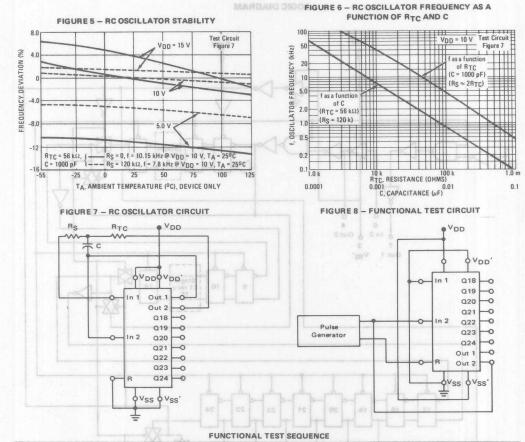
FIGURE 4 – TYPICAL DATA FOR CRYSTAL OSCILLATOR CIRCUIT

CHARACTERISTIC	500 kHz CIRCUIT	50 kHz CIRCUIT	UNIT
Crystal Characteristics			
Resonant Frequency	500	50	kHz
Equivalent Resistance, RS	1.0	6.2	kΩ
External Resistor/Capacitor Values			
Ro	47	750	kΩ
C _T	82	82	pF
CS	20	20	pF
Frequency Stability Frequency Change as a Function of V _{DD} (T _A = 25°C) V _{DD} Change from 5.0 V to 10 V V _{DD} Change from 10 V to 15 V	+6.0 +2.0	+2.0 +2.0	ppm ppm
Frequency Change as a Function of Temperature (V _{DD} = 10 V) T _A Change from -55°C to +25°C MC14521 only Complete Oscillator*	-4.0 +100	-2.0 +120	ppm
TA Change from +25°C to +125°C MC14521 only	-2.0	-2.0	ppm
Complete Oscillator®	-160	-560	ppm

*Complete oscillator includes crystal, capacitors, and resistors.

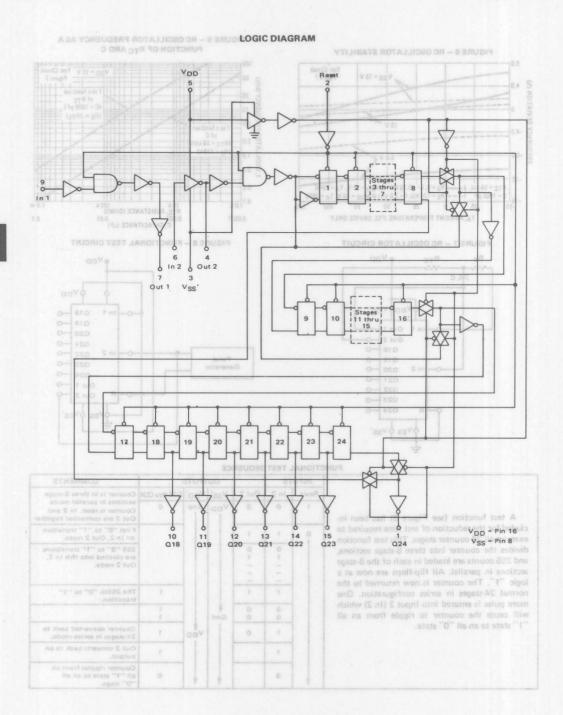






	INPL	ITS		ou	TPUTS	3	COMMENTS
	Reset	Reset In 2		Vss'	VDD'	Q18 thru Q24	Counter is in three 8-stage
A test function (see Figure 8) has been included for the reduction of test time required to exercise all 24 counter stages. This test function divides the counter into three 8-stage sections, and 255 counts are loaded in each of the 8-stage sections in parallel. All flip-flops are now at a logic "1". The counter is now returned to the	1	0	0	VDD	Gnd	0	sections in parallel mode Counter is reset. In 2 and Out 2 are connected togethe
	0	1	1		0	10	First "0" to "1" transition on In 2, Out 2 node.
		0 1 - -	0 1 - -		15101	arp	255 "0" to "1" transitions are clocked into this In 2, Out 2 node.
normal 24-stages in series configuration. One more pulse is entered into Input 2 (In 2) which		1	.1			1	The 255th "0" to "1" transition.
will cause the counter to ripple from an all		0	0	Gnd		1 1	
"1" state to an all "0" state.		1	0		V _{DD}	1	Counter converted back to 24-stages in series mode.
		1				1	Out 2 converts back to an output.
		0			-	0	Counter ripples from an all "1" state to an all "0" stage.







MC14522B MC14526B

NC145228 • MC14526B

PROGRAMMABLE DIVIDE-BY-N 4-BIT COUNTERS

The MC14522B BCD counter and the MC14526B binary counter are constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure.

These devices are programmable, cascadable down counters with a decoded "0" state output for divide-by-N applications. In single stage applications the "0" output is applied to the Preset Enable input. The Cascade Feedback input allows cascade divide-by-N operation with no additional gates required. The Clock Inhibit input allows disabling of the pulse counting function.

These complementary MOS counters can be used in frequency synthesizers, phase-locked loops, and other frequency division applications requiring low power dissipation and/or high noise immunity.

- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Internally Synchronous for High Internal and External Speeds.
- Logic Edge-Clocked Design Incremented on Positive Transition of Clock or Negative Transition of Clock Inhibit
- 5.0 MHz Counting Rate
- Asynchronous Preset Enable
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range

MAXIMUM RATINGS (Voltages referenced to VSS)

Rating 25	0.6	Symbol	Value	Unit
DC Supply Voltage		VDD	-0.5 to +18	Vdc
Input Voltage, All Inputs	800.	V _{in}	-0.5 to V _{DD} + 0.5	Vdc
DC Current Drain per Pin	010.	1	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	000	TA	-55 to +125 -40 to +85	°C
Storage Temperature Range	910	T _{stg}	-65 to +150	оС

TRUTH TABLES

BOTH TYPES

Clock	Inhibit	Preset Enable	Master Reset	Action
0	0	0	0	No Count
5	0	0	0	Count-1
×	1	0	0	No Count
1	17	0	0	Count-1
×	×	1	0	Preset
×	X	X	1	Reset

MC14522B

	Output									
Coent	Q3	Q2	,Q1	0.0						
9 8	1 1	0	0	1 0						
7 6 5 4	0 0 0	1 1 1 1 1	1 1 0 0	1 0 1 0						
3 2 1	0 0	0 0	1 1 0	1 0 1						

MC14526B

	Output QQ V								
Count	0.3	Q2	01	0.0					
15 14 13 12	par ju	ani ii s	1 1 0 0	1 0 1					
11 10 9 8	1 1 1 1	0 0 0	1 1 0 0	1 0 1 0					
7 6 5 4	0 0 0	1 1 1 1	1 1 0 0	1 0 1 0					
3 2 1 0	0 0 0	0 0 0	1 1 0 0	1 0 1 0					

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

PROGRAMMABLE DIVIDE-BY-N 4-BIT COUNTERS

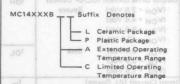
> BCD - MC14522B Binary - MC14526B



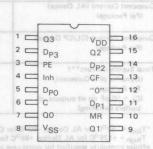
L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX PLASTIC PACKAGE CASE 648

ORDERING INFORMATION



PIN ASSIGNMENT IO - AVI



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leqslant (V_{in} \text{ or } V_{out}) \leqslant V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD).

		VDD	-	w*	25°C		Th	igh*		
Characteristic	Symbol	Vdc	Min	Max	Min	Тур	Max	Min	Max	Unit
Output Voltage "0" Level	VOL	5.0	-	0.05	-	0	0.05	-	0.05	Vdc
Vin = VDD or 0		10	-	0.05	-	0	0.05		0.05	-
PROWER COMPLEMENTARY MOSI	ion I	15	TERS	0.05	187 /	- 0	0.05	BAMM	0.05	19
"1" Level	VOH	5.0	4.95	-	4.95	5.0	-	4.95		Vdc
Vin = 0 or VDD	DAY	10	9.95	enid 88	9.95	10	gundos (9.95	18 MC 148	1
4-BIT COUNTERS		15	14.95	frie jenn	14.95	15	NOS P-	14.95	onstructe	976
nput Voltage# "0" Level	VIL				,976	FOU US SHI	MODON	ignie s n	GBSHUES S	Vdc
(VO = 4.5 or 0.5 Vdc)	-11	5.0	tiw znem	U015 W	to eldab	2.25	1.5	d 938 25	1.5	A CC
(VO = 9.0 or 1.0 Vdc)		10	In single	3.0	ros Vi-v	4.50	3.0	0 07232 "	3.000	a de
(V _O = 13.5 or 1.5 Vdc)		15	der-il te	4.0	ot balls	6.75	4.0	adt-ano	4.0	SUBUR
"1" Level	VIH	10		4.0	to ewol		Landino	abcons	0.04.0	ugni
(V _O = 0.5 or 4.5 Vdc)	VIH	5.0	-yd-sbiy	Value of		5 Jugni	SUBUSUS IN			
(V _O = 1.0 or 9.0 Vdc)			3.5	int Hook	3.5	2.75	ig lenoit	3.5	Biw-noise	Vdc
(VO = 1.5 or 13.5 Vdc)	Direct II	10	7.0	_	7.0	5.50	noo-salui	7.0	nild a aib a	wolls
		15	11.0	ni Toneu	11.0	8.25	ROW AND R	11.0	mon - manu	T
Output Drive Current (AL Device)	ОН		i que nois	ivib yous	upest requi	s, and oth	gool be:	hass-look	resizers, p	mAdc
(V _{OH} = 2.5 Vdc) Source	0.001	5.0'	-3.0	enion ric	-2.4	-4.2	uib tewe	-1.7	กร regula	pisses
(V _{OH} = 4.6 Vdc)	1	5.0	-0.64	-	-0.51	-0.88	-	-0.36	-	
(V _{OH} = 9.5 Vdc)	. 1	10	-1.6	-	-1.3	-2.25	-	-0.9	-	
(V _{OH} = 13.5 Vdc)	1	15	-4.2	ab¥ 8 ¶	-3.4	-8.8	An-0.∂	-2.4	Inscrain	0 0
(VOL = 0.4 Vdc) Sink	IOL	5.0	0.64	-	0.51	0.88	0.8 = 80	0.36	leV-vion	mAdo
(VOL = 0.5 Vdc)		10	1.6	-	1.3	2.25	-	0.9	-	
(VOL = 1.5 Vdc)		15	4.2	K retrible	3.4	8.8	ing for h	2.4	tarnality 5	11 9
Output Drive Current (CL/CP Device)	ІОН		nuitianan'	avisico9	no beto	emetani -	Design	Clocked	suic Edge	mAdo
(Var 2 E Vida) Course	-	5.0	-2.5	- 4	-2.1	-4.2	inis-caT	-1.7	Clock or	in
(V _{OH} = 4.6 Vdc)	MCNE	5.0	-0.52		-0.44	-0.88	Permitted by	-0.36	TO MODILE	
(VOH = 9.5 Vdc)		10	-1.3	_	-1.1	-2.25	_ 016	-0.9	D MHIT OF	9 0
(VOH = 13.5 Vdc)		15	-3.6		-3.0	-8.8	En s sig	-2.4	nor-have	A a
(VOI = 0.4 Vdc) Sink	Lav	5.0	0.52		0.44	0.88		0.36	THE STORY	mAdo
(VOI = 0.5 Vdc)	IOL	10		s, One L	District Co. Co. Co.	10 100000000000000000000000000000000000	NOT DAY	78 - EXCESS VOL. 11-LA	to stosqu	mAde
(VOL = 1.5 Vdc)	1	15	1.3	ets Rate	3.0	2.25 8.8	OF TWO	0.9	hotticy T	- 36
02			3.6	-	3.0		-	2.4	us Range	te .
nput Current (AL Device)	lin	15	-	± 0.1		±0.00001	± 0.1	-	±1.0	μAdc
nput Current (CL/CP Device)	lin	15	-	± 0.3	- 1	±0.00001	±0.3	SS (Yolts	±1.0	μAdc
nput Capacitance	Cin	Hint.	-	Helde	Hedro	5.0	7.5	-going	-	pF.
(Vin = 0) THEMMENT (0 = niV)		Vete	81	-0.5.to	00				saurio	vione
Quiescent Current (AL Device)	IDD	5.0	Den :	5.0		0.005	5.0		150	μAdc
(Per Package)	.00	10	0.0	10	01.5	0.010	10		300	100 1075
		15	1	20	1	0.015	20	0	600	TUSTAN
uiescent Current (CL/CP Device)	IDD	5.0	- 09	20	A	0.005	20	- senañ	150	μAdo
(Per Package)	ו סטי	10	88	F 037074		0.005	40	100		μAdc
(Per Package)		15	98	40 80	1000	0.015	80	epm	300	me T sp
10 to			-	80	1 - 1				600	
otal Supply Current**†	IT	5.0			T = (1	1.7 μA/kHz) f + 100			μAdc
(Dynamic plus Quiescent,		10	1 34.5			3.4 μA/kHz				
Per Package)		15			17 = (£	5.1 μA/kHz	II+ IDD			
(CL = 50 pF on all outputs, all			1							
buffers switching)										

T_{1ow} = -55°C for AL Device, -40°C for CL/CP Device.

Thigh = +125°C for AL Device, +85°C for CL/CP Device.

#Noise immunity specified for worst-case input combination.

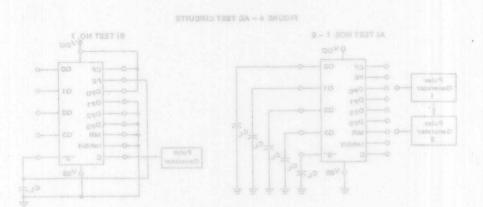
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc

Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc 2.0 Vdc min @ V_{DD} = 10 Vdc 2.5 Vdc min @ V_{DD} = 15 Vdc 1 To calculate total supply current at loads other than 50 pF: $I_{T}(C_{L}) = I_{T}(50 \text{ pF}) + 1 \times 10^{-3} (C_{L} - 50) V_{DD}$ where: I_{T} is in μ A (per package), C_{L} in pF. V_{DD} in Vdc, and f in kHz is input frequency. "The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS*	(C. = 50 pF T. = 250C)	

Characteristic	Symbol	VDD	Min	Тур	Max	Unit
Output Rise Time	tTLH	Но				ns
tTLH = (3.0 ns/pF) CL + 30 ns		5.0	-	100	200	
tTLH = (1.5 ns/pF) CL + 15 ns		10		50	100	-
tTLH = (1.1 ns/pF) CL + 9.5 ns		15	_	40	80	
Output Fall Time	†THL			- 0	10	ns
t _{THI} = (1.5 ns/pF) C ₁ + 25 ns	11112	5.0		100	200	-0-4
t _{THL} = (0.75 ns/pF) C _L + 12.5 ns		10	- 0	50	100	-0-6
t _{THL} = (0.55 ns/pF) C _L + 9.5 ns		15	_ 9	40	80	-0-
Proposetion Delay Time	20111	-			1.1.1	ns
Q Outputs	tPLH,				290	
tpLH, tpHL = (1.7 ns/pF) CL + 465 ns	PHL	5.00		550	1100	-0-
tp_H, tpHL = (0.66 ns/pF) CL + 197 ns		10	1	225	450	10-
tp_H, tpHL = (0.5 ns/pF) CL + 135 ns		15		160	320	-0
"0" Output		15	_	160	320	-0-
tpLH, tpHL = (1.7 ns/pF) CL + 155 ns		5.0	10 E	240	480	
tp_H, tpHL = (0.66 ns/pF) CL + 87 ns		10	Pos	130	260	-
tp_H, tpHL = (0.5 ns/pF) CL + 65 ns			Sup	100	200	130
Minimum Clock Pulse Width	_	5.0	250	125	-	
Willimum Clock Fulse Wildth	tWH(cl)			130000	-	ns
		10	100	50	-	
NOTE TO A STATE OF THE STATE OF		15 700	80	40	-	
Maximum Clock Pulse Frequency (with PE = low)	fcl	5.0	-	2.0	1.5	MHz
		10	-	5.0	3.0	
		15		6.6	4.0	
Maximum Clock or Inhibit Rise and Fall Time	tTLH,	5.0			15	μs
	THL	10	-1	-	5	
		15	-1	_	4	
Hold Time	th	5.0	150	75	-	ns
		10	50	25	_	
		15	40	20	_	
Minimum Preset Enable Pulse Width	tWH(PE)	5.0	250	125	T _	ns
1 7.0.	WHI(PE)	10	100	50		113
	1 0-	15	80	40		
Minimum Master Reset Pulse Width	hausten:	5.0	350	175		-
William Master Meset Fulse Width	tWH(R)	10	250	175		ns
		15	200	100	_	
	elise token	10	200	100	_	

^{*} The formulae given are for the typical characteristics only.





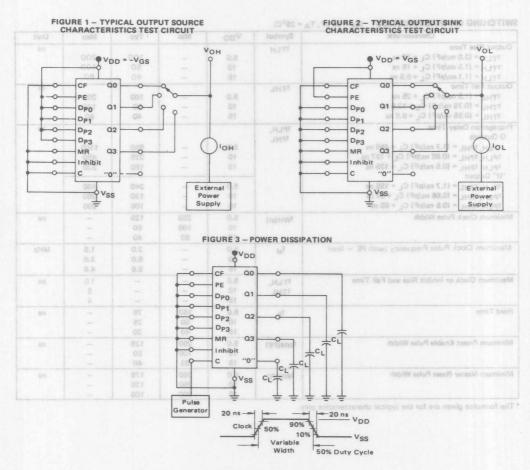


FIGURE 4 - AC TEST CIRCUITS

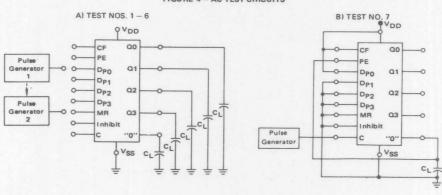
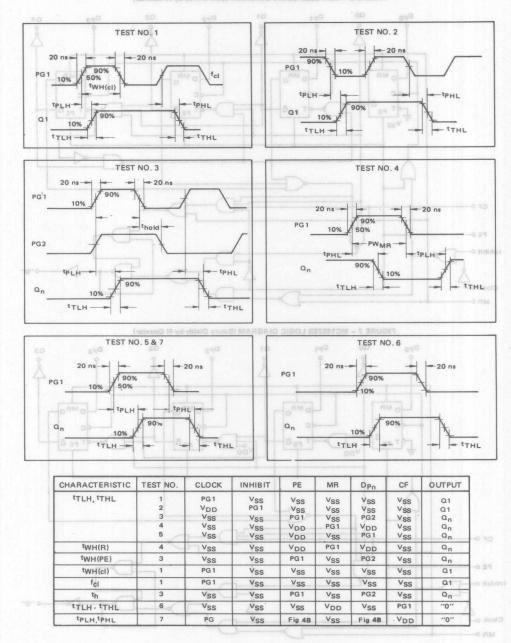
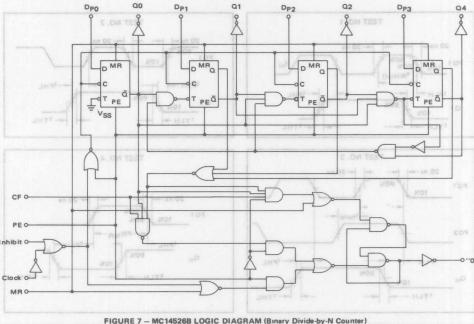


FIGURE 5 - AC TEST CONNECTIONS AND WAVEFORMS





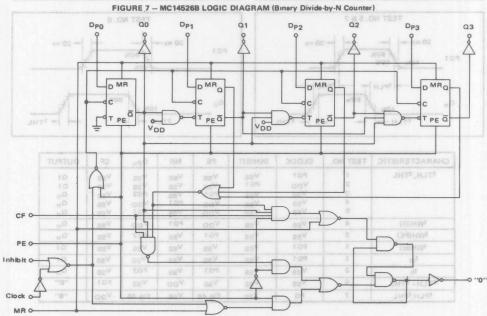
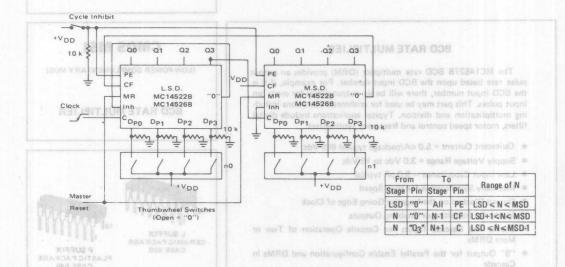
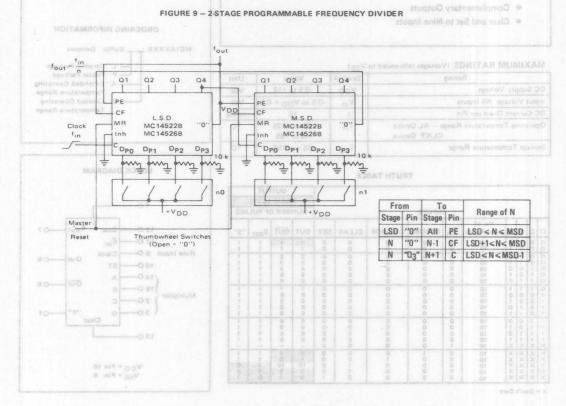


FIGURE 8 - 2-STAGE PROGRAMMABLE DOWN COUNTER (One Cycle)





MC14527B

BCD RATE MULTIPLIER

FIGURE 8 - 2 STAGE PROGRAMMABLE DOWN COUNTER

The MC14527B BCD rate multiplier (DRM) provides an output pulse rate based upon the BCD input number. For example, if 6 is the BCD input number, there will be six output pulses for every ten input pulses. This part may be used for arithmetic operations including multiplication and division. Typical applications include digital filters, motor speed control and frequency synthesizers.

- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Low Input Capacitance 5.0 pF typical
- Internally Synchronous for High Speed
- Output Clocked on the Negative Going Edge of Clock
- Strobe for Inhibiting or Enabling Outputs
- Enable and Cascade Inputs for Cascade Operation of Two or More DRMs
- "9" Output for the Parallel Enable Configuration and DRMs in
- Complementary Outputs
- Clear and Set to Nine Inputs

MAXIMUM RATINGS (Voltages referenced to Voc.)

Rating	Symbol	value 10	Unit
DC Supply Voltage	VDD	-0.5 to +18	Vdc
Input Voltage, All Inputs	Vin	-0.5 to V _{DD} + 0.5	Vdc
DC Current Drain per Pin	1	10	mAdc
Operating Temperature Range - AL Device CL/CP Device	TA	-55 to +125 -40 to +85	°C
Storage Temperature Range	T _{stg}	-65 to +150	°C

TRUTH TABLE

								105	1		OUT	PUT	
											OGIC	LEVEL	100
			W			INPUTS		NUN	NUMBER OF PULSES				
D	С	В	A	No. of Clock Pulses	Ēin	STROBE	CASCADE	CLEAR	SET	OUT	OUT	Eout	"9"
00	0	00	0	10 10	0	1-10	0	0	0	0	1	1 1	1 1
00000	0 0 1 1 1 1	1 0 0 1	0 1 0 1 0	10 10 10 10 10	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0 0	0 0 0 0	2 3 4 5 6	2 3 4 5 6	1 1 1 1 1	1 1 1 1 1
0 1 1 1 1 1	1 0 0 0 0	1 0 0 8	1 0 1 0 1	10 10 10 10 10	0 0 0	0 0 0 0	0 0 0 0	0 0 0 0 0	0 0 0 0	7 8 9 8 9	7 8 9 8 9	1 1 1 1 1	1 1 1 1 1
1 1 1 1 X	1 1 1 1 X	0 0 1 1 X	0 1 0 1 X	10 10 10 10 10	0 0 0 0 1	0 0 0	0 . 0 . 0 . 0 . 0	0 0 0 0 0	0 0 0 0	8 9 8 9	8 9 8 9	1 1 1 -	1 1 1 1 -
X X 1 0 X	XXXX	XXXX	XXXX	10 10 10 10	0 0 0 0	1 0 0 0	0 1 0 0	0 0 1 1 1 0	0 0 0 0 1	1000	1 0 10 1	1 1 1 1 1 0	1 1 0 0 1

X = Don't Care

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

BCD RATE MULTIPLIER



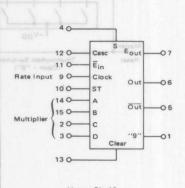


PLASTIC PACKAGE CASE 648

ORDERING INFORMATION

MC14XXXB _ Suffix Denotes - L Ceramic Package P Plastic Package - A Extended Operating Temperature Range - C Limited Operating Temperature Range





V_{DD} = Pin 16 V_{SS} = Pin 8

	xsM	Typ	nihi	VDD	Tic	ow*		25°C	01701500	Thi	igh °	
an C	haracteristic		Symbol	Vdc	Min	Max	Min	Тур	Max	Min	Max	Unit
Output Voltag	e our	"0" Level	VOL	5.0	-	0.05	-	0	0.05	+ 75 (46	0.05	Vdc
Vin = VDD	or 0	0.9		10		0.05	-	0	0.05	4 10 (30	0.05	LIFE
		. OA		15		0.05	_	0	0.05	+ JO (3q	0.05	U73
80		"1" Level	VOH	5.0	4.95	JHT	4.95	5.0	-	4.95	8037 135	Vdc
Vin = 0 or '	VDD	100	0	10	9.95	-	9.95	10	En 65	9.95	and_() =	HT7
	001	. 60	344	15	14.95	-	14.95	15	12.5 ns	14.95	= (0,78 n	MTI
Input Voltage#	-00	"0" Level	VIL						111 0.0	30 1 195	17 (00,0)	Vdc
(VD = 4.5 c	r 0.5 Vdc)			5.0	-	1.5	-	2.25	1.5	<u>90717</u>	1.5	1008401
(VO = 9.0 c				10	-	3.0	-	4.50	3.0	-	3.0	Clock!
(VO = 13.5		200		15	-	4.0	-	6.75	4.0	Aglen T.1	4.0	191
		"1" Level	VIH					911	0.4301	Marie Agric	S. J. H. H.	FT.At
(VO = 0.5 c	r 4.5 Vdc)	70		5.0	3.5	-	3.5	2.75	99+10	3.5	" THAT	Vdc
(VO = 1.0 c				10	7.0	HJE	7.0	5.50	_	7.0	100 a	Clock
(VO = 1.5 c		125	-	15	11.0	JHP	11.0	8.25	GL ±40	11.0	PART.	1192
Output Drive C	urrent (AL	Device)	ГОН	1			1	SIL	10 - 10 t	MAIN CO.C	21Hd1	mAdc
(VOH = 2.5		Source	·On	5.0	-3.0	-	-2.4	-4.2	CL + 20	-1.7	1 Tilds	17141
(VQH = 4.6				5.0	-0.64	H.J.DJ	-0.51	-0.88	_	-0.36	1140 E 0411	Clack
(VOH = 9.5		295	-	10	-1.6	11497	-1.3	-2.25	CL + 210	-0.9	" Held.	16297
(VOH = 13.		130	-	15	-4.2	-	-3.4	-8.8	18+_10 (-2.4	10141 *	HJ93
(V _{OL} = 0.4		Sink	loL	5.0	0.64	-	0.51	0.88	00 - 10	0.36	s = Tilda	mAdo
(VOL = 0.5		SIIIK	IOL	10	1.6	H-101	1.3	2.25		0.9	7.6	IIIAGC
(VOL = 1.5		000	-	15	4.2	JHS	3.4	8.8	CF F318	2.4	1 - Digt.	1,392
Output Drive C	urrent (CL/	CP Device)	ГОН	1				400 3	10.0	Nun co.c	389	mAdo
(VOH = 2.5		Source	·UH	5.0	-2.5		-2.1	-4.2	CL + 85	-1.7	" THAT	11/1/1
(VOH = 4.6				5.0	-0.52	THE	-0.44	-0.88	_	-0.36	Clear_to C	Set or
(VOH = 9.5		380	-	10	-1.3	-	-1.1	-2.25	295 <u>n</u> s	-0.9	# [1 <u>.7</u> nu	Helph.
(VOH = 13.		165	200	15	-3.6	-	-3.0	-8.8	132 ns	-2.4	m 38,0) m	HH92
(VOL = 0.4		Sink	lOL	5.0	0.52	_	0.44	0.88	81 00	0.36	(an 0.0)	mAdc
(VOL = 0.5		SIIIK	OL	10	1.3	H.PSI	1.1	2.25		0.9	10 <u>0</u> 02 1	IIIAGC
(VOL = 1.5		125	-	15	3.6	_	3.0	8.8	_an 01	2.4	lon <u>V</u> .11 =	1H42
Input Current (1100	- 00	lin	15	5.0	± 0.1	3.0	±0.00001	±0.1	10.130	±1.0	μAdc
Input Current (1		15		± 0.3	-	±0.00001	5,61,135	7 12 (B)	1000	1000
		cei	lin		-	14-1477			± 0.3		±1.0	μAdc
Input Capacitar (V _{in} = 0)	250 920	230	Cin	- 0	-	-	-	5.0	7.5	OF) CL+	(an (T.F) = n 86.01 =	pF
Quiescent Curr		rice)	IDD	5.0	-	5.0	-	0.005	5.0	# JB (Rd	150	μAdc
(Per Package	e)	250	500	10	-	10	-	0.010	10	-	300	A Hook
		011	200	15	-	20	-	0.015	20	-	600	
Quiescent Curr	ent (CL/CP	Device)	IDD	5.0	-	20	-	0.005	20	-	150	μAdc
(Per Packag	e) <u>c</u> (e	2.0	-	10 0	-	40	-	0.010	40	- van	300	Plack Pa
	2.5	4.6		15	-	80	-	0.015	80	-	600	
Total Supply C	urrent**†	0.0	IT	5.0			IT = (0	.85 μA/kHz) f + lpp			μAdc
(Dynamic p		and the same of th		10	5	11.199	IT = (1	.75 μA/kHz) f + Ipp			
Per Package				15	-	10.272	IT = (2	6 μA/kHz) f + Ipp	110 1 01		- January
(CL = 50 pF		uts, all				THAT		p,	UU			
buffers swi			-		-							
	3.	536	1100	1 0		HIMT				- STOR	A WEST IN THE	110000

**Tlow = -55°C for AL Device, -40°C for CL/CP Device.

Thigh = +125°C for AL Device, +85°C for CL/CP Device.

**Noise immunity specified for worst-case input combination.

Noise Margin for both "1" and "0" level = 1.0 Vdc min @ VDD = 5.0 Vdc

2.0 Vdc min @ VDD = 10 Vdc

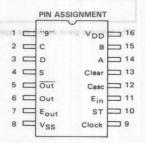
2.5 Vdc min @ VDD = 15 Vdc

1To calculate total supply current at loads other than 50 pF:

IT(CL) = IT(50 pF) +1.2 × 10⁻³ (CL -50) VDD

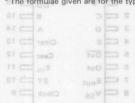
where: IT is in µA (per package), CL in pF, VDD in Vdc, and f in kHz is input frequency.

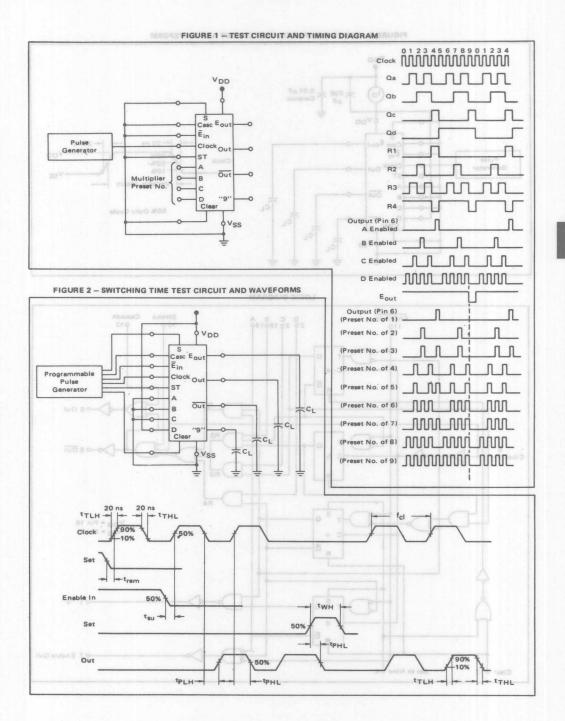
**The formulas given are for the typical characteristics only at 25°C.



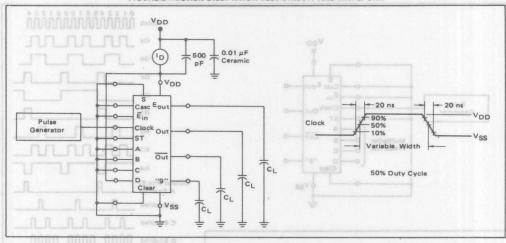
Characteri	istic	2800		Symbol	VDD	Visi	Min	Тур	Max	Unit
Output Rise Time		Typ	- Min	tTLH	124	Vác	Byrnisal		Charperspissi	ns
tTLH = (3.0 ns/pF) CL + 30	ns			60.0	5.0	5.0	JoV	100	200	How readed
tTLH = (1.5 ns/pF) CL + 15	ns			30.0	10	01	-	50	100	
tTLH = (1.1 ns/pF) CL + 10	ns			ann	15	20	-	40	80	
Output Fall Time			4.95	tTHL	0.6	0.8	1	Name of Street		ns
tTHL = (1.5 ns/pF) CL + 25			8.86	STILL	5.0	0.0	HOV	100	200	
tTHL = (0.75 ns/pF) CL + 12				- 13	10		1 -	50	100	
tTHL = (0.55 ns/pF) CL + 9.			14.95	- 1	15	-81	-	40	80	
Propagation Delay Time		-		tour			1117	leve F 'O'	201	ns
Clock to Out		2.28		tPHL,	F F	5.0			lobV 8.0 to	
tpLH. tpHL = (1.7 ns/pF) C	0.8 A			TPHL	5.0	01		200	400	
tpLH, tpHL = (0.66 ns/pF) (0.4	10	15		100	200	
					15		HIV	70	140	
tPLH, tPHL = (0.5 ns/pF) C	T 45 NS				15	6.0	1 -	70	THE R. P. LEW.	140-08
Clock to Out			7.0	tPLH,	1.7.0	01			(abV 0.9 ap	ns
tpLH, tpHL = (1.7 ns/pF) C				tPHL	5.0	311	-	125	250	B. L = OVI
tpLH, tpHL = (0.66 ns/pF)					10		leur	65	130	
tpLH, tpHL = (0.5 ns/pF) C	+ 20 ns	- 4.2	-2.4	- 10	15	0.8	200	45	90	S-MAVI
Clock to Eout				tPLH,	0-0.8	0.8			6 Vec)	ns
tpLH, tpHL = (1.7 ns/pF) C				tPHL	5.0	10	-	295	590	
tpLH tpHL = (0.66 ns/pF) (10	ar	- 1	130	260	T = HD\/4
tpLH, tpHL = (0.5 ns/pF) C	+ 60 ns				15			85	170	
Clock to "9"				tPLH.	100	200	1 10		710077 7	ns
tpLH, tpHL = (1.7 ns/pF) C	+ 315 ns			tPHL	5.0	10		400	800	-0.35
tpLH, tpHL = (0.66 ns/pF) (3.6	THE	10	- 25	1	155	310	(VOL = 1
tpLH, tpHL = (0.5 ns/pF) C	+ 85 ne				15		HOL	110	220	swing Juque
				-	15-1-	0.0		- Constant	TISNV 8	Creek
Set or Clear to Out	- 8			tPHL S	1.0-	5.0		200	S Vdc)	ns
*tpHL = (1.7 ns/pF) CL + 29				- 13	5.0	10.0	-	380	760	6 = MOAI
tpHL' = (0.66 ns/pF) CL + 1:				- 1-1	10	165	-	165	330	(VOH = 1
tpHL = (0.5 ns/pF) CL + 85	ns				15	(3.22	Test	110	220	O S WAYS
Cascade to Out			1.1	tPLH	1.1	10	30		5 Vide)	ns ns
tpHL = (1.7 ns/pF) CL + 40	ns				5.0	15	-	125	250	5 - 10VI
tpHL = (0.66 ns/pF) CL + 32	2 ns			.101	10	21		65	130	manua Curran
tpHL = (0.5 ns/pF) CL + 20	ns			1 102	15	01	-01	45	90	ne nuo nugi
Strobe to Out				tPLH		9.0	. 1817	19	1880 201327	ns
tpHL = (1.7 ns/pF) CL + 145	5 ns				5.0	-	_h(0)	230	260	Plasent Capsell
tpHL = (0.66 ns/pF) CL + 72					10		_	105	210	(0 = m/V)
tpHL = (0.5 ns/pF) CL + 45				0.8	15	5.0	-nl	70	140	uD znaceni
Clock Pulse Width		010.0		twH	5.0	01	500	250	_ 100	ns
OOR THIS PRINT				WH	10	315	200	110		113
				ne l	15	62	150	80	901J9) Inest	uioscant Gu
		010.9		N/3	5.0	10	100			
Clock Pulse Frequency				fcl	1	15	-	2.0		MHz
008 1 - 1				08	10		-	4.5	2.5	
abAu l ne	1 + 1 dsld				15	5,0	-71	6.0	3.5	otal Supply
Clock Pulse Rise and Fall Time				tTLH,	5.0	1.0	-	-	15	μs
. GC	at a restrict			tTHL.	10	15	-	-	1	Per Packs
					15		-	_36,36	anuo 14 no 90	(61, = 50
Set or Clear Pulse Width				twH	5.0		240	80	(Survivous	ns
					10		100	35	vaG JA set S	038
					15	-	75	30	40 46 Tel 00	ich wil
Set Removal Time				Ť	5.0	noise.	0	-20	belli-or yri	ns of
				trem		6) 10	0 1 -	-10		
				obV 0		@ n	000	-7.5	101	THE PERSON
		-		45.17.3	-	D 10	100		-	
Enable In Setup Time				t _{su}	5.0	200	400	175	-	ns
PIN ASSIGNMENT					10	191 00	150	60	total supply of	
					15		120	45	+ (3g ge)+1 =	(10)71

^{*} The formulae given are for the typical characteristics only.









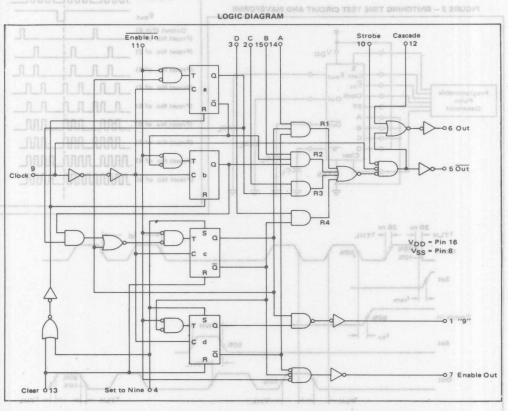
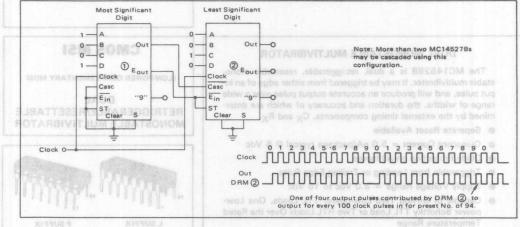


FIGURE 4 - TWO MC145278s IN CASCADE WITH PRESET NO. of 94

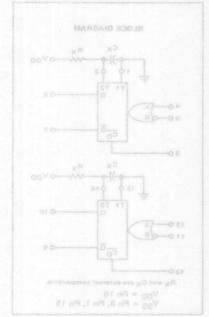


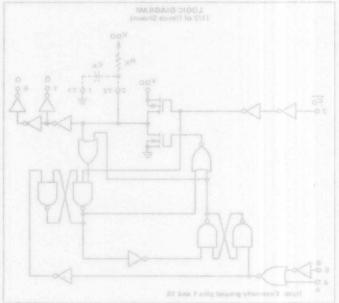
CASE 648

		Greater	9 For

MOTOROLA

	enlsV	Pating
	-0.5 to +18	
Vdc		
20		Operating Temperature Range - AL Dovice GU/OP Device





3



MC14528B

DUAL MONOSTABLE MULTIVIBRATOR

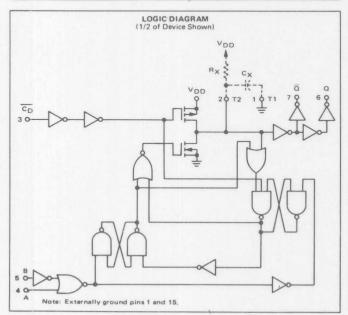
O MC1452784 IN CASOADE WITH PRESET NO. of S4

The MC14528B is a dual, retriggerable, resettable monostable multivibrator. It may be triggered from either edge of an input pulse, and will produce an accurate output pulse over a wide range of widths, the duration and accuracy of which are determined by the external timing components, C_X and R_X .

- Separate Reset Available
- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- Diode Protection on All Inputs
- Triggerable from Leading or Trailing Edge Pulse
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range
- ullet For Pulse Width Greater than 1.0 μ S, the MC14548B Is Recommended

MAXIMUM RATINGS (Voltages referenced to Vss)

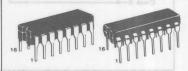
Rating	Symbol	Value	Unit
DC Supply Voltage	V _{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	Vin	-0.5 to V _{DD} + 0.5	Vdc
DC Current Drain per Pin	1	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	TA	-55 to +125 -40 to +85	°C
Storage Temperature Range	T _{stg}	-65 to +150	°C



CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

DUAL
RETRIGGERABLE/RESETTABLE
MONOSTABLE MULTIVIBRATOR



L SUFFIX
CERAMIC PACKAGE

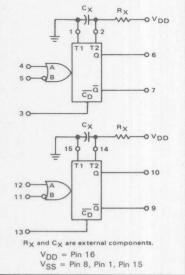
P SUFFIX
PLASTIC PACKAGE

ORDERING INFORMATION

MC14XXXB Suffix Denotes

L Ceramic Package
P Plastic Package
A Extended Operating
Temperature Range
C Limited Operating
Temperature Range

BLOCK DIAGRAM



			aa,	35,311	VDD	Tio	w*		25°C	hartman A	Thi	gh* .	
	Characteristi		Vdc	Symbol	Vdc	Min	Max	Min	Тур	Max	Min	Max	Unit
Output	Voltage	"0" L	evel	VOL	5.0	RUHT I	0.05	-	0	0.05	-	0.05	Vdc
Vin	= V _{DD} or 0		6.0	0.	10	-	0.05	-	0	0.05	10FTCL+	0.05	177
	S0 100	-	01-		15	-	0.05	_	0	0.05	LOFTCL -	0.05	173
		"1" L	evel	VOH	5.0	4.95	_	4.95	5.0	38.01	4.95	11.11	Vdc
Vin	- 0 or VDD			On	10	9.95	_	9.95	10	_	9.95	erol Tito?	Duspul
	100 200		0.3		15	14.95		14.95	15	20 05	14.95	n 2 11 - 1	672
Input V	oltage#	"0"	Level	VIL						In 2,51 9	30 thqui	93.U1 ~]	Vdc
	= 4.5 or 0.5 Vdc)	-	16	11.	5.0	_	1.5	_	2.25	1.5	JO (30/o	1.5	177
	= 9.0 or 1.0 Vdc)			5.0	10	,14,1217	3.0	_ 3	4.50	3.0	t Delay T	3.0	DemisT
	= 13.5 or 1.5 Vdc)		0.8		15	THE!	4.0	-	6.75	4.0	Bolem T.T.	4.0	101
		"1"	Level	VIH					60.3	0 4 70 14	avan 00,01	* JH97.3	192
(Vo	= 0.5 or 4.5 Vdc)		15	-111	5.0	3.5	_	3.5	2.75	1 CL + 88	3.5	* 3H97.1	Vdc
	= 1.0 or 9.0 Vdc)				10	7.0	_	7.0	5.50	0 A - 07	7.0	O-muiT.	D-maT
-	= 1.5 or 13.5 Vdc)		6.0		15	11.0	_	11.0	8.25	1 CL 2- 62	11.0	F 31497 A	191
	Drive Current (AL		- 01	ТОН	-	11.0		11.0	0.20	1917	(tun 00.01	ur i	mAdo
	4 = 2.5 Vdc)	Source	20.0	ЮН	5.0	-1.2		-1.0	-1.7	81 + 10 (-0.7	* JH97 J	MAGC
	4 = 4.6 Vdc)	087	5.0		5.0	-0.64		-0.51	-0.88	-	-0.36	fred Wilder	jugni
	4 = 9.5 Vdc)		10		10	-1.6	_	-1.3	-2.25	_	-0.36	_	1
	4 = 13.5 Vdc)		31		15	-4.2		-3.4	-8.8	_	-2.4	_	
	= 0.4 Vdc)	Sink	5.0	1,07	5.0	0.64	-	0.51	0.88		0.36	_	mAdo
	= 0.4 Vdc)	SINK	10	IOL	10		200			-		-	MAdd
	= 1.5 Vdc)		16		15	1.6	_	1.3	2.25 8.8		0.9	-	
			-	1	15		-	3.4	8.8	-	2.4	_	-
	Drive Current (CL/		45.0	ІОН		Mil		LinuxLini	Vatabana	ph for opt	N 100 20	EX ≤0.03	mAdo
0.	4 = 2.5 Vdc)	Source	35		5.0	-1.0	-	-0.8	-0.7		-0.6	- 4-	
	4 = 4.6 Vdc)		5.0		5.0	-0.52	-	-0.44	-0.88	-	-0.36	A COLUMN TO	
	4 = 9.5 Vdc)		1.0		10	-1.3	-	-1.1	-2.25	- A	-0.9	Puleative	
	4 = 13.5 Vdc)		15		15	-3.6	-	-3.0	-8.8	: <u>uluma</u>	-2.4	C _X ≥ 9.0	
	= 0.4 Vdc)	Sink		IOL	5.0	0.52	-	0.44	0.88	- 00 x	0.36	W. P 18	mAdo
	= 0.5 Vdc)	-	0.8		10	21.3	-	1.1	2.25	mi alluonii	0.9	dun March	Pulse V
(VOI	= 1.5 Vdc)		Of		15	3.6	-	3.0	8.8	-	2.4	_	
Input Cu	irrent (AL Device)		0.1	lin	15	-	±0.1	-	±0.00001	±0.1	-	± 1.0	μAdc
Input Cu	rrent (CL/CP Devi	ice)	0.0	lin	15	147ah	± 0.3	-	±0.00001	± 0.3	- Antorn	±1.0	μAdc
Input Ca	pacitance = 0)		15	Cin	-	200	-		5.0	7.5	-	- 1	pF
Quiescer	nt Current (AL Dev	vice)	0.0	IDD	5.0	-	5.0	-	0.005	5.0	-	150	μAdc
	Package)		10	.00	10	_	10	_	0.010	10	-	300	-
	195		611		15	-	20	-	0.015	20	-	600	-
Quiescer	nt Current (CL/CP	Device	1 0	IDD	5.0	12	20	-	0.005	20		150	μAdo
	Package)	- CVICE	90.1	יטטי	10		40	_	0.010	40		300	μAdd
		0	16		15		80		0.015	80		600	
* Total	Supply Current	-	0.2	l=	7,10	1.15		-			D 0 (1:		2
los	Supply Current at ad Capacitance (Cu ternal timing capac the formula —) and a	16 tr	lΤ		IT(CL)	, C _X) = [(here: I _T	in μA (per	CX)VDDf f circuit), CL Vdc, f in kH	and CX	n pF, RX	n megohr	ns,

*Tlow = -55°C for AL Device, -40°C for CL/CP Device.

Thigh = +125°C for AL Device, +85°C for CL/CP Device.

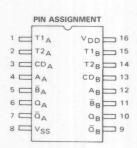
#Noise immunity specified for worst-case input combination.

Noise Margin for both "1" and "0" level = 1.0 Vdc min @ VDD = 5.0 Vdc

2.0 Vdc min @ VDD = 10 Vdc

 $2.5~\rm Vdc~min~@~V_{DD}~=15~\rm Vdc$ **The formulas given are for the typical characteristics only at $25^{o}C$.

The formulas given are in	or the typical and	nootoriatios offi	01 20 0.
	8		
Y A	4	3	H
Not Triggered Not Triggered	六	1A	
Not Triggered Not Triggered	L, H, _		
L H Not Triggered	×	X	i



SWITCHING CHARACTERISTICS** (CL = 50 pF, TA = 25°C)

			Characteris				Symbol	CX	RX	VDD	Min	Тур	Max	Unit
He Unit	leg/M	Min	NBK	Typ	nild	Max	nilit	pF	kΩ	Vdc	si	811075618	10	
The state of the s	Rise Time		60.0				TLH	0.0	JO.	lava	1 "0"		operioV	ns
	4 = (3.0 ns						-	10		5.0	-	100	200	niV.
	4 = (1.5 ns						H 1	15		10	-	50	100	100
	4 = (1.1 ns	/pF) CL	+ 10 ns	0.8	4.95		4.95	0.8	Vay	15	3-17-1	40	80	
	Fall Time						THL	OT	-			00	V 10 0 :	ns
	= (1.5 ns						14.95	87		5.0	-	100	200	
	= (0.75 n								JIV	10	.0	50	100	V rus
	= (0.55 n			2.05		21		50	21	15	-	40	80	No
				r B to Q or	0		tPLH,	15	5.0			IsbV 0.1	10 0.8	ns
TPLH	, tPHL =	1.7 ns/p	F) CL + 24	O ns		0.6	tPHL	aı		5.0	- 1	325	650	(No
			pF) CL + 8						HIN	10	ope-	120	240	1
			F) CL + 65		25		2.5	loal	1,10	15	-	90	180	OVE
				r B to Q or	0		tPLH,	1000	10			abV 0.6	1.0 0.1	ns
TPLH	, tPHL =	1.7 ns/p	F) CL + 62	20 ns			tPHL	16		5.0	- 1	705	107.1	OVI
			pF) CL + 2					-	HO	10	soivaCl	290	uO revisi	togs
tPLH	I, TPHL =	0.5 ns/p	F) CL + 18	5 ns	-0.t-		0.1	o.a	mb.	15	Soluces	210	V 25 ×	(No.
Input Pu	ulse Width	- A or E	В	88.0-	-0.51	-	tWH	15	5.0	5.0	150	70	/ 8.0 -	ns
							8.1-	10		10	75	30	4 8:5 V	(Vo
							24-1	15		15	55	30	a.et =	lov)
							tWL	1000	10	5.0	Sink	70	V 1071 -	ns
							1.6	01	200	10	-	30	V 2001 -	(VOI
							4.2	ar I		15	-	30	(27 -	LOVA
Output I	Pulse Widt	h - Q or	ā				tw	15	5.0	5.0	vaCT40\	550	- 0	ns
(For t	CX < 0.01	μF use gr	aph for app	propriate V	D level.)		0.1-	5.0	HO	10	Source	350	U ST	(VO
				99.0	A D . O		ea n	5.0		15	-	300	V 27	200
Output I	Pulse Widt	h - Q or	ā	-2.25	1.1-1		e tw	10,000	10	5.0	_	30	±15	μs
(For	Cx > 0.01	μF use t	formula:				8.8-	15		10	_	50	±40	(VO
			[VDD - V	/ss])†			CRO	0.8		15		55	±40	Lava
		107000, 101		the same pa				10,000	10	5.0	Mile	6.0	25	%
-		2.4		8.8	0.8		t1 - t2	at		10	_	8.0	35	(NO)
		P.X	-				3.8	91	-	15	-	8.0	35	10.41
Recet Pr	onecation	Delay -	C _D to Q o	- 0			*****	15	5.0	5.0		325	600	ns
11030111	opagation	Delay -	CD to do	10000.0±			tPLH,	10	3.0	10	{eps	90	225	O IIIS
							tPHL	- 1	Cin	15	_	60	170	O rue
								1000	10	5.0		1000	170	niV)
								1000	agi	10	(gaiv	300	Curren	ns
							1	10	24	15	_	250	186 kaga l	
Potrioss	-		- 00	810.0		- 09		15	E0.	-	0	200	-	-
Retrigge	r Time					20	trr	15	5.0	5.0	0	3/13/1	1 Curren	ns
		-				40	- 1	10	- Ga	15	0	-	leggs and	1093
							- 1	200	10		0	_		
			-				01-1	1000	10	5.0	0	inervo	vianus	ns
				SciVippi + sireuit), Cr.			(2) TI		1	10	0	3) emet	d Caper	10101
				de, f in kH		in fit switchis	1		-	15	0	-	of large	100
			a warding of 5	111 111 1 1010						L'IX31		Min		
, art														
, art	Timing R						RX	-	-	-	5.0	1000	1000	kΩ

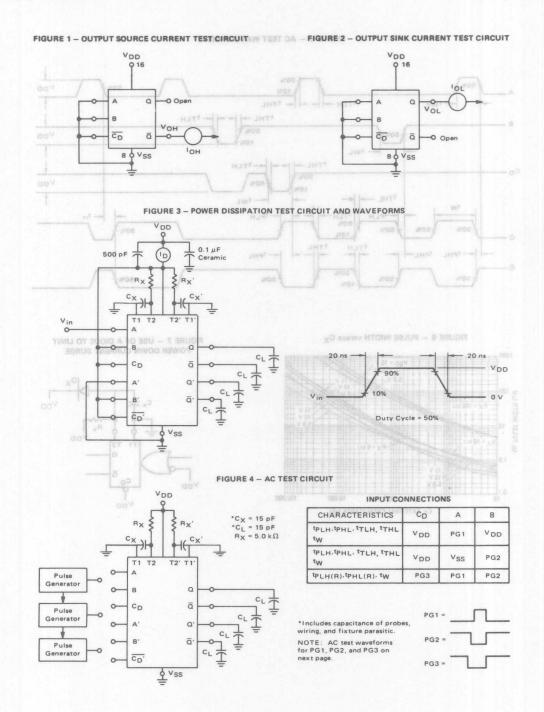
^{**} The formulae given are for the typical characteristics only.

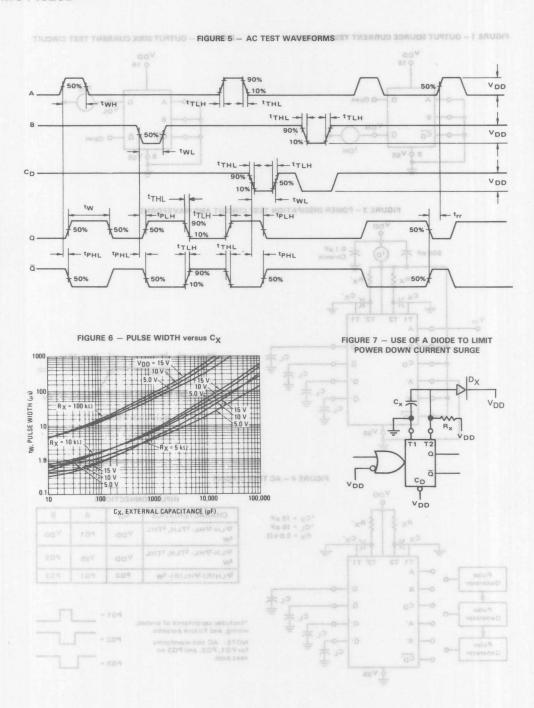
PIN ASSIGNMENT

SAV 91 - GOV 9 ALM SAV FUNCTION TABLE

at 25°C.	Inputs	the typical cha	of ore of Out	puts
Reset	А	В	Q	ā
H	_ L	7	Y	J.
H	√, ∼	2.7		iggered iggered
H	L, H, _	H L, H, √		iggered iggered
25	X	X	L Not Tri	H iggered

 ^{**} The formulae given are for the typical characteristics only.
 † R_X is in Ohms, C_X is in farads, V_{DD} and V_{SS} in volts, PW_{out} in seconds.
 * If C_X > 15 μF, Use Discharge Protection Diode D_X, per Fig. 7.





NC14529B



DUAL 4-CHANNEL ANALOG DATA SELECTOR

The MC14529B analog data selector is a dual 4-channel or single 8-channel device depending on the input coding. The device is suitable for digital as well as analog application, including various oneof-four and one-of-eight data selector functions. Since the device has bidirectional analog characteristics it can also be used as a dual binary to 1-of-4 or a binary to 1-of-8 decoder.

- Data Paths Are Bidirectional
 - Quiescent Current = 1.0 nA/package typical @ 5.0 Vdc
 - 10-MHz Operation (typical)
 - 3-State Outputs

φ = Don't Care

- Linear "On" Resistance
- "On" Resistance 120 Ohms typical @ 15 V
- Low Noise 12 nV/√ Cycle, f ≥ 1 kHz typical
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range

MAXIMUM RATINGS (Voltages referenced to Voc.)

Rating	Symbol	Value	Unit
DC Supply Voltage	VDD	-0.5 to +18	Vdc
Input Voltage, All Inputs	Vin	-0.5 to V _{DD} + 0.5	Vdc
DC Current Drain per Pin	1	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	TA	-55 to +125 -40 to +85	°C
Storage Temperature Range	T _{stg}	-65 to +150	оС

00 15 - 072 081 TRUTH TABLE 0

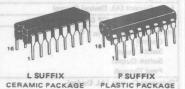
		- DRC	1 180	2333			
		- W 000	arz	AZO	В	STY	STX
		YO	X0	0	0	1	10
-Channel Mode	Dual 4-	Y1	X1	1	0	1	1
outs	2 Outp	Y2	X2	0	1	1	1
		Y3	X3	1	1	1	1
		0	>	0	0	0	.1
		4 019	190	089	0	0	1
8-Channel Mode	Single 8	2- 089	186	0	-1	0	1
	1 Outp	3 089	160	000	_1	0	1
and W tied togeth		00	120	0	_0	cust	0
	10 -	1 014	180	- 1	0	1	0
		2		0	1	1	0
	-	3	180	1	1	1	0 .
0		gh dance		φ	φ	0	0

This device contains circuitry to protect the control inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit. A destructive high-current mode may occur if Vin or Vout is not constrained to the range VSS. ≤ Vin or Vout ≤ VDD.

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

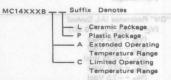
DUAL 4-CHANNEL ANALOG DATA SELECTOR OR 8-CHANNEL ANALOG DATA SELECTOR



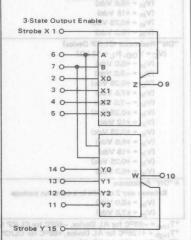
CASE 620

CASE 648

ORDERING INFORMATION



BLOCK DIAGRAM



VDD = Pin 16 VSS = Pin 8

together)

Cheracteristic		Figure	Symbol	VSS	VDD	Tlo	w°		25°C		Th	igh*	Unit
C. reli do fer la re				Vdc	Vdc	Min	Max	Min	Тур	Max	Min	Max	
Output Voltage "0" Level	7.1	1	VOL	0.0	5.0	-	0.05	-	0	0.05	-	0.05	Vdc
V _{in} = V _{DD} or 0		100	BOT:	BUE	10	ACI :	0.05	MAA.	130 //	0.05	LAG	0.05	
Table 20013			1		15	-	0.05	-	0	0.05	-	0.05	
TORK COMMO	1" Level	elo	Voh	0.0	5.0	4.95	10-19	4.95	5.0	5228	4.95	e:47	Vdc
LOW-POWER COMPLEMENTARY MOSI		-7/4		ab ac	10	9.95		9.95	10	b wol	9.95	meto	8
Vin = 0 or VDD		-318	S 21 SUIT	30 50	15	14.95	All Total	14.95	15	are la	14.95	ol-ole	
1 . 1/ 1/ //	'0" Level	2	VIL	0.0	100 1	1110121	in tot	sales o	tols trania	\$0-s0	o bos	nemat.	Vdc
(V _O = 4.5 or 0.5 Vdc)	0 20001	200		2112.00	5.0	noiton	1.5	Hanes a	2.25	1.5	hmoi	1.5	
(V==00==10Vd=)		lau	98 B O	nsed	10	de Tre	3.0	132110	4.50	3.0	1003.446.	3.0	
(Vo = 13 5 or 1 5 Vdc)					15	roder.	4.0	o-Fo	6.75	4.0	0-T 0	4.0	0
	'1" Level		VIH	0.0	5.0	3.5	-	3.5	2.75		3.5	1 3	Vdc
(V _O = 1.0 or 9.0 Vdc)	1 50001		AIH	0.0	10	7.0		7.0	5.50	91A	7.0	Usta	
(V _O = 1.5 or 13.5 Vdc)				nbV 4	15	11V	sossi	11	8.25	Curre	111	Quie	0
		-	1	0.0	15	-	±0.1	-(1)	±0.00001	±0.1	O+H	±1.0	μAdc
Input Current (AL Device) Control	-11		lin		-			1 1 1		-	-		#Adc
Input Current (CL/CP Device) Control	-	-	lin	0.0	15	-	±0.3	-	±0.00001	±0.3	(C) est	±1.0	
Input Capacitance (Vin = 0)		1	Cin	0.0					istance	BB "	10" 16	Line	pF
Control					-	Var	S feed	DVI 20	5.0	7.5	Resi	aD"	100
Switch Input					-		20	1000				T.	
Switch Output		1			IEDI	42.176	NTS	ole, f	0.3	12	Naise	WILL	100
Feed Through				-	_	obV S	010	WO.	The Marketon St.	00001	W 40	0.00	10
Quiescent Current (AL Device)	3	3	IDD		5.0	I LTT	1.0	-	0.001	1.0	o sid	60	μAdc
(Per Package)		769	Rod-wo-	SnC	10		1.0	0-1W0-	0.002	1.0	10/17	60	
		-18	gms T b	Hate	15	O abs	2.0	H DW	0.003	2.0	-	120	
Quiescent Current (CL/CP Device)		3	IDD	-	5.0	-	5.0	-	0.001	5.0	ouen.	70	μAdc
(Per Package)	11		-		10	-	5.0	-	0.002	5.0	-	70	
CHAXXXB Suffix Danstes	VI.				15	-	10	-	0.003	10	-	140	
"ON" Resistance (AL Device)	-	4,5,6	RON			1.85	A 01.0	eonare	B1 SHEET HO	77 60	11117	A INC	Ohms
$(V_C = V_{DD}, R_L = 10 k\Omega)$		tints	1	HsV		tonin y				Dustus.			
(V _{in} = +5.0 Vdc)	11	obV	81+	-5.0	5.0	QQ.V	400	-	200	480	7006	640	gqu2
$(V_{in} = -5.0 \text{ Vdc})$		Vda	8.0 + 6	aV or	8.0-	nīV.	400	-	200	480	ggT II/	640	oV tue
(Vin = ±0.25 Vdc)		o.Am	-	01			400	-	190	480	180 0	640	Curre
$(V_{in} = +7.5 \text{ Vdc})$		00	128	-7.5	7.5	-7	240	Spin	160	270	101516	400	PITATE
(Vin = -7.5 Vdc)			284	07 04		-	240	Bon	120	270	_	400	
(V _{in} = ±0.25 Vdc)		30	1		10	-	400	-	180	480	-	640	Fenery
(V _{in} = +10 Vdc) (V _{in} = +0.25 Vdc)	-11	3"	160	000	10	Big	400	_	180	480	o stuss	640	oliant
(V _{in} = +5.6 Vdc)							400		220	480	_	640	
(V _{in} = +15 Vdc)				0	15		250	-	180	270	_	400	
(Vin = +0.25 Vdc)						_ =	250	PI S CON	180	270	_	400	
(Vin = +9.3 Vdc) O 1 X sdor3		1			- 3	_	250	W -	215	270	8-	400	STX
"ON" Resistance (CL/CP Device)		4,5,6	RON				1	V	000	0	0		Ohms
$(V_C = V_{DD}, R_L = 10 \text{ k}\Omega)$		1,0,0	obal.	ennari	D-9-15:	(C.		y	77%	111	0	1	7
(Vin = +5.0 Vdc)	-11			-5.0	5.0	2	410	Y _	200	480	15-1	560	15
$(V_1 = -6.0 \text{ V/do})$	-11			0.0		-	410	1	200	480	0	560	-
(V _{in} = +0.25 Vdc)						_	410	-93	190	480	0-	560	1
(Vin = +7.5 Vdc)			stoM h	-7.5	7.5	12 -	250	00	160	270	7-	350	1
(Vin = -7.5 Vdc)	11		2000	1	Dutpu	1 -	250	50	160	270	1-	350	1
(Vin = ±0.25 Vdc)	11	-(3)	ditaget b	de W. ti	(Z 20)	-	250	_0	120	270	0	350	0
(Vin = +10 Vdc)		12		0	10	-	410	-0	180	480	10-	560	0
(Vin = +0.25 Vdc)	1					-	410	-81	180	480	-	560	0
(Vin = +5.6 Vdc)						-	410	To	220	480	-	560	-
(Vin = +15 Vdc)	11			0	15	-	250	son-bi	180	270	9-	350	0
(Vin = +0.25 Vdc)						-	250	-	180	270	-	350	
(Vin = +9.3 Vdc)					100	-	250	-	215	270	-57	350	0 = 0
Δ"ON" Resistance	L		ARON								-	-	Ohms
Between any 2 circuits in a common packag	9		- Old	-				-	-		-	-	-
(Vin = ±5.0 Vdc)			-	-5.0	5.0	-	-	-	15	-	-	-	
(Vin = ±7.5 Vdc)	8 8	155.000	A DESCRIPTION	-7.5	7.5	mi lem	occord	10000	010	00im 21	100000	and a	This !

⁽V_{In} = ±7.5 Vdc)

*T_{IOW} = -55°C for AL Device, -40°C for CL/CP Device

*T_{IOIS} = +125°C for AL Device, +85°C for CL/CP Device.

#Noise immunity specified for worst-case input combination.

Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc

2.0 Vdc min @ V_{DD} = 10 Vdc

2.5 Vdc min @ V_{DD} = 15 Vdc

					Typical	Maxi	imum	
Characteristic	Figure	Symbol	VSS	VDD	All Types	AL Device	CL/CP Device	Unit
Vin to Vout Propagation Delay Time	7	tPLH,tPHL	0.0	5.0	20	40	60	ns
$(C_L = 50 pF, R_L = 1.0 k\Omega)$				10	10	20	30	14
	× T3 -4	-4		15	8.0	15	25	
Propagation Delay Time, Control to	8	tPHL,tPLH	0.0	5.0	200	400	600	ns
Output, Vin = VDD or VSS	Alex			10	80	160	240	
(V _{in} ≤ 10 Vdc, C _L = 50 pF,	8	N.N.		15	50	120	180	
$R_L = 1.0 k\Omega$)	0 100				(V)		88V	
Crosstalk, Control to Output	9	7 -	0.0	5.0	5.0	-	-	mV
$(C_L = 50 pF, R_L = 1.0 k\Omega)$	EY La	-0		10	5.0	-	-	13.00
$R_{out} = 10 k\Omega$				15	5.0	alV O	V88_= 0.0	
Maximum Control Input	10	J -	0.0	5.0	5.0	-	-	MHz
Pulse Frequency				10	10	-	-	
(C _L = 50 pF, R _L = 1.0 kΩ)	3			15	12	-	-	
Noise Voltage pre cr.sr.a.c.s and	11,12	-	0.0	5.0	24 .	-	-	nV/√Cycl
(f = 100 Hz)				10	25	_	-	
				15	30	_	_	
(f = 100 kHz)		bin in		5.0	12	_		
	8-4E	RIGUR		10	12		IUD - E BRUI	19
THEOREM TEST	7			15	15	IST CINCUIT	-	
Sine Wave (Distortion)	-	-						%
(V _{in} = 1.77 Vdc RMS			-5.0	5.0	0.36	9	agV yT8	XIR
Centered @ 0.0 Vdc,							B 19 15	
$R_L = 10 \text{ k}\Omega$, $f = 1.0 \text{ kHz}$						1		
Input/Output Leakage Current	-	-				4		nA
	N. PAGE					01)		
(Vin = +5.0 Vdc, Vout = -5.0 Vdc)		11 -2 74 11	-5.0	5.0	±0.001	±125	±125	
(Vin = -5.0 Vdc, Vout = +5.0 Vdc)			-5.0	5.0	±0.001	±125	±125	11 33
(Vin = +7.5 Vdc, Vout = -7.5 Vdc)	- asv		-7.5	7.5	±0.0015	±250	±250	1119
$(V_{in} = -7.5 \text{ Vdc}, V_{out} = +7.5 \text{ Vdc})$			-7.5	7.5	±0.0015	±250	±250	
Insertion Loss	-	-				100-100-1		dB
(V _{in} = 1.77 Vdc	1 1 1 1		-5.0	5.0		PA,0A	10	D remed
RMS centered @ 0.0 Vdc,						T	- bearing	
f = 1.0 MHz,						\$28V		
I _{loss} = 20 Log ₁₀ Vout						+	Veckle	" a3
Vin	100							
$(R_L = 1.0 k\Omega)$	W- 14.3				2.0	-	-	
$(R_L = 10 k\Omega)$		045 1007	COMP access		0.8	-	-	
$(R_L = 100 k\Omega)$		DALTON	- Inter departs	CAL RON	0.25	-	-	
(R _L = 1.0 MΩ) a 3.9Up/3					0.01	F1G14918.5.	-	
Bandwidth (-3 dB)	-	BW	-5.0	5.0				MHz
(V _{in} = 1.77 Vdc								
RMS centered @ 0.0 Vdc)								
(R _L = 1.0 kΩ) V0 = ggV		00	100	V 2 =		-	N	200
$(R_L = 10 k\Omega)$			è	V2- =	28	7-	-	
(R _L = 100 kΩ)			833 533	Von = 7.5 V	27	-	1	
(R _L = 1.0 MΩ)		108	2	A 0'4 - 0'0's	26			180
Feedthrough and Crosstalk	-/	-	-5.0	5.0		1		kHz
(20 Log10 Vout = -50 dB)	-		100					1000
Vin		00	186					
$(R_L = 1.0 k\Omega)$	-	-	1		850	-	-	
$(R_L = 10 \text{ k}\Omega)$		no.	20 20 20 20 20 20 20 20 20 20 20 20 20 2		100	_		43
$(R_L = 100 \text{ k}\Omega)$		100			12	_	_	
$(R_L = 1.0 M\Omega)$					1.5	-		
	-							

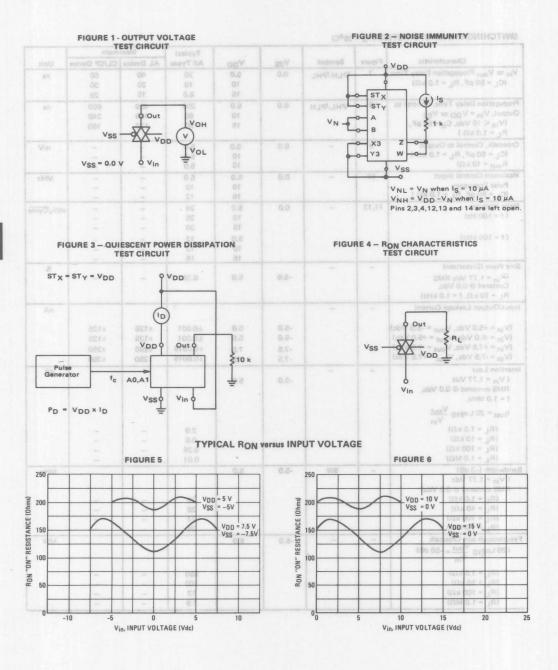


FIGURE 7 - PROPAGATION DELAY TEST CIRCUIT AND WAVEFORMS

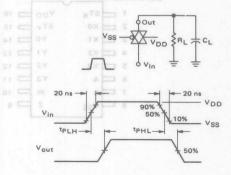


FIGURE 9 - CROSSTALK TEST CIRCUIT

FIGURE 8 - TURN-ON DELAY TIME TEST CIRCUIT AND WAVEFORMS

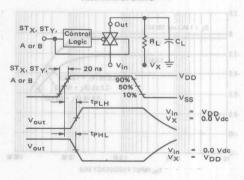


FIGURE 10 - FREQUENCY RESPONSE TEST CIRCUIT

I VSS

VFeedthrough Input

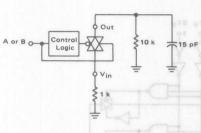


FIGURE 11 - NOISE VOLTAGE TEST CIRCUIT

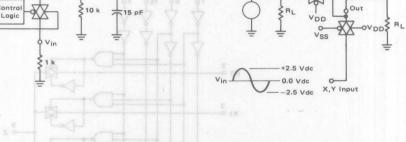


FIGURE 12 - TYPICAL NOISE CHARACTERISTICS

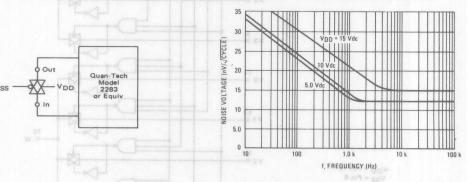
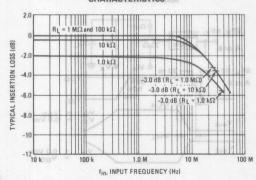
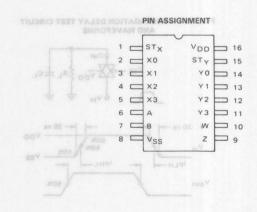
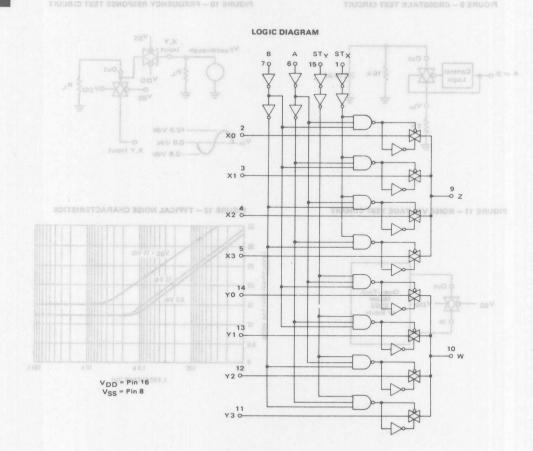


FIGURE 13 – TYPICAL INSERTION LOSS/BANDWIDTH CHARACTERISTICS





3





DUAL 5-INPUT MAJORITY LOGIC GATE

The MC14530B dual five-input majority logic gate is constructed with P-channel and N-channel enhancement mode devices in a single monolithic structure. Combinational and sequential logic expressions are easily implemented with the majority logic gate, often resulting in fewer components than obtainable with the more basic gates. This device can also provide numerous logic functions by using the W and some of the logic (A thru E) inputs as control inputs.

- Single Supply Operation Positive or Negative
- Quiescent Current = 0.5 nA/package typical @ 5 Vdc
- Input Impedance = 10¹² ohms typical
- High Fanout > 50
- Diode Protection on Inputs
- Noise Immunity = 45% of VDD typical
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range

MAXIMUM RATINGS (Voltages referenced to VSS)

The state of the s	E 00 00	and the second s	frankliker i de la servicio della servicio de la servicio della se	
Rating	Symbol	Value	Unit	
DC Supply Voltage	V _{DD}	-0.5 to +18	Vdc	
Input Voltage, All Inputs	Vin	-0.5 to V _{DD} + 0.5	Vdc	
DC Current Drain per Pin		10	mAdc	
Operating Temperature Range - AL Device CL/CP Device	TA_	-55 to +125 -40 to +85	°C	
Storage Temperature Range	T _{stg}	-65 to +150	°C	

LOGIC TABLE

INPUTS A B C D E	W	Z
For all combinations of inputs where three	0	1
or more inputs are logical "0".	- 1	0
For all combinations of inputs where three	0	0
or more inputs are logical "1".	1	1

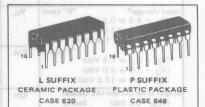
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, it is recommended that Vin and Vout be constrained to the range VSS < (Vin or Vout) < VDD.

Unused inputs must be tied to an appropriate logic level (e.g., VSS or VDD).

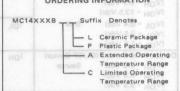
CMOS SSI

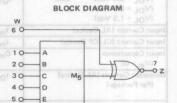
(LOW-POWER COMPLEMENTARY MOS)

DUAL 5-INPUT MAJORITY LOGIC GATE



ORDERING INFORMATION





°M₅ is a logical "1" if any three or more inputs are logical "1".

⊕ ≡ Exclusive NOR ≡ Exclusive OR

TRUTH TABLE

11110		
M ₅	W	Z
0	0	1
0	1	0
1	0	. 0
1	1	1

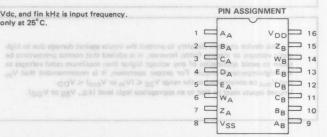
V_{DD} = Pin 16 V_{SS} = Pin 8

122 2080		VDD	Tic	w*		25°C		Th	igh *	
Characteristic	Symbol	Vdc	Min	Max	Min	Тур	Max	Min	Max	Unit
Output Voltage "0" Level	VOL	5.0	-	0.05	-	0	0.05	-	0.05	Vdc
Vin = VDD or 0		10	-	0.05	-	0	0.05	-	0.05	
UAL SUMPUT MAJORITY	9	15	-	0.05	-	0	0.05	-	0.05	
"1" Level	VOH	5.0	4.95	TAD S	4.95	5.0	MA-TUP	4.95	AUR	Vdc
Vin = 0 or VDD	011	10	9.95	-	9.95	10	-	9.95	-	
		15	14.95	to all other	14.95	15	·	14.95	IAT THE	T.
Input Voltage# "0" Level	VIL						1	10 6000		Vdc
$(V_0 = 4.5 \text{ or } 0.5 \text{ Vdc})$	"-	5.0	gnie s ni	1.2	bom in	2.25	1.25	-VI bns	1.15	115335
$(V_0 = 9.0 \text{ or } 1.0 \text{ Vdc})$	Sin.	10	polssend)	2.5	ineupe	4.50	2.5	normer of	2.4	mont
$(V_0 = 13.5 \text{ or } 1.5 \text{ Vdc})$		15	milliuzer	3.0	se signal	6.75	3.0	patrierna	2.9	0 970
"1" Level	VIH		111 /840 8	1 appen a	UP13 3010 3	TIVE SHOULD	STOR THE	U. SETTIMETU	dusine ras	(51) 149
$(V_O = 0.5 \text{ or } 4.5 \text{ Vdc})$	081	5.0	3.85	gniau y	3.75	2.75	ดาลุภามก	3.75	rele nab s	Vdc
$(V_0 = 1.0 \text{ or } 9.0 \text{ Vdc})$	1	10	7.6	npi <u>ut</u> s,	7.5	5.50	(3_und	7.5	of the	EGUJE .
$(V_0 = 1.5 \text{ or } 13.5 \text{ Vdc})$		15	12.1	-	12	8.25	-	12	_	
Output Drive Current (AL Device)	ГОН				evitages	10 Bylltian	9 - 001	E1BOD V	agu2 eine	mAdc
(V _{OH} = 2.5 Vdc) Source	·On	5.0	-3.0	-100	-2.4	-4.2	1-Aπ 2-O	-1.7		O 0
(V _{OH} = 4.6 Vdc)		5.0	-0.64	5 V de	-0.51	-0.88	DAM U.U	-0.36	O Misoson	m .
(V _{OH} = 9.5 Vdc)		10	-1.6	_	-1.3	-2.25	012_one	-0.9	sur imper	of e
(V _{OH} = 13.5 Vdc)		15	-4.2	-	-3.4	-8.8	_	-2.4	uor=3 di	O 1-11
(VOL = 0.4 Vdc) Sink	IOL	5.0	0.64	_	0.51	0.88		0.36	-	mAdc
(VOL = 0.5 Vdc)	IOL	10	1.6		1.3	2.25	arugol	0.9	etotal epo	MAGC
(V _{OL} = 1.5 Vdc)		15	4.2		3.4	8.8	V la &	2.4	ummi said	e No
Output Drive Current (CL/CP Device)	lau	10	7.2		30V	BT of shi	OFER	RaFi sps	IloV vice	mAdc
(V _{OH} = 2.5 Vdc) Source	ІОН	5.0	-2.5		-2.1				1000	17.10.11.11.1
(V _{OH} = 4.6 Vdc)		5.0	-0.52	J ono	-0.44	-4.2 -0.88	WO LOW	-1.7 -0.36	to Bldsq	0 9
(V _{OH} = 9.5 Vdc)	1	10	-1.3	he Hated	-1.1	-2.25	039 (10	-0.36	T yoursey	68
(V _{OH} = 13.5 Vdc)	-	15	-3.6	_	-3.0	-8.8		-0.9	egns.Fi-en	ds
	-		-		-	-		-		- 0.1
(V _{OL} = 0.4 Vdc) Sink (V _{OL} = 0.5 Vdc)	IOL	5.0	0.52		0.44	0.88	-	0.36	-	mAdc
		15	3.6		3.0	8.8	igus ratori	2.4	MITARIA	UMHX
(V _{OL} = 1.5 Vdc)	W	1 11331	3.0	Water	3.0					
nput Current (AL Device)	lin	15	0.0	± 0.1	T. Comb	±0.00001	±0.1	-	± 1.0	μAdc
nput Current (CL/CP Device)	lin	15	20.00	± 0.3	-	±0.00001	± 0.3	-	±1.0	μAdc
nput Capacitance	Cin	m Aute	1		1	5.0	7.5	-	-	pF
(V _{in} = 0)	2.0			121					Drain per	100200
Quiescent Current (AL Device)	OG IDD	5.0	- 03/1	0.25	1 -A*	0.0005	0.25	- admin	7.5	μAdc
(Per Package)	40	10	_ 88	0.50		0.0010	0.50	70_	15	
		15	150 -	1.00	Total T	0.0015	1.00	-10 m	30	neT see
Quiescent Current (CL/CP Device)	IDD	5.0	-	1.0	-	0.0005	1.0	-	7.5	иAdc
(Per Package)		10	-	2.0	-	0.0010	2.0	_	15	A.130
CA * Mg W W = (ADC+ADS+RCD+RCD+RCD		15	-	4.0	-	0.0015	4.0	-	30	
Total Supply Current**†	IT	5.0	-		1 10		1611	-		μAdc
	9.6	10				.75 µA/kHz				μAdc
D D11	001	15				.50 μA/kHz				
(C _L = 50 pF on all outputs, all		10			T = (2	.25 μA/kHz				
buffers switching)	2.11	1 1								

*Tlow = -55°C for AL Device, -40°C for CL/CP Device.

Thigh = +125°C for AL Device, +85°C for CL/CP Device. #Noise immunity specified for worst-case input combination. Standard family noise margin

specification is met for any one input tested at a time.

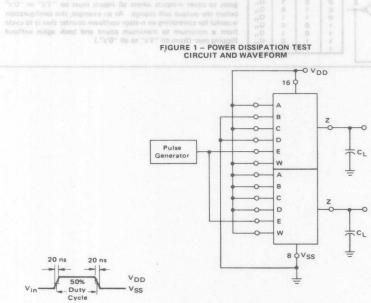


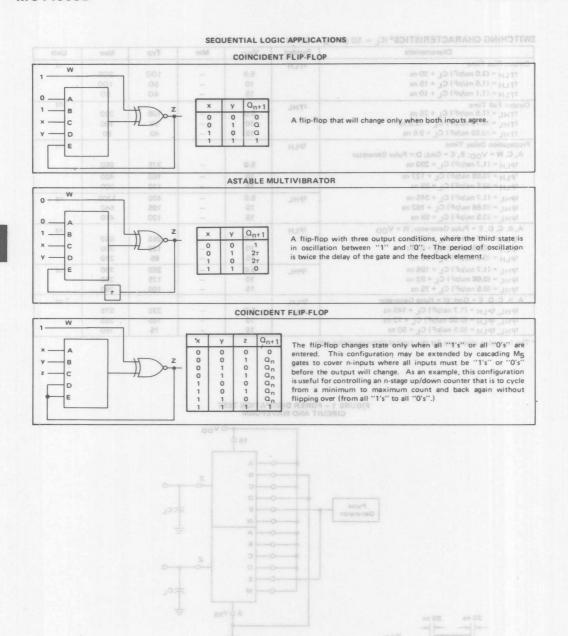
†To calculate total supply current at loads other than 50 pF: $\frac{1}{17}(C_L) = \frac{1}{17}(50 \text{ pF}) + 2 \times 10^{-3} (C_L - 50) \text{ VDDf}$ where: $\frac{1}{17}$ is in μ A (per package), C_L in pF, VDD in Vdc, and fin kHz is input frequency. "The formulas given are for the typical characteristics only at 25°C.

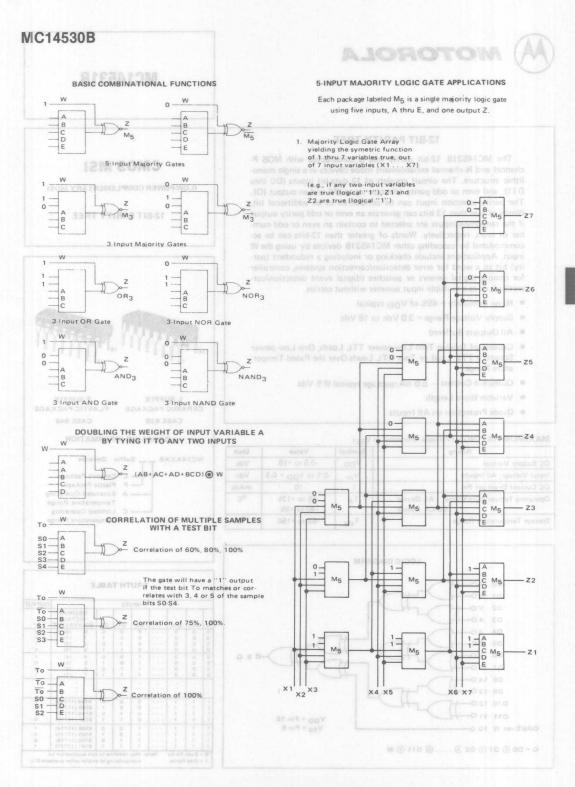
SWITCHING CHARACTERISTICS*	(CL =	= 50 pF,	TA	25°C)
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Characteristic	Symbol	VDD	Min	Тур	Max	Unit
Output Rise Time	tTLH			-		ns
tTLH = (3.0 ns/pF) CL + 30 ns		5.0	-	100	200	1
t _{TLH} = (1.5 ns/pF) C _L + 15 ns		10	-	50	100	
tTLH = (1.1 ns/pF) CL + 10 ns		15	_	40	80	
Output Fall Time	tTHL	THID Y	. 20	2 21		ns
t _{THL} = (1.5 ns/pF) C _L + 25 ns	10 -010 0	5.0	0-1 -	100	200	0
t _{THL} = (0.75 ns/pF) C _L + 12.5 ns	H-gill A	010	0-	50	100	3
t _{THL} = (0.55 ns/pF) C _L + 9.5 ns		15 8	1-1	40	80	O Prime
ropagation Delay Time	tPLH					ns
A, C, W = V _{DD} ; B, E = Gnd; D = Pulse Generator						-
tpLH = (1.7 ns/pF) CL + 290 ns		5.0	-	375	960	-
^t _{PLH} = (0.66 ns/pF) C _L + 127 ns	ARBIVITJU	10	-	160	400	
tpLH = (0.5 ns/pF) CL + 85 ns	AMBIVITIO	15		110	300	
tpHL = (1.7 ns/pF) CL + 345 ns	tPHL	5.0	_	430	1200	ns
tpHL = (0.66 ns/pF) CL + 162 ns		10	_	195	540	
tpHL = (0.5 ns/pF) CL + 95 ns		15	-	120	410	
A, B, C, D, E = Pulse Generator; W = VDD	tPLH	E KI	7	5		ns
tpLH = (1.7 ns/pF) CL + 170 ns	II-qift A	5.0	4-0-1	255	640	9
tpLH = (0.66 ns/pF) CL + 87 ns		10	1 2-1	120	300	1 0
tpLH = (0.5 ns/pF) CL + 60 ns	Anned al	15	1 7-1	85	210	0
tpHL = (1.7 ns/pF) CL + 195 ns	tPHL	5.0	1 1-1	280	750	ns
tpHL = (0.66 ns/pF) CL + 92 ns		10	-	125	330	-
tpHL = (0.5 ns/pF) CL + 75 ns		15	-	100	250	
A, B, C, D, E = Gnd; W = Pulse Generator	tPLH.				Lund	ns
tpHL, tpLH = (1.7 ns/pF) CL + 145 ns	tPHL THE	5.0	-	230	575	,
tpHL, tpLH = (0.66 ns/pF) CL + 72 ns		10	-	105	265	100
tpHL, tpLH = (0.5 ns/pF) CL + 50 ns		15	-	75	190	

^{*} The formulae given are for the typical characteristics only,







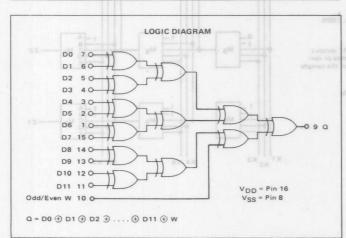
12-BIT PARITY TREE

The MC14531B 12-bit parity tree is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. The circuit consists of 12 data-bit inputs (D0 thru D11), and even or odd parity selection input (W) and an output (Q). The parity selection input can be considered as an additional bit. Words of less than 13 bits can generate an even or odd parity output if the remaining inputs are selected to contain an even or odd number of ones, respectively. Words of greater than 12-bits can be accommodated by cascading other MC14531B devices by using the Winput. Applications include checking or including a redundant (parity) bit to a word for error detection/correction systems, controller for remote digital sensors or switches (digital event detection/correction), or as a multiple input summer without carries.

- Noise Immunity = 45% of Vpp typical
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range
- Quiescent Current 5.0 nA/package typical @ 5 Vdc
- Variable Word Length
- Diode Protection on All Inputs

MAXIMUM RATINGS (Voltages referenced to VSS)

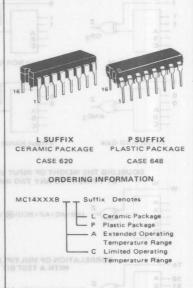
Rating	Symbol	Value	Unit	
DÇ Supply Voltage	V _{DD}	-0.5 to +18	Vdc	
Input Voltage, All Inputs	Vin	-0.5 to V _{DD} + 0.5	Vdc	
DC Current Drain per Pin		10	mAdc	
Operating Temperature Range AL Device CL/CP Device	TA	-55 to +125 -40 to +85	°C	
Storage Temperature Range	T _{stg}	-65 to +150	°C	



CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

12-BIT PARITY TREE



-			99183 03.35		UTS		-	ОИТРИТ
w	D11	D10). tz 10	D2	D1	DO	DECIMAL (OCTAL) EQUIVALENT	0.
0	0	0		0	0	0	0 (0)	0
0	0	0		0	0	1	1 (1)	501
0	0	0		0	1	0	2 (2)	1
0	0	0		0	1	1	3 (3)	0
0	0	0		1	0	0	4 (4)	1
0	0	0		1	0	1	5 (5)	0
0	0	0		1	1	0	6 (6)	0
0	0	0		1	1	1	7 (7)	1
							. A-	- 07
			2.55		5.	-	8-	- 55
	9800	Lie o	bileb	3300		. 11		
1	1	1		0	0	0	8184 (17770)	0
1	1	.1		0	0	1	8185 (17771)	1
1	1	1		0	1	0	8186 (17772)	- 53
1	1	1		0	1	1	8187 (17773)	0
1	1	1		1	0	0	8188 (17774)	1
1	1	1		1	0	1	8189 (17775)	0
1	1	1		- 1	1	0	8190 (17776)	0
1	1	1		1	1	1	8191 (17777)	1

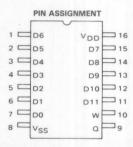
Mex Unit	Typ	18(5)(1	VDD	TI	ow*		25°C	pitzine)	Thi	gh°	
Characteristic		Symbol	Vdc	Min	Max	Min	Тур	Max	Min	Max	Unit
Output Voltage	"O" Level	VOL	5.0	-	0.05		0 '	0.05	+ JQ (9a)	0.05	Vdc
Vin VDD or 0	08 - 1		10	-	0.05	-	0	0.05	+ 1314d	0.05	UT!
08	40	-	15	-	0.05	-	0	0.05	+ 10 [Ro	0.05	NUTT.
	"1" Level	Vон	5.0	4.95	JHZ	4.95	5.0	_	4.95	ami_I no	Vdc
Vin Oor VDD	001	011	10	9.95	_	9.95	10	_2m 8	9.95	(an 8.11-	HT
Dor	08		15	14.95	-	14.95	15	18. <u>5</u> nt	14.95	= (0.75 x	HITT
Input Voltage#	"0" Level	VIL	- 0					BIX IQ. G	Po cardia	H CO,01	Vdc
(VO - 4.5 or 0.5 Vdc)		12	5.0	_	1.5	-	2.25	1.5	<u>a</u> m(7)	1.5	capaga
(VO = 9.0 or 1.0 Vdc)			10	-	3.0	-	4.50	3.0	-	3.0	Data to
(V _O = 13.5 or 1.5 Vdc)	840	-	15	-	4.0	-	6.75	4.0	Rolan C. P	4.0	R_(97
929	"1" Level	VIH	- 0				851.20	4 4 101	9100.00.0	* JH4	1,191
(VO = 0.5 or 4.5 Vdc)	120	-1111	5.0	3.5		3.5	2.75	56 T 73	3.5	EH41	Vdc
(VO = 1.0 or 9.0 Vdc)			10	7.0	_	7.0	5.50	_	7.0	O or na	Tube
(V _O = 1.5 or 13.5 Vdc)	250	-	15	11.0	_	11.0	8.25	GL + 16	11.0	= 11197	1,197
Output Drive Current (AL D	evice)	ІОН	- 0	1		11.0	0.20	9+194	-	37177	mAdc
	Source	.Он	5.0		_		80	56+33	O.5 ns/pif	T.JH97	8,197
(V _{OH} = 4.6 Vdc)			5.0	-3.0	- 4	-2.4	-4.2	piq <u>v</u> z eris	-1.7	ulac_give	real error
(VOH = 9.5 Vdc)			10	-0.64 -1.6		-0.51 -1.3	-0.88 -2.25		-0.36 -0.9	_	
(VOH = 13.5 Vdc)		1.0	15	-4.2	_	-3.4	-8.8		-0.9	_	
0.1	Sink	In.	5.0	0.64	-	0.51	0.88	_	0.36	_	mAdc
(VOL = 0.5 Vdc)	DITIK	IOL	10	1.6		1.3	2.25	_	0.30		MAGC
$(V_{OL} = 0.5 \text{ Vdc})$			15	4.2		3.4	8.8		2.4		
			15	4.2	-	3.4	0.0		2.4		
Output Drive Current (CL/C		ІОН									mAdc
011	Source		5.0	-2.5	-	-2.1	-4.2		-1.7		
$(V_{OH} = 4.6 \text{ Vdc})$			5.0	-0.52	-	-0.44	-0.88		-0.36	-	
(V _{OH} = 9.5 Vdc)			10	-3.6	-	$\begin{vmatrix} -1.1 \\ -3.0 \end{vmatrix}$	-2.25 -8.8	-	-0.9 -2.4	-	
(V _{OH} = 13.5 Vdc)			15	-	-	-					-
OF	Sink	OL	5.0	0.52	-	0.44	0.88	-	0.36	-	mAdc
$(V_{OL} = 0.5 \text{ Vdc})$			10	1.3	-	1.1	2.25	-	0.9	-	
(V _{OL} = 1.5 Vdc)			15	3.6	-	3.0	8.8	-	2.4		
Input Current (AL Device)		lin	15	-	± 0.1	-	±0.00001	± 0.1	_	± 1.0	μAdc
Input Current (CL/CP Device	e)	lin	15	-	± 0.3		±0.00001	± 0.3	-	±1.0	μAdc
Input Capacitance		Cin	-		-		5.0	7.5	-	-	pF
(V _{in} = 0)		9		WER DIS	IAMINC PO	YO - F	FIGURE				
Quiescent Current (AL Devi	ce)	IDD	5.0	MBORE	5.0	28161	0.005	5.0	-	150	μAdc
(Per Package)		00	10	-	10	-	0.010	10	-	300	
			15	20-20	20		0.015	20	-	600	
Quiescent Current (CL/CP [Device)	IDD	5.0	-	20	arae 1	0.005	20	-	150	μAdc
(Per Package)		00	10	-17	40	5606 £	0.010	40		300	
	94.1		15	-	80	201	0.015	80	_	600	
Total Supply Current**†		IT	5.0			1= : (0	.25 µA/kHz	1111		000	μAdc
(Dynamic plus Quiescen			10			IT = (0	.25 μΑ/κΗz) f + Ico			μΑσο
Per Package)			15				.75 µA/kHz				
(C ₁ = 50 pF on all outpu	its all		13	136.			.73 40/6112				
buffers switching)	,			Noale m		eigent mich					

tTo calculate total supply current at loads other than 50 pF:

I_T(C_L) = I_T(50 pF) + 1 x 10⁻³ (C_L -50) V_{DD}

where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.

*The formulas given are for the typical characteristics only at 25°C.



^{*}Tlow = -55°C for AL Device, -40°C for CL/CP Device.

Thigh = +125°C for AL Device, +85°C for CL/CP Device.

=Noise immunity specified for worst-case input combination.

Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc

2.0 Vdc min @ V_{DD} = 10 Vdc

2.5 Vdc min @ V_{DD} = 15 Vdc

To calculate total supply current at leads other than 50 05.

WITCHING CHARACTERISTICS*	(CL =	50 pF, TA	= 25°C)			CLEBIRATIC	AL CHARA	ELECTRIC
Characteristic	25°c		Symbol	VDD	Min	Тур	Max	Unit
Output Rise Time	ay T	nifē	tTLH	Vdc Mile	Tedmy2		Characteristic	ns
tTLH = (3.0 ns/pF) CL + 30 ns			80.0	5.0	ToV	100	200	Sulpur Voite
tTLH = (1.5 ns/pF) CL + 15 ns			0.05	10	-	50	100	OV NV
tTLH = (1.1 ns/pF) CL + 10 ns			80.0	15	-	40	80	
Output Fall Time	8.0	4.95	tTHL	50 1 495	HOV	- Impost 2 to		ns
tTHL - (1.5 ns/pF) CL + 25 ns				5.0	The state of	100	200	00 aV
t _{THL} = (0.75 ns/pF) C _L + 12.5 ns				10	-	50	100	
t _{THL} = (0.55 ns/pF) C _L + 9.5 ns				15	5.V	40	80	werte V some
Propagation Delay Time			tPLH,	5.0			or 0.5 Vde)	ns ns
D-4- 4- 0			TPHL	- 01		1 1 1 1 1	(suV B.1 to	Corne to the same
tplH, tpHL = (1.7 ns/pF) CL + 355 ns			0.4	5.0	171 -	440	1220	(Vo - 13)
tpLH tpHL = (0.66 ns/pF) CL + 142	ns			10	- Tul	175	525	9
tpLH tpHL = (0.5 ns/pF) CL + 95 ns				15	1 2	120	360	20 - 00
Odd/Even to Q				10 7.0			or 9.0 Vdc)	
tpLH, tpHL = (1.7 ns/pF) CL + 165 ns	5			5.0	_	250	750	a.r = 0V7
tpLH tpHL = (0.66 ns/pF) CL + 67 ns				10		100	300	
tpLH, tpHL = (0.5 ns/pF) CL + 45 ns				15	HO.	70	210	ewinG zurgtes

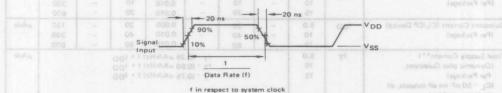
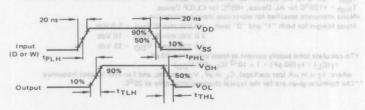


FIGURE 2 - DYNAMIC SIGNAL WAVEFORMS OF 10 100 DO 10







MC14532B

SEEST OF

8-BIT PRIORITY ENCODER

The MC14532B is constructed with complementary MOS (CMOS) enhancement mode devices. The primary function of a priority encoder is to provide a binary address for the active input with the highest priority. Eight data inputs (D0 thru D7) and an enable input (Ein) are provided. Five outputs are available, three are address outputs (Q0 thru Q2), one group select (GS) and one enable output (Eout).

- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- Noise Immunity = 45% of Vpp typical
- Diode Protection on All Inputs
- Low Input Capacitance 5.0 pF typical
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range

MAXIMUM RATINGS (Voltages referenced to VSS)

- Ra	ting	- 1	8.8	Symbol	Value 8.8	Unit
DC Supply Voltage	-	1.0 =	10000	V _{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	-	5.0.2	10000	Vin-	-0.5 to V _{DD} + 0.5	Vdc
DC Current Drain per Pin		7.8	5.0	1 -	- 10	mAdc
Operating Temperature R	lange	AL Device		TA	-55 to +125	°C
150 aAda	CL	/CP Device	800.		-40 to +85	0.8
Storage Temperature Ran	nge	10	010,	T _{stg}	-65 to +150	°C

TRUTH TABLE

		00		NPUT	- 0	8 1				DB	OUTPU	JT	
Ein	D7,	D6	D5	D4	D3	D2	D1	D0	GS	02	Q1	00	Eout
0	X 0	X 0	X 0	X 0	X	X	X 0	EXX 0	0	0	0	0	0
1	1 0	X 1.	×	×	×	×	. X	×	1	1	1	1 0	0
1	0	0	1 0	X 1	X	X	×	×	1 1	1	0	1 0	0
1	0	0	0	0	1 0	X	×	×	1	0	1	1 0	0
1	0	0	0	0	0	0	1	×	1	0	0 d	1	000
1	0	0	0	0	0	0	0	1	1	0	0	0	0

X = Don't Care

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leqslant (V_{in} \text{ or } V_{out}) \leqslant V_{DD}.$

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

8-BIT PRIORITY ENCODER

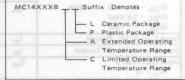


L SUFFIX
CERAMIC PACKAGE
CASE 620

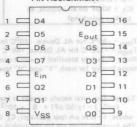
P SUFFIX
PLASTIC PACKAGE

CASE 648

ORDERING INFORMATION



PIN ASSIGNMENT



ľ	3	6	3
	С	9	4
Г	з	p	ч

		VDD	Tic	w*		25°C		Thi		
Characteristic	Symbol	Vdc	Min	Max	Min	Тур	Max	Min	Max	Unit
Output Voltage "0" Level	VOL	5.0	-	0.05	-	0	0.05	-	0.05	Vdc
V _{in} · V _{DD} or 0		10	-	0.05	-	0	0.05	-	0.05	-
		15	-	0.05	-	0	0.05	-	0.05	
"1" Level	VOH	5.0	4.95		4.95	5.0	OTES :	4.95	-	Vdc
Vin - 0 or VDD	Oil	10	9.95	- 7	9.95	10	HUMMIT !	9.95	-	
CMOS MSI		15	14.95	_	14.95	15	-	14.95	_	
Input Voltage# "0" Level	VIL		ON YO	Jinomoid	2100 10	W pathon	PERSON C	0200	*1:0/m = 01	Vdc
(V _O = 4.5 or 0.5 Vdc)	an - IL	5.0	15 5 10	1.5	primary	2.25	1.5	maman	1.5	MADI
(V _O = 9.0 or 1.0 Vdc)		10	rativ tuqu	3.0	ss for th	4.50	3.0	010_01 2	3.0	pritty
(V _O = 13.5 or 1.5 Vdc)		15	dans ne	4.0	usels O	6.75	4.0	ority. B	4.0	tise it
"1" Level	VIH	10	e addres	is sening :	Idelisvs	oto shugh	L Five o	epivoro	Pie Louis	ngni
(V _O = 0.5 or 4.5 Vdc)	VIH	5.0	3.5	dana ann	3.5	2.75	om spoi	3.5	ts (Q0 th	Vdc
(V _O = 1.0 or 9.0 Vdc)		10	7.0				100		- 6	0031
(VO = 1.5 or 13.5 Vdc)	-	15			7.0	5.50	_	7.0	- 4	0041
		15	11.0	-	11.0	8.25		11.0		
Output Drive Current (AL Device)	IOH			obV č	@ faoig	vackage IV	5.0 nA/	= 1097110	descent C	mAdc
(V _{OH} = 2.5 Vdc) Source		5.0	-3.0	-	-2.4	-4.2	-	-1.7	-	
(V _{OH} = 4.6 Vdc)	Re II	5.0	-0.64	-	-0.51	-0.88	IA TO SUS	-0.36	ammai seid	N O
(V _{OH} = 9.5 Vdc)		10	-1.6	-	-1.3	-2.25	All Topu	-0.9	ode Prote	0 0
(V _{OH} = 13.5 Vdc)		15	-4.2	-	-3.4	-8.8	-	-2.4	-	
(VOL = 0.4 Vdc) Sink	IOL	5.0	0.64	-	0.51	0.88	1.d = 90f	0.36	THOUSE W	mAdc
(VOL = 0.5 Vdc)		10	1.6	-	1.3	2.25	0.5 = 90	0.9	lo V-ylog	2.8
(VOL = 1.5 Vdc)		15	4.2	-	3.4	8.8	-	2.4	-	
Output Drive Current (CL/CP Device)	ЮН		tuod an	191018	7007 47	1 150000	WOLL CHI	GHIVING	to sides	mAdo
(VOH = 2.5 Vdc) Source	011	5.0	-2.5	the Raw	-2.1	-2.4	OWT 10	-1.7	hordsy T	20
(V _{OH} = 4.6 Vdc)		5.0	-0.52	_	-0.44	-0.88	_	-0.36	ure <u>Pl</u> ange	16
(V _{OH} = 9.5 Vdc)		10	-1.3	_	-1.1	-2.25	_	-0.9	_	
(V _{OH} = 13.5 Vdc)		15	-3.6	_	-3.0	-8.8	_	-2.4	_	1
(VOI = 0.4 Vdc) Sink	101	5.0	0.52		0.44	0.88		0.36		mAdo
(VOL = 0.5 Vdc)	IOL	10	1.3		1.1	2.25	malan sage	0.9	MITARIN	III AGC
(VOL = 1.5 Vdc)		15	3.6	ula\L	3.0	8.8		2.4		
		A CONTRACTOR OF THE PARTY OF TH	-	-			-	2.4		
nput Current (AL Device)	lin	15	- 871	± 0.1	-00	±0.00001	±0.1	-	± 1.0	μAdc
nput Current (CL/CP Device)	lin	15 V	30+6	± 0.3	- m	±0.00001	± 0.3	- 23	±1.0	μAdc
nput Capacitance	Cin	250		01 -	- 1	5.0	7.5	- 111	тик-патО	pF
(V _{in} = 0)			125	ot 23-	TA.		AL David	- apros A	mularadime	Tomas
Quiescent Current (AL Device)	IDD	5.0	- 88	5.0	1-	0.005	5.0	13-	150	μAdc
(Per Package)	.00	10	- 021	10	- T	0.010	10	-sgns	300	noT up
		15	- 00	20	835.	0.015	20		600	-100
Quiescent Current (CL/CP Device)	lee	5.0	1 -	20	_	0.005	20	_		۸ -1 -
No. of the second of the control of the second of the seco	IDD	10		20		0.003			150	μAdc
(Per Package)		15	-	40	-	0.010	80	-	300	-
			Tues	80	_			73.10141	600	
Total Supply Current**†	IT	5.0	00 1		JT = (1	.74 µA/kH2	f + IDD			μAdc
(Dynamic plus Quiescent,		10				.65 µA/kHz			XX	X
Per Package)		15			T = (5	.73 µA/kH2) f + IDD		0 0	0
(C _L = 50 pF on all outputs, all			-					-		-
buffers switching)			1 1						XX	5.1

2.5 Vdc min @ VDD = 15 Vdc

†To calculate total supply current at loads other than 50 pF:

IT(CL) = IT(50 pF) + 5 x 10⁻³ (CL -50) VDpf

where: IT is in µA (per package), CL in pF, VDD in Vdc, and f in kHz is input frequency.

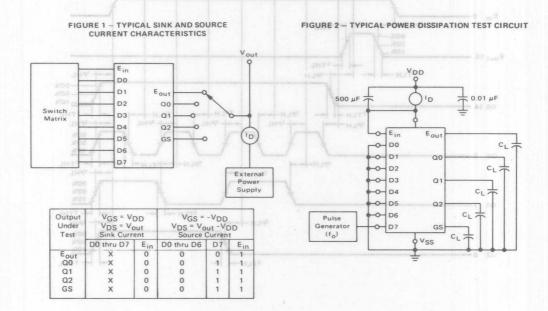
**The formulas given are for the typical characteristics only at 25°C.

^{*}T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.

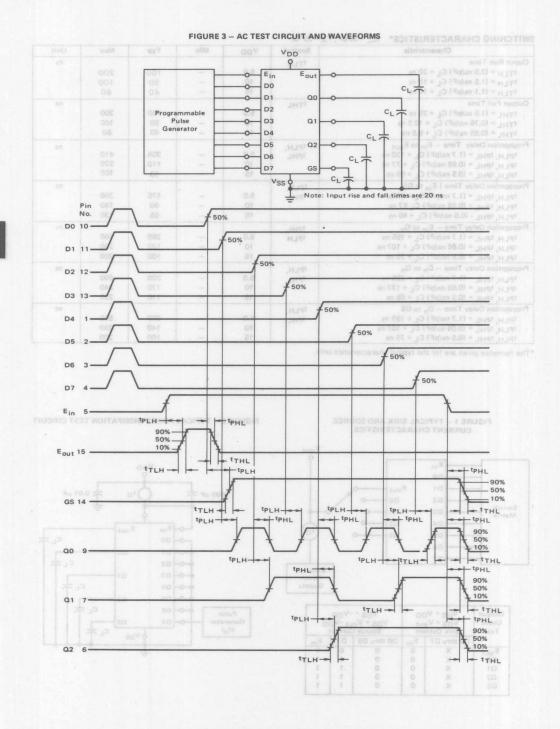
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc 2.0 Vdc min @ V_{DD} = 10 Vdc 2.5 Vdc min @ V_{DD} = 15 Vdc

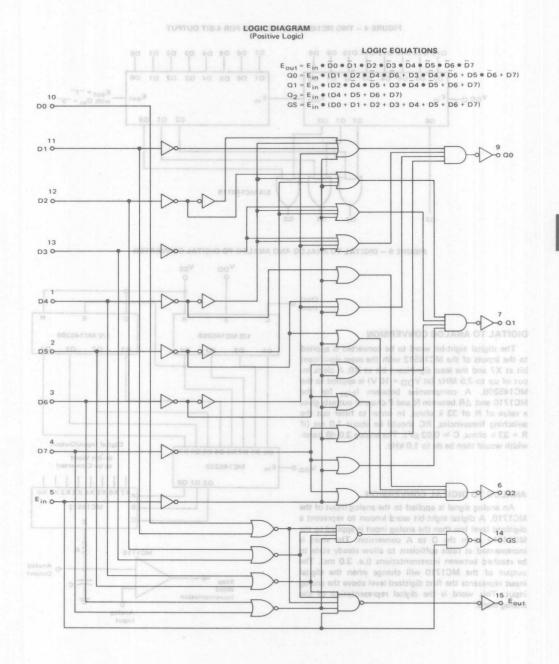
Characteristic	Symbol	V _{DD}	Min	Тур	Max	Unit
Ouput Rise Time	tTLH					ns
t _{TLH} = (3.0 ns/pF) C _L + 30 ns	Trun3	5.0	-	100	200	
tTLH = (1.5 ns/pF) CL + 15 ns		10	-	50	100	
tTLH = (1.1 ns/pF) CL + 10 ns	lon .	15	-	40	80	
Output Fall Time	tTHL					ns
t _{THL} = (1.5 ns/pF) C _L + 25 ns		5.0	=idpmm	100	200	
t _{THL} = (0.75 ns/pF) C _L + 12.5 ns	10	10	_ seli	50	100	
t _{THL} = (0.55 ns/pF) C _L + 9.5 ns		15	10381	40	80	
Progagation Delay Time - Ein to Eout	SE TPLH.	0-0-				ns
tpLH, tpHL = (1.7 ns/pF) CL + 120 ns	tPHL	5.0	-	205	410	
tpLH, tpHL = (0.66 ns/pF) CL + 77 ns	25	10	-	110	220	
tPLH, tPHL = (0.5 ns/pF) CL + 55 ns		15	_	80	160	
Propagation Delay Time (Ein to GS	tPLH.					ns
tpLH, tpHL = (1.7 ns/pF) CL + 90 ns	TO TPHL	5.0	-	175	350	
tPLH, tPHL = (0.66 ns/pF) CL 57 ns		10	-	90	180	
tPLH, tPHL - (0.5 ns/pF) CL + 40 ns		15	02 ¥-	65	130	
Propagation Delay Time - Ein to Qn	tPHL.				America ()	ns
tplH, tpHL = (1.7 ns/pF) CL + 195 ns	tPLH	5.0	-	280	560	
tplH tpHL = (0.66 ns/pF) CL + 107 ns		10	\	140	280	7.0
tPLH, tPHL = (0.5 ns/pF) CL + 75 ns		15		100	200	
Propagation Delay Time - D _n to Q _n	tPLH.	100 %			1	so ns
tpLH, tpHL = (1.7 ns/pF) CL + 265 ns	tPHL	5.0	-	300	600	
tpLH, tpHL = (0.66 ns/pF) CL + 137 ns	- 900g -	10	-	170	340	
tPLH, tPHL = (0.5 ns/pF) CL + 85 ns	-	15	-	110	220	60
Propagation Delay Time - Dn to GS	tPLH,			/		ns
tPLH, tPHL = (1.7 ns/pF) CL + 195 ns	tPHL	5.0		280	560	50
tPLH, tPHL = (0.66 ns/pF) CL + 107 ns		10	-	140	280	
tPLH, tPHL = (0.5 ns/pF) CL + 75 ns		15	-	100	200	100

^{*}The formulae given are for the typical characteristics only.









- C

Analog Input

FIGURE 4 - TWO MC14532B's CASCADED FOR 4-BIT OUTPUT

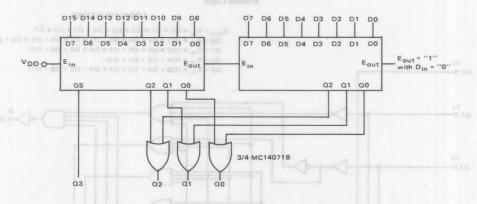
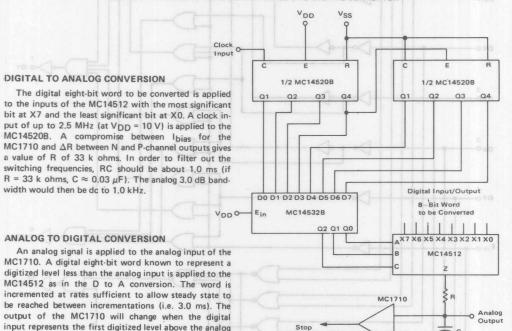


FIGURE 5 - DIGITAL TO ANALOG AND ANALOG TO DIGITAL CONVERTER



Word Incrementation

input. This word is the digital representation of the

analog word.



MC14534B

CMOS LSI

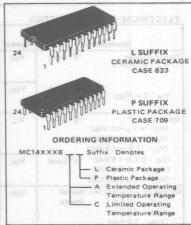
(LOW-POWER COMPLEMENTARY MOS)

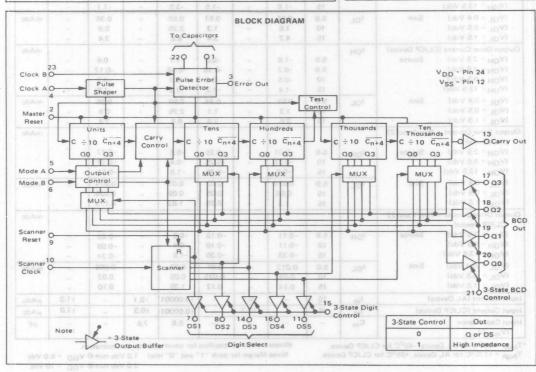
5-DECADE COUNTER

5-DECADE COUNTER

The MC14534B is a complementary MOS circuit composed of five decade ripple counters that have their respective outputs time multiplexed using an internal scanner. Outputs of each counter are selected by the scanner and appear on four BCD pins. The selected decade is indicated by a logic high on the appropriate digit select pin. Both BCD and digit select outputs have three-state controls providing an "open-circuit" when these controls are high and allowing time multiplexing. Cascading may be accomplished by using the carry-out pin. The counters and scanner can be independently reset by applying a high to the counter master reset (MR) and the scanner reset (SR). The MC14534B was specifically designed for application in real time or event counters where continual updating and multiplexed displays are used.

- Four Operating Modes (See truth table)
- Input Error Detection Circuit
- Clock Conditioning Circuits for Slow Transition Inputs
- Counter Sequences on Positive Transition of Clock A
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range







MAXIMUM RATINGS (Voltages referenced to VSS)

Rating	Symbol	Value	Unit
DC Supply Voltage	V _{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	Vin	-0.5 to V _{DD} + 0.5	Vdc
DC Current Drain per Pin	1	10	mAdo
Operating Temperature Range — AL Device CL/CP Device	TA	-55 to +125 -40 to +85	NOS C
Storage Temperature Range	T _{stg}	-65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that Vin and Vout be constrained to the range VSS \leq (Vin or VI) $V_{out}) \leqslant V_{DD}$

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD).

ELECTRICAL	CHARACTERISTICS
------------	-----------------

	108	VDD	Tio	W	relejo del	25°C	uffer o	Th	igh*	
Characteristic	Symbol	Vdc	Min	Max	Min	Тур	Max	Min	Max	Unit
Output Voltage "0" Level	VOL	5.0	CHAINING F	0.05	2 10 (010/1/	0	0.05	no manne	0.05	Vdc
Vin VDD or 0	0.	10	erts grieut	0.05	ilamoss	0	0.05	sung. Ca	0.05	
ENG SERT		15	ently rese	0.05	can be i	0	0.05	The cos	0.05	
"1" Level	VOH	5.0	4.95	a pure tu	4.95	5.0	TOWN DAY	4.95	a Britishiring	Vdc
Vin - 0 or VDD	- OH	10	9.95	n not ben	9.95	10	334B w	9.95	I (NE) I	
	10P	15	14.95	polating	14.95	15	ounters	14.95	eal time of	
Input Voltage# "0" Level	VIL							8571 818 51	red display	Vdc
(V _O = 4.5 or 0.5 Vdc)	1	5.0		1.0	_ 1	1.5	1.0	oM mite	1301.0 00	
(Vo = 9.0 or 1.0 Vdc)		10		2.0	-	3.0	2.0	Detection	2.0	
(V _O = 13.5 or 1.5 Vdc)		15		3.0		4.5	3.0	0.00130	3.0	
(V _O = 0.5 or 4.5 Vdc) "1" Level	VIH	5.0	4.0	atudin a	4.0	3.5	CHUONU	4.0	mod room	Vdc
(VO = 1.0 or 9.0 Vdc)	VIH	10	8.0	pole_A	8.0	7.0	en Posit	8.0	Counter Se	0
(VO = 1.5 or 13.5 Vdc)	1	15	12	_	12	It ontoV	0.E = 50	16 F12 61	oV-ylqqui	
Output Drive Current (AL Device)	1	1.0	swoo-wo	ls, One L	neo J JT	19W00-W	Cwo Lo	Driving	to eldses!	mAd
	ОН	5.0	-1.2	of the Flatte	-1.0	-1.7	wT-10	-0.7	chotticu	MAG
(V _{OH} 2.5 Vdc) Source (V _{OH} 4.6 Vdc)		5.0	-0.25	THE FLUIS	-0.2	-0.36	W. 1-10	-0.14	Date R and	
(VOH = 9.5 Vdc)		10	-0.62		-0.2	-0.9		-0.35	Bueu aum	
(VOH = 13.5 Vdc)		15	-1.8	7	-1.5	-3.5		-1.1		
(VOI = 0.4 Vdc) Sink	1-1-	5.0	0.64		0.51	0.88	_	0.36		mAd
OL .	IOL	10	1.6	BLOCK	1.3	2.25	_	0.36		MAG
(V _{OL} = 0.5 Vdc) (V _{OL} = 1.5 Vdc)		15	4.2	_	3.4	8.8	2.	2.4		
	—	13	4.2		3.4	0.0		2.4	_	
Output Drive Current (CL/CP Device)	ІОН	F 0			40	91.7		0.0		mAd
(VOH = 2.5 Vdc) Source		5.0	-1.0	-	-0.8		-	-0.6	5.5	
(V _{OH} = 4.6 Vdc)		5.0	-0.2	-	-0.16	-0.36		-0.12	0	
(V _{OH} = 9.5 Vdc)		10	-0.5	UD 10113	-0.4	-3.5	-	-0.3	0	
(V _{OH} = 13.5 Vdc)		15	-1.4					-1.0		-
(VOL = 0.4 Vdc) Sink	OL	5.0	0.52	-	0.44	0.88	-	0.36		mAd
(V _{OL} = 0.5 Vdc)		10	1.3	-	1.1	2.25		0.9	- 0	
(V _{OL} = 1.5 Vdc)		15	3.6	1-	3.0	8.8		2.4		70287
Output Drive Current - Pins 1 and 22					-					mAd
(AL Device)	"D 01+		Ern2 01	3 2 7	HaD OF-	ion		AtaD OF	- open	
(VOH = 2.5 Vdc) Source	OH	5.0	-0.31	e_	-0.25	-0.8		-0.17	100	
(V _{OH} = 9.5 Vdc)		10	-0.31		-0.25	-0.4	- 1	-0.17	- 5	
(VOH = 13.5 Vdc)	XUM S	15	-0.9	197 1	-0.75	-1.6	-	-0.51	0 -2-0	
(VOL = 0.4 Vdc) Sink	OL	5.0	0.024	F +	0.02	0.03	-	0.014	2 2 9	mAd
(V _{OL} = 0.5 Vdc)	115111	10	0.06	+	0.05	0.09	-	0.035	-	
(V _{OL} = 1.5 Vdc)		15	1.3	-	0.25	1.63	-	0.175	-	
Output Drive Current – Pins 1 and 22 (CL/CP Device)			- 1							mAd
(VOH = 2.5 Vdc) Source	ІОН	5.0	-0.11	-	-0.10	-0.8		-0.08		
(V _{OH} = 9.5 Vdc)		10	-0.11	-	-0.10	-0.4		-0.08	- 0	
(V _{OH} = 13.5 Vdc)		15	-0.33	-	-0.30	-1.6	-	-0.24	- 4	
(VOL = 0.4 Vdc) Sink	IOL	5.0	0.012	1	0.01	0.02	10	0.008		mAd
(VOL = 0.5 Vdc)	0.	10	0.03		0.025	0.05	-	0.02	_	×300
(VOL = 1.5 Vdc)		15	0.14	_	0.12	1.35	1 -	0.10		
Input Current (AL Device)	lin	15	7 -57	±0.1	T-2 1	±0.00001	:0.1		±1.0	μAd
nput Current (CL/CP Device)	1	15	CZY	±0.1	EV 1	±0.00001	±0.1	_	±1.0	
	1 _{in}	150		0.87	OR	17.5		-		μAd
nput Capacitance (Vin - 0)	Cin	- 3	60 _F50	680	190	5.0	7.5	- 3	Note:	pF

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device. Thigh = +125°C for AL Device, +85°C for CL/CP Device.

#Noise immunity specified for worst-case input combination.

Noise Margin for both "1" and "0" level 1.0 Vdc min @ VDD = 5.0 Vdc

2.0 Vdc min @ V_{DD} = 10 Vdc 2.5 Vdc min @ V_{DD} = 15 Vdc

		VDD	Tie	ow*	1000	25°C		Th	igh "	
Characteristic	Symbol	Vdc	Min	Max	Min	Тур	Max	Min	Max	Unit
Quiescent Current (AL Device)	Ipp	5.0	-	5.0	7 8 8	0.010	5.0		150	μAdc
(Per Package)		10		10		0.020	10	Stocks -	300	
		15	-31	20	_	0.030	20	-	600	
Quiescent Current (CL/CP Device)	IDD	5.0	-	50	11	0.010	50	adin'	375	μAdo
(Per Package)	1	10	- 4	100	loans.	0.020	100	_	750	-
	1 11	15	!	200	-	0.030	200	-	1500	
Total Supply Current**†	- IT	5.0		I _T = (0.5 μA/kHz) f + IDD						μAdd
(Dynamic plus Quiescent,	1 11	10				A/kHz) f +		Scan O	scillator	
Per Package)	1 11	15				A/kHz) f +		Frequenc	y = 1 kHz	
(CL = 50 pF on all outputs, all buffers switching)	1						00			
Three-State Leakage Current (AL Device)	JTL	15		± 0.1	-	•0.00001	± 0.1	-	± 3.0	μAdo
Three-State Leakage Current (CL/CP Device)	ITL	15		±1.0		+0.00001	± 1.0	NO SHAD	± 7.5	μAdo

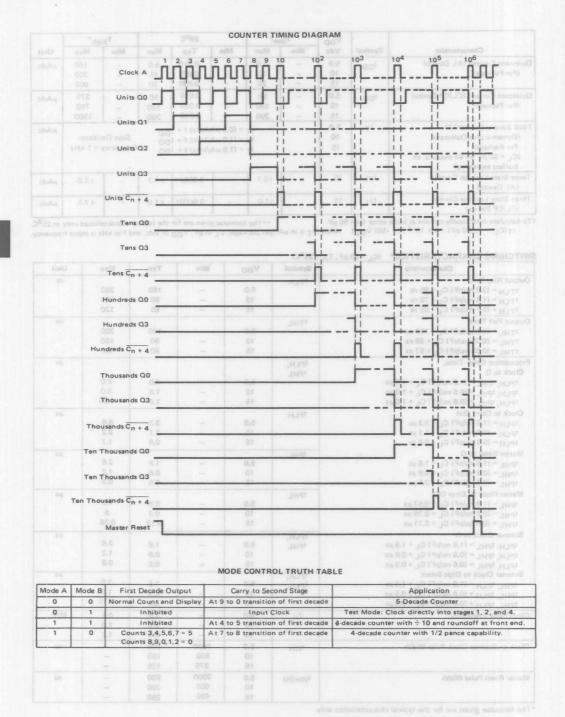
To calculate total supply current at loads other than 50 pF:

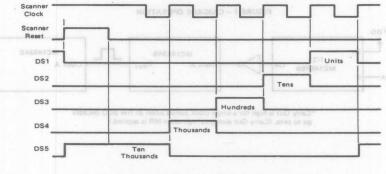
--The formulas given are for the typical characteristics only at 25° C.

IT(CL) = IT(50 pF) + 1 x 10^{-3} (CL -50) VDDf where: IT is in μ A (per package), CL in pF, VDD in Vdc, and f in kHz is input frequency.

Characteristic	Symbol	VDD	Min	Тур	Max	Unit
Output Rise Time	tTLH		- Company	Carterior St.		ns
tTI H = (3.0 ns/pF) C ₁ + 95 ns		5.0	_	180	360	
tTLH = (1.5 ns/pF) CL + 78 ns		10	_	90 00	180	
tTLH = (1.1 ns/pF) CL + 68 ns	Enterprise and con-	15	-	65	130	
Output Fall Time	tTHL			E (2.3	entrepolet	ns
tTHI = (1.5 ns/pF) C ₁ + 117 ns		5.0		100	200	
tTHI = (0.75 ns/pF) C1 + 89 ns		10	_	50	100	
t _{THL} = (0.55 ns/pF) C _L + 67 ns		15	12.12	40	80	
Propagation Delay Time,	tPLH.					μs
Clock to Q	tPHL			in the same of		
tPLH tPHL = (1.8 ns/pF) C _L + 4.0 μs	THE	5.0		4.0	8.0	
tplH, tpHL = (0.8 ns/pF) CL + 1.5 µs		10		1.5	3.0	
tp_H, tpHL = (0.6 ns/pF) CL + 1.0 \(\mu\)s		15		1.0	2.25	
Clock to Carry Out	toru			1.0		μς
$t_{PLH} = (1.8 \text{ ns/pF}) C_1 + 3.3 \mu s$	tPLH	5.0		3.3	6.6	μ.,
$t_{PLH} = (0.8 \text{ ns/pF}) C_1 + 1.1 \mu s$		10		1.1	2.2	
$t_{PLH} = (0.6 \text{ ns/pF}) C_1 + 0.8 \mu s$		15		0.8	1.7	
Master Reset to Q		13		0.0	1.7	
tpH _L = (1.8 ns/pF) C _L + 1.8 μs	tPHL	5.0	-	1.8	3.6	μs
		10	_		1.2	F 45, 247
$t_{PHL} = (0.8 \text{ ns/pF}) C_{L} + 0.6 \mu s$		15		0.6	0.9	
tpHL = (0.6 ns/pF) CL + 0.5 μs		15		0.5	0.5	
Master Reset to Error Out	tPHL				1.5	hs.
tpHL = (1.8 ns/pF) CL + 0.57 μs		5.0			The second second	
$t_{PHL} = (0.8 \text{ ns/pF}) C_{L} + 0.19 \mu s$		10		0.2	.5	
tpHL = (0.6 ns/pF) CL + 0.11 μs		15	-	0.12	0.38	
Scanner Clock to Q	tPLH,			40000		μs
tpLH, tpHL = (1.8 ns/pF) CL + 1.8 μs	tPHL	5.0		1.8	3.6	
tpLH, tpHL = (0.8 ns/pF) CL + 0.6 μs		10	-	0.6	1.2	5 P. S.
tpLH, tpHL = (0.6 ns/pF) CL + 0.5 μs	BUILD MANAGE AN	15	-	0.5	0.9	
Scanner Clock to Digit Select	TPLH,				0.0	μs
tpHL, tpLH = (1.8 ns/pF) CL + 1.5 μs	tPLH,	5.0		1.5	3.0	M A sb
tpHL, tpLH = (0.8 ns/pF) CL + 0.5 μs	Manue un ve	10		0.5	1.0	transfer manager
tpHL, tpLH = (0.6 ns/pF) CL + 0.4 μs	abious (in) to it	15	P IA Lysinali	0.4	0.75	1 0
Clock Pulse Frequency	fcl	5.0	-	1.0	0.5	MHz
	ab-9 ebicab zent te n		1 5 1A	3.0	1.0	
A-decade countar with 1/2 ponce controllity.	n of first decade	15	TIAL 8-	5.0	1.2	1
Clock or Scanner Clock Pulse Width	tWH	5.0	1000	500		ns
		10	500	190	-	
		15	375	125	-	
Master Reset Pulse Width	tWH(R)	5.0	2000	900		ns
		10	600	300	_	
		15	450	250	_	

^{*}The formulae given are for the typical characteristics only.



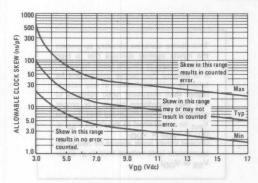


Note: If Mode B = 1, the first decade is inhibited and S1 will not go high, and the cycle will be shortened to four stages. DS5 is selected automatically when Scanner Reset goes high.

ERROR DETECTION TIMING DIAGRAM Error Good Pulse Error Good Pulse 2 Out

Note: Error detector looks for inverted pulse on Clock B. Whenever a positive edge at Clock A is not accompanied by a negative pulse at Clock B (or vice-verse) within a time period of the one-shots an error is counted. Three errors result in Error Out to go to a "1". If error detection is not needed, tie Clock B high or low and leave Pins 1 and 22 unconnected.

CLOCK SKEW RANGE



- The skew is the time difference between the low-to-high transition of C_A to the high-to-low transition of C_B or vice-wersa. Capacitors C1 = C22 tied from pins 1 and 22 to V_{SS}.
 This graph is accurate for C1 = C22 ≥ 100 pF.
- 3. When the error detection circuitry is not used, pins 1 and 22 are left open.

APPLICATIONS INFORMATION

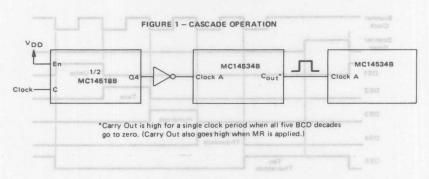
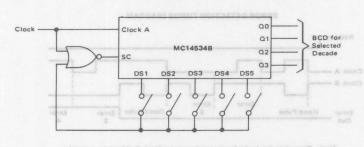


FIGURE 2 - FORCING A DECADE TO THE Q OUTPUTS



When the Q outputs of a given decade are required, this configuration will lock up the selected decade within four clock cycles. The select line feedback may be hardwired or switched.

PIN ASSIGNMENT VDD 24 2 MR Clock B 23 3 Eout Cext 22 4 Clock A 3-St BCD 21 5 Mode A Q0 20 01 19 6 Mode B 7 DS1 Q2 18 03 17 8 DS2 9 SR DS4 16 10 =sc 3-St Dig 15 11 DS5 DS3 14 Cout 13 12 VSS

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields: however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leqslant (V_{in}$ or $V_{out}) \leqslant V_{DD}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g. either

V_{SS} or V_{DD}).

3



MC14536B

PROGRAMMABLE TIMER

The MC14536B programmable timer is a flexible 24-stage ripple binary counter with 16 stages selectable by a binary code. Provisions for an on-chip RC oscillator, or an external clock are provided. An on-chip monostable circuit incorporating a pulse-type output has also been included. By selecting the appropriate output in conjunction with the correct input clock frequency, a variety of timing can be achieved.

- 24 Flip-Flop Stages Will Count From 20 to 224
- Last 16 Stages Selectable By Four-Bit Select Code
- Input Allows Bypassing of First Eight Stages
- Set and Reset Inputs
- Clock Inhibit Input
- On-Chip RC Oscillator Provisions
- On-Chip Monostable Output Provisions
- Clock Conditioning Circuit Permits Operation With Very Long Rise and Fall Times
- Clock Input f_{max} = 3.0 MHz typical @ V_{DD} = 10 Vdc
- Counter Advances On Negative Going Edge of Clock
- Test Mode Allows Fast Test Sequence
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range

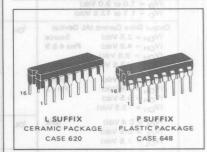
MAXIMUM RATINGS (Voltages referenced to VSS)

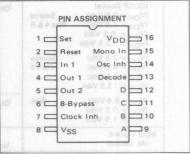
Rating p.g.	Symbol	Value	Unit
DC Supply Voltage	VDD	-0.5 to +18	Vdc
Input Voltage, All Inputs	8 Vin	-0.5 to V _{DD} + 0.5	Vdc
DC Current Drain per Pin	1 1 2 25	-10	mAdo
Operating Temperature Range - AL Device	TA	-55 to +125	оС
CL/CP Device		-40 to +85	
Storage Temperature Range	T _{stg}	-65 to +150	°C

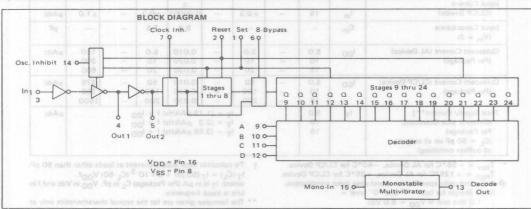
CMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

PROGRAMMABLE TIMER







ELECTRICAL CHARACTERISTICS

		V _{DD}	T _{lo}	w		25°C			Thigh *	
Characteristic	Symbol	Vdc	Min	Max	Min	Тур	Max	Min	Max	Unit
Output Voltage "O" Level	VOL	5.0	-	0.05	-	0	0.05	-	0.05	Vdc
$V_{in} = V_{DD}$ or 0		10 15	-	0.05	RHAI	0	0.05	паон	0.05	
"1" Level	VOH	5.0	4.95	_	4.95	5.0	_	4.95		Vdc
V _{in} = 0 or V _{DD}	, OH	10	9.95	10-145 N	9.95	10	eld-mi	9.95	0145-96	M artT
NO ATMENT INVESTIGATION OF THE PROPERTY.	. 11	15	14.95	stop	14.95	15	pols u sej	14.95	w Tetro	0p. y166
nput Voltage # "O" Level	VIL		A .bebi	orq sis	Maple II	extern)	8 10 ,1	dellicen	Ohip. RIC	Vdc
$(V_0 = 4.5 \text{ or } 0.5 \text{ Vdc})$		5.0	set High	1.5	relue s	2.25	1.5	CONTRACTOR	1.5	distant
$(V_0 = 9.0 \text{ or } 1.0 \text{ Vdc})$ $(V_0 = 13.5 \text{ or } 1.5 \text{ Vdc})$		10	NUTHE CO	3.0	io e t sini	4.50 6.75	3.0	Hoe-AB"	3.0	Head o
0		15	no prinsi	4.0	315 N. S. V.	0.75	4.0	signi to	4.0	diffe n
"1" Level $(V_0 = 0.5 \text{ or } 4.5 \text{ Vdc})$	VIH	5.0	3.5	- 3	3.5	2.75		3.5		Vdc
$(V_O = 0.3 \text{ or } 4.5 \text{ Vdc})$ $(V_O = 1.0 \text{ or } 9.0 \text{ Vdc})$		10	7.0	_ *	7.0	5.50	mon H	7.0	-F10p Sta	24 FB
(V _O = 1.5 or 13.5 Vdc)		15	11.0	_ 9	11.0	8.25	BUFG	11.0	Stages S	1 225.3
Output Drive Current (AL Device)	ГОН				1963	Elght St	12 H - 14	grdssig	E ewolls	mAdc
(V _{OH} = 2.5 Vdc) Source	UH	5.0	-1.2	-	-1.0	-1.7	-	-0.7	I Reset I	Set an
(V _{OH} = 4.6 Vdc) Pins 4 & 5		5.0	-0.25	-	-0.2	-0.36	-	-0.14	-	Clack
$(V_{OH} = 9.5 \text{ Vdc})$	1	10	-0.62	-	-0.5	-0.9	-	-0.35	ni s <u>id</u> ide	
$(V_{OH} = 13.5 \text{ Vdc})$	to 1	15	-1.8	-	-1.5	-3.5	10/27/01	-1.1	p RG-Ou	1000
(V _{OH} = 2.5 Vdc) Source	展 11	5.0	-3.0	-	-2.4	-4.2	pu+Pro	-1.7	p Menos	mAdc
(V _{OH} = 4.6 Vdc) Pin 13	ar	5.0	-0.64	V THW	-0.51	-0.88	e9 Tius	-0.36	Conditio	Clock
(V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc)		1.0	-1.6 -4.2	_	-1.3 -3.4	-2.25 -8.8	_	-0.9 -2.4	d Fall Ti	Rise as
	1	5.0	0.64	aby t	0.51	0.88	A1 2140	0.36	smi zugn	mAdc
$(V_{OL} = 0.4 \text{ Vdc})$ Sink $(V_{OL} = 0.5 \text{ Vdc})$	OL	10	1.6	_lbo	1.3	2.25		0.36	showh A n	mAdc
(V _{OL} = 1.5 Vdc)		15	4.2	-	3.4	8.8	100	2.4	edi A ebo	M too T
Output Drive Current					de	/ 81-01	bV D.E	Range =	Voltage	demi2
(CL/CP Device)	ІОН			1						mAdc
(V _{OH} = 2.5 Vdc) Source		5.0	-1.0	U WO.	-0.8	-1.7	d-Ann	-0.6	of Draw	School
(V _{OH} = 4.6 Vdc) Pins 4 & 5 (V _{OH} = 9.5 Vdc)		5.0	-0.2 -0.5	J10315-411-101	-0.16 -0.4	-0.36 -0.9	H =N1	-0.12 -0.3	JIT y	Familia
(V _{OH} = 13.5 Vds)		15	-1.4	_	-1.2	-3.5		-1.0	- agree	0.1075
(V _{OH} = 2.5 Vdc) Source		5.0	-2.5	_	-2.1	-4.2		-1.7	_	mAdc
(V _{OH} = 4.6 Vdc) Pin 13	1 1 1	5.0	-0.52	_	-0.44	-0.88	anenste:	-0.36	TINGS	NAME
(V _{OH} = 9.5 Vdc)		10	-1.3	uhiV_	-101	-2.25	-	-0.9	nate <u>B</u>	
(V _{OH} = 13.5 Vdc)		15	-3.6	or 3. 0-	-3.0	-8.8	-	-2.4	- 90	szlość y
(V _{OL} = 0.4 Vdc) Sink	loL	5.0	0.52	g V_p1 d	0.44	0.88	_	0.36	stwan!	mAdc
$(V_{OL} = 0.5 \text{ Vdc})$ $(V_{OL} = 1.5 \text{ Vdc})$		10	1.3	- 10	1.1	2.25		0.9	000 Ppg	mag in
PT TO STATE OF THE PARTY OF THE		15	3.6	Q1 88 -	3.0	8.8	e.live()	2.4	N Gruzer	Sqime T
nput Current (AL Device)	lin	15	-0.07	±0.1	-	± 0.00001	±0.1	40/30	±1.0	цAdc
nput Current	'in		1	20.7	7 845	±		-		pr. 100
(CL/CP Device)	lin	15	-	±0.3	-	0.00001	±0.3	-	± 1.0	μAdc
nput Capacitance	C _{in}	_	eminut	8	100.70	5.0	7.5	_	1_	pF
$(V_{in} = 0)$	an .			90 9	2.0	9	2			
Quiescent Current (AL Device)	IDD	5.0	-	5.0	-	0.010	5.0	-	150	μAdc
(Per Package)		10	-	10	-	0.020	10	-	300	THE PERSON
		15	-	20	- 1	0.030	20	_	600	
Quiescent Current (CL/CP Device)	lDD	5.0	-	50	100112	0.010	50	4	375	μAdc
(Per Package)	0 0 0	10	1 5 m	100	thru B	0.020	100	7-1-0	750 1500	V
otal Supply Current**†	1 1 1	5.0			1 /1	-			11500	A de
(Dynamic plus Quiescent,	IT	10			$I_T = (1.$	15 μA/kH: 3 μA/kH:	z) f + 10	D		μAdc
Per Package)		15	-		$I_T = (3.$	55 μA/kH	z) f + lp	D		
(C _L = 50 pF on all outputs,						50	7100 P	1 100		1

^{**} Tlow = -55°C for AL Device, -40°C for CL/CP Device.

Thigh = +125°C for AL Device, +85°C for CL/CP Device.

** Noise immunity specified for worst-case input combination.

Noise Margin for both "1" and "0" level =

1.0 Vdc min @ V_{DD} = 5.0 Vdc

2.0 Vdc min @ V_{DD} = 10 Vdc

2.5 Vdc min @ V_{DD} = 15 Vdc

MOTOROLA

SWITCHING CHARACTERISTICS* (CL = 50 pF, TA = 25°C)

Characteristic	Symbol	VDD	Min	Тур	Max	Unit
Output Rise Time (Counter Outputs) t _{TLH} = (3.0 ns/pF) C _L + 30 ns t _{TLH} = (1.5 ns/pF) C _L + 15 ns t _{TLH} = (1.1 ns/pF) C _L + 10 ns	TLH self	10	utitioning to the 24 flip gative trans	100 50 40	200 100 80	while at the
Output Fall Time (Counter Outputs) tTHL = (1.5 ns/pF) CL + 25 ns tTHL = (0.75 ns/pF) CL + 12.5 ns tTHL = (0.55 ns/pF) CL + 9.5 ns	THL		Hip-Hop stay zansit <u>io</u> n. T thu 24 thy	100 50 40	200 100 80	in the Set counting of behavior is
Propagation Delay Time Clock to Q1, 8-Bypass (Pin 6) High tpLH, tpHL = (1.7 ns/pF) CL + 1715 ns tpLH, tpHL = (0.66 ns/pF) CL + 617 ns tpLH, tpHL = (0.5 ns/pF) CL + 425 ns	tPLH, tPHL	5.0	a logical "I oscillator to or input is input to	1800 650	3600 1300 1000	Reset in Reset in Set also di low power external C
Clock to Q1, 8-Bypass (Pin 6) Low	tPLH,		od in-the	3.8	3.0	NICE SUCIES OF THE CONTROL OF THE CO
Clock to Q16 tPHL, tPLH = (1.7 ns/pF) CL + 6915 ns tPHL, tPLH = (0.66 ns/pF) CL + 2967 ns tPHL, tPLH = (0.5 ns/pF) CL + 2175 ns	tPLH, tPHL	10		7.0	6.0	
Reset to Q _n tpH _L = (1.7 ns/pF) C _L + 1415 ns tpH _L = (0.66 ns/pF) C _L + 567 ns tpH _L = (0.5 ns/pF) C _L + 425 ns	tPHL A	5.0 10 15	FIGURATION ND OLOGK	1500 600 450	3000 1200 900	ns FIGURE 1
Clock Pulse Width	tWH	5.0 10 15	600 200 170	300 100 85	-	ns
Clock Pulse Frequency (50% Duty Cycle)	f _{Cl}	5.0 10 15	0-1 t tu0	1.2 3.0 5.0	0.4 1.5 2.0	MHz
Clock Rise and Fall Time	tTLH, tTHL	5.0 10 15		No Limit	3-0 0-0	<u>-</u> ال
Reset Pulse Width	tWH	5.0 10 15	1000 400 300	500 200 150	2 o = 0	ns

^{*} The formulae given are for the typical characteristics only.

IN ₁	Set	Reset	Clock	Osc	Out 1	Out 2	Decode Out
5	0	0	0	0	5	7	No Change
~	0	0	0	0	~	5	Advance to next state
×	1	0	0	0	0	1	1
×	0	1	0	0	0	1	0
×	0	0	-10-	0	9		No Change
0	0	0	0	×	0	1	No Change
1	0	0	0	5	1	5	Advance to next state

				HIMDE	•	
			П	8-By	oass	
D	,C	В	A	0	1	
0	0	0	0	9	1	
0	0	0	1	10	2	
0	0	1	0	11	3	
0	0	1	1	12	4	- 18 ATB 1
0	1	0	0	13	5	
0	1	0	1	14	6	
0	1	1	0	15	7	Anna a managana
0	1	1	1	16	8	FLOURE 3 - TIM
1	0	0	0	17	9	ON-CHIP RC
1	0	0	1	18	10	TOT
1	0	1	0	19	11	
1	0	1	1	20	12	
1	1	0	0	21	13	
1	1	0	1	22	14	
1	1	1	0	23	15	
1 1	11	11	11	24	16	

TRUTH TABLE

OPERATING CHARACTERISTICS 101 *20172183TDARAND 2011HOTHWS

Set input initializes output to a "1". This is accomplished by setting an output conditioning latch to a 1 while at the same time resetting the 24 flip-flop stages. With the occurence of the first negative transition of the clock, the output will change to a "0". When the circuit is in the Set condition, the counter flip-flop stages will start counting on the second negative transition. The resulting behavior is the same as if each of the 24 flip-flop stages were set.

Reset inputs resets all stages to a logical "O". Reset or Set also disables the on-chip RC oscillator to allow very low power standby operation. In 1 input is used as the external Clock input or as the input to the on-chip RC oscillator.

Out 1, Out 2 outputs are used in the on-chip RC oscillator configuration.

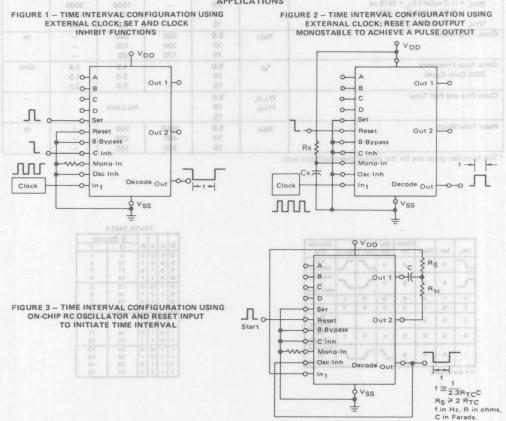
8-Bypass input bypasses the first eight stages resulting in a 16-stage counter with all 16 stages selectable, one at a time. Clock Inhibit input disconnects the first counter stage from the input circuit, therefore inhibiting counting. This Clock Inhibit input is independent of the state of the

Clock input. When the Clock Inhibit input is disabled, the counter will start counting only with the occurrence of the first negative edge of the Clock.

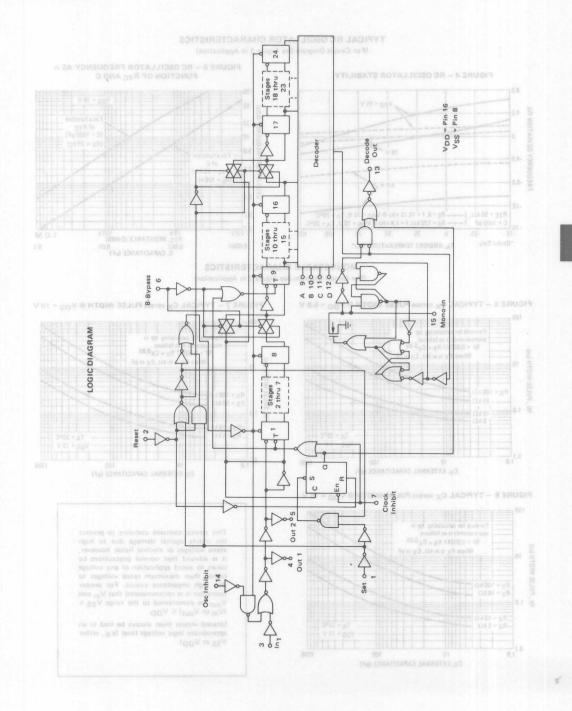
Binary Select inputs A, B, C, and D select the flip-flop stage to be connected to the output. Decode Out output can either be connected directly to a flip-flop output or to the monostable output. Osc Inhibit input can be used to disable the on-chip RC oscillator to allow very low power standby operation. Mono In input is used as the timing pin for the on-chip monostable oscillator. If the Mono In input is grounded through a resistor, the monostable circuit is disabled and the output is connected directly to the selected flip-flop. The monostable circuit is enabled if a resistor is connected between this pin and VDD and a capacitor connected between this pin and ground. Any desired pulse width can be achieved depending upon the value of the R and C selected.

The test mode configuration divides the 24 flip-flop stages into three 8-stage sections to facilitate a fast test sequence. This test mode is enabled when 8-Bypass, Set and Reset are at a "1"

APPLICATIONS



3



TYPICAL RC OSCILLATOR CHARACTERISTICS

(For Circuit Diagram See Figure 3 in Application)

FIGURE 4 - RC OSCILLATOR STABILITY

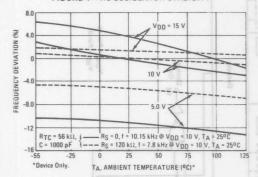
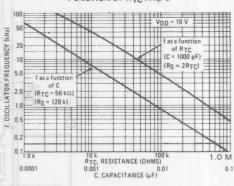


FIGURE 5 – RC OSCILLATOR FREQUENCY AS A FUNCTION OF R_{TC} AND C



MONOSTABLE CHARACTERISTICS

(For Circuit Diagram See Figure 2 in Application)

FIGURE 6 - TYPICAL CX versus PULSE WIDTH @ VDD = 5.0 V

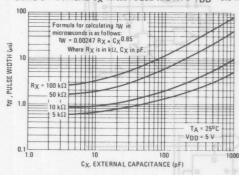


FIGURE 7 - TYPICAL CX versus PULSE WIDTH @ VDD = 10 V

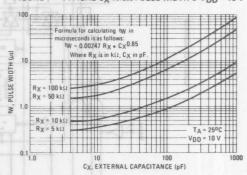
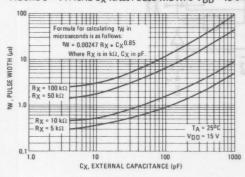


FIGURE 8 - TYPICAL CX versus PULSE WIDTH @ VDD = 15 V

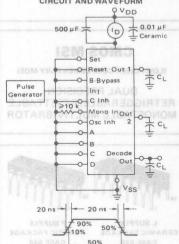


This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leqslant (V_{in} \text{ or } V_{out}) \leqslant V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD).

MC14536B

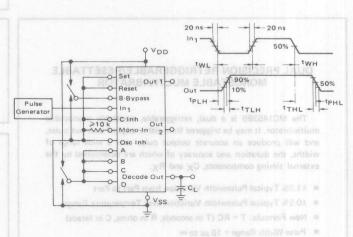
FIGURE 9 - POWER DISSIPATION TEST CIRCUIT AND WAVEFORM



Duty Cycle

MOTOROLA

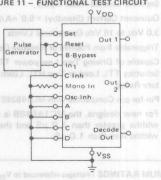
FIGURE 10 - SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



FUNCTIONAL TEST SEQUENCE

Test function (Figure 11) has been included for the reduction of test time required to exercise all 24 counter stages. This test function divides the counter into three 8-stage sections and 255 counts are loaded in each of the 8-stage sections in parallel. All flip-flops are now at a "1". The counter is now returned to the normal 24-stages in series configuration. One more pulse is entered into Inj not be based modes at 88 which will cause the counter to ripple from an all "1" state and 88024413M and br to an all "O" state.

FIGURE 11 - FUNCTIONAL TEST CIRCUIT



FUNCTIONAL TEST SEQUENCE

	100000000000000000000000000000000000000	INPUTS	30	OUTPUTS	A GOV of 2.0 COMMENTS stages II A sostio
In ₁	Set	Reset	8-Bypass	Decade Out Q1 thru Q24	All 24 stages are in Reset mode.
1	0	0.01	1	0	CL/CP Device 40 to 185
1	1	-1	1	0	Counter is in three 8-stage sections in parallel mode.
0	10	1	1	0	First "1" to "0" transition of clock.
1 0 -	1 55	, (F	12 0 11 11 0 0		255 "1" to "0" transitions are clocked in the counter.
0	1	11	0 1;	1 _{ni} V sortt l	
0	0	EDING OS XO	ana gO	lamia .a.	Counter converted back to 24 stages in series mode. Set and Reset must be connected together and simultaneously go from "1" to "0".
1	0	It nino agv	0	1	In 1 Switches to a "1".
0	0	0	0	0	Counter Ripples from an all "1" state to an all "0" state.



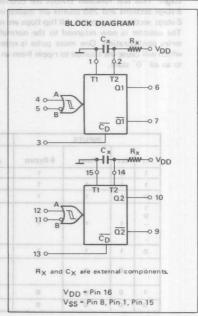
MC14538B

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

DUAL PRECISION
RETRIGGERABLE/RESETTABLE
MONOSTABLE MULTIVIBRATOR

L SUFFIX CERAMIC PACKAGE CASE 620 CASE 648 ORDERING INFORMATION MC14XXXB L Ceramic Package Plastic Package A Extended Operating Temperature Range C Limited Operating Temperature Range



DUAL PRECISION RETRIGGERABLE/RESETTABLE MONOSTABLE MULTIVIBRATOR

The MC14538B is a dual, retriggerable, resettable monostable multivibrator. It may be triggered from either edge of an input pulse, and will produce an accurate output pulse over a wide range of widths, the duration and accuracy of which are determined by the external timing components, C_X and R_X .

- ±1.0% Typical Pulsewidth Variation from Part to Part
- ±0.5% Typical Pulsewidth Variation over Temperature Range
- New Formula: T = RC (T in seconds, R in ohms, C in farads)
- Pulse Width Range = 10 μs to ∞
- Symmetrical Output Sink and Source Capability
- Latched Trigger Inputs
- Separate Latched Reset Inputs
- Quiescent Current (Standby) = 5.0 nA/package typical @ 5 Vdc
- 3.0 Vdc to 18 Vdc Operational Limits
- Triggerable from Positive or Negative-Going Edge
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range
- Pin-for-pin Compatible with MC14528B and CD4528B (CD4098)
- For new designs, the MC14548B is recommended for pulse widths greater than 1.0 μ S and the MC14528B for pulse widths less than 1.0 μ S.

MAXIMUM RATINGS (Voltages referenced to VSS)

Rating	Symbol	Value	Unit
DĆ Supply Voltage	VDD	-0.5 to +18	Vdc
Input Voltage, All Inputs	Vin	-0.5 to V _{DD} + 0.5	Vdc
DC Current Drain per Pin	1	10	mAdd
Operating Temperature Range — AL Device CL/CP Device	TA	-55 to +125 -40 to +85	oC
Storage Temperature Range	T _{stg}	-65 to +150	oC.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leqslant |V_{in}$ or $V_{out} | \leqslant V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either Vss or $\rm V_{DD}$).

SWITCHING CHARACTERISTICS* (C) = 50.pf. Ta = 26°C)

ELECTRICAL CHARACTERISTICS

				H neV	VDD	Tic	w*		25°C		Thi	gh*	
	Charact	teristic	niN	Symbol	Vdc	Min	Max	Min	Тур	Max	Min	Max	Unit
Output	Voltage	"0"	Level	VOL	5.0	HUTE!	0.05	_	0	0.05	979	0.05	Vdc
	= V _{DD} or 0			0.6	10	_	0.05	_	0 10	0.05	Halan B	0.05	ITI
- 111	001			07	15	_	0.05	_	0 811	0.05	Rolan Ol	0.05	UTF
		OA 11911	Level	VOH	5.0	4.95		4.95	5.0	22 - 10	4.95	(0) - 11	Vdc
V	O or VDD		revei	VOH	10	9.95		9.95	10		9.95	noT (lin ti	AUG INC
v in	OGLADD	001	-	6.0	15	14.95	-	14.95	15	10_+33	14.95	(1) <u>=</u> (1)	NT7
Input V			Level	VIL					201	3C + 30 /	Belan Ol	inter t	Vdc
	= 4.5 or 0.5 Vd	c)			5.0	-	1.5		2.25	1.5	-	1.5	10.3
(Vo	= 9.0 or 1.0 Vd	lc)			10	HUT	3.0	-	4.50	3.0	Broil I ye	3.0	endo.
(VO	= 13.5 or 1.5 V				15	3H4	4.0	-	6.75	4.0	<u>D</u> 10	4.0	GA.
		000 "1"	Level	VIH					GGT + 70 :	-10/300 DE	MIT THE	97 78014	Vdc
(Vo	= 0.5 or 4.5 Vd			1 200	5.0	3.5	-	3.5	2.75	36 ms/pF	3.5	dy PR'14	
(Vo	= 1.0 or 9.0 Vd	lc)		- 61	10	7.0	-	7.0	5.50	3q\an 65	7.0	an APPTA	
(Vo	= 1.5 or 13.5 V	dc)			15	11.0	-	11.0	8.25	-	11.0	10 0	00
Output	Drive Current (AL Device)		Іон				20	cor . Jr.	ad/su os	O) = JH	97-14-19	mAdd
(VO	H = 2.5 Vdc)	Sou	rce	100	5.0	-3.0	-	-2.4	-4.2	36 ms/pF	-1.7	di PRTd	
(Val	H = 4.6 Vdc)	98 000		1.5	5.0	-0.64	-	-0.51	-0.88	Relan 85	-0.36	97月上19	
	H = 9.5 Vdc)			0.8	10	-1.6	-	-1.3	-2.25	_	-0.9	SHW_BSTU	1 10 Qrt
(Vo	H = 13.5 Vdc)			10	15	-4.2	-	-3.4	-8.8	-	-2.4	0070	E.A
(Vo	_ = 0.4 Vdc)	Sink	08	loL	5.0	0.64	_	0.51	0.88	_	0.36	_	mAdd
	= 0.5 Vdc)	-	0	0.8	10	1.6		1.3	2.25	_	0.9	omi <u>T</u> is	pphageF
	= 1.5 Vdc)			10	15	4.2	_	3.4	8.8	_	2.4	_	
	Drive Current (CL /CP Davi	ical	Іон						-			mAdo
	H = 2.5 Vdc)	Sou		TOH	5.0	-2.5		-2.1	-4.2	0.10	-1.7	7 salo9	matus.
	H = 4.6 Vdc)	300	100		5.0	-0.52	1,40 6	-0.44	-0.88	to rot 8	-0.36	Pigun	t refel
	H = 9.5 Vdc)			6.0	10	-1.3	1 ×	-1.1	-2.25	601- v	-0.9	0.0 ± x	
	H = 13.5 Vdc)			10	15	-3.6		-3.0	-8.8	AND X	-2.4	2.0 - X	
1700		214				-	-		-		-		
	L = 0.4 Vdc)	Sink	6.9	IOL	5.0	0.52	-	0.44	0.88	= 100 kg	0.36	-0 Ey6	mAdd
	L = 0.5 Vdc)			01	10 15	1.3	- 1	1.1	2.25 8.8		0.9	- 10	1
	L = 1.5 Vdc)	27.07	- 0.0			-			-		-		
-	urrent, Pin 2 or	200.0	210.0	lin	15	-	±0.05	-	±0.00001	±.05	La-1	± 0.5	μAdd
	urrent, Other In	7100.12	2000	lin	15	-	±0.1	-	±0.00001	±0.1	-	±1.0	μAdd
Input Ci	urrent, Other In	puts (CL/C	P Device)	lin	15	_	±0.3	-	±0.00001	±0.3	-	±1.0	μAdo
Input Ca	apacitance, Pin	2 or 14		Cin	to T	- 17700	-	-	25	umidinee	wred dos	eM Trbi	pF
	apacitance, Oth = 0)	er Inputs		Cin	-	-	-	-	5.0	7.5	Rv =	aq u ne tu 1.0 ×	pF
	nt Current (AL			IDD	5.0	†	5.0		0.005	5.0	-	150	μAdc
	Package)	Device)		,00	10		10	aracteris	0.010	10	given se	300	AAuc
11.61	rackage/			11000	15		20		0.015	20	h	600	esser
Outeses	nt Current (CL/	CR Davisal		1	5.0		20		0.005	20	LIVIUL.	150	μAdo
	Package)	Cr Device)		DD	10	RX	40		0.005	40	STREET,	300	μAdd
(rei	rackage/				15	76.9C	80		0.015	80	Сврас Т	600	marx2
0 :	Tames .	0				-	00		35	00	-	000	
	nt Current, Acti = Logic 1)	ve State		IDD	5.0	to anax	sol out h	no <u>ti</u> on o	80	onstalee	eld <u>e</u> su	munica	μAdo
				ed noise sig	15	kern <u>u</u> txe	or willing	87995818	125	rface re	a bres to	ovel by	end of
	Logic o/				15	-	1 017 15	d shall	125	SENSITOR	b agu a	201-	VO II
ca	Supply Curren apacitance (C _L) ming network (and at exte		IT (eve	5.0 10.0 15.0	J ₁	= (8 x 1 = (1.25	0 ⁻²) R _X × 10 ⁻¹) re: I _T i	R _X C _X f + 4C C _X f + 9C _X R _X C _X f + 1 n µA (one r in µF, C _L ii	$f + 2 \times 10^{-2}$ $2C\chi f + 3$ nonostab	0-5 CLf x 10-5 le switch	CLf	h.

^{*}Tlow = -55° C for AL Device, -40° C for CL/CP Device. Thigh = $+125^{\circ}$ C for AL Device, $+85^{\circ}$ C for CL/CP Device. #Noise immunity specified for worst-case input combination. Noise Margin both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc 2.0 Vdc min @ V_{DD} = 10 Vdc 2.5 Vdc min @ V_{DD} = 15 Vdc *The formulas given are for the typical characteristics only at 25° C.

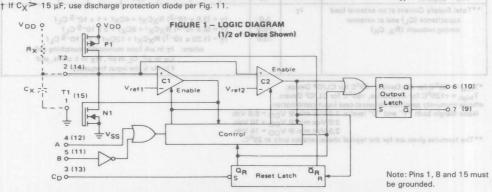
	-	office			T.	ac V	7		All Types		
	Chara	acteristic		импо	Symbol		V _{DD} Vdc	Min	Тур	Max	Unit
Output Rise Time	_ 80	0.0		80.0	tTLH	0.4	I www.	(byd.)	.0.,	epatio\	ns
tTLH = (1.35	ns/pF) CL	+ 33 ns		80.0		01	5.0	-	100	200	niV
tTLH = (0.60	ns/pF) CL	+ 20 ns		80.0		81	10	-	50	100	1
tTLH = (0.40	ns/pF) CL	+ 20 ns		1	1 4 66	0	15	Thirt	40	80	
Output Fall Time	0.0	- 01	3.95	1	THL	08	1	1		0 of V 0	ns
tTHL = (1.35	ns/pF) CL	+ 33 ns			14.98	81	5.0	-	100	200	
tTHL = (0.60	ns/pF) CL	+ 20 ns			1		10	Tovs.J	50	100	W ruge
tTHL = (0.40	ns/pF) CL	+ 20 ns				al	15	-104921	40	80	
Propagation Delay	Time	4.50		0.0	tpLH,	01			Vetet	0. f an 0.2 a	ns
A or B to Q or	ā				tPHL	21			(pbV 6	1 to 8.51 v	avi
tPLH, tPHI	= (0.90 r	ns/pF) CL + 255	5 ns			-	5.0	- Invad	300	600	-
		ns/pF) CL + 132			3.6	0.4	10	- consta	150	300	-30
		ns/pF) CL + 97			0.0	01	15	-	100	220	OV)
					0.71	81			(96V/-E	1.5 or 13.	ns
tPLH, tPHI	= (0.90	ns/pF) CL + 20!	5 ns				5.0	-	250	500	
		ns/pF) CL + 10			0.5-	0.8	10		125	250	3000
		ns/pF) CL + 82			AR 04	0.0	15	- 80	95	190	lovi.
Input Pulse Width		-2.25	6.1-	1	twh.	01	5.0	170	85	55V (±8 =)	ns
A, B or CD					twL	31	10	90	45	13.5 Vd	envi
					50.0	0.4	15	80	40	Sect En	Cave
Retrigger Time	8.0	2.25	1.3	1 -	a t _{rr}	01	5.0	0	-	sbV at0 =	ns
					5.4	21	10	0	-	with Vdc	(NOV)
							15	0	WG 97 (2) +	and Tardet	20000
Output Pulse Wid	th - Q or	ā	1.5-		acT	0.3	1100	80	Sour	= 2.6 Vdc	μs
Refer to Figures	8 and 9 f	or other values	of R _X a	nd Cx.	-0.62	0.8				= 4,6 Vdc	ovi.
Cx = 0.002	μF, Ry =	= 100 kΩ	1.1-	1	0.15	0.0	5.0	198	210	222	(Vo
^	S . C .	8.8-			8.0-	33	10	200	212	224	SVI
					0.62	0.4	15	202	214	226	
C _X = 0.1 μ					5.7	01	5.0	9.3	9.86	10.4	ms
^	^	8.8			3.0	31	10	9.5	10	10.5	(Vol
					1 00	-	15	9.6	10.14	10.7	0
C _X = 10 µl	Rx = 10	00 kΩ				91	5.0	0.915	0.965	1.015	s
DEAH O. 13	- "	0: 00000:0:				6	10	0.93	0.98	1.03	Dut Ci
					H. C. I	91	15	0.94	0.99	1.04	D jug
Pulse Width Matcl	between	circuits in	-	luz i	100(T ₁ - 7	T2)	5.0	-	± 5	±10	%
the same pack	age.				T ₁		10	-	±7.5	±15	Dug C
CX = 0.1 µF, 1	-	kΩ					15	-	±7.5	±15	m(V)

^{*} The formulae given are for the typical characteristics only.

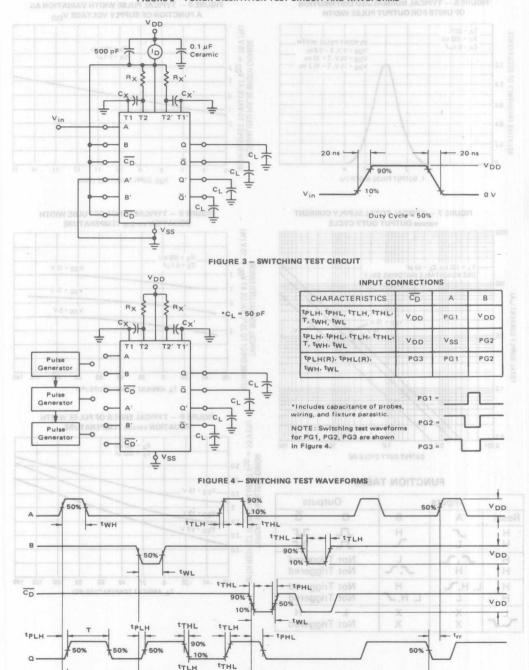
OPERATING CONDITIONS

External Timing Resistance	RX	700	5.0	BONNEY JUVD	Imp Such	kΩ
External Timing Capacitance	_ C _X	-	0	-	No	μF
					Limit †	-

The maximum usable resistance R_X is a function of the leakage of the capacitor C_X, leakage of the MC14538B, and leakage due
to board layout and surface resistance. Susceptability to externally induced noise signals may occur for R_X > 1 MΩ.







10%

₹PLH 50%

50%

tPHL.

FIGURE 5 - TYPICAL NORMALIZED DISTRIBUTION OF UNITS FOR OUTPUT PULSE WIDTH

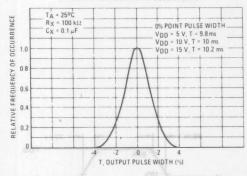


FIGURE 6 - TYPICAL PULSE WIDTH VARIATION AS A FUNCTION OF SUPPLY VOLTAGE VDD

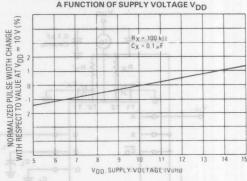


FIGURE 7 - TYPICAL TOTAL SUPPLY CURRENT

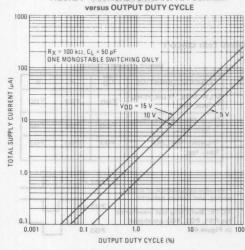
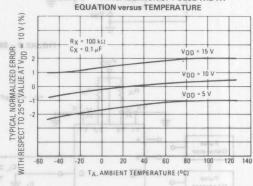


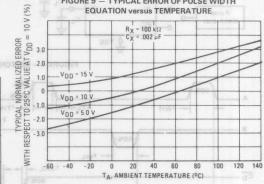
FIGURE 8 - TYPICAL ERROR OF PULSE WIDTH

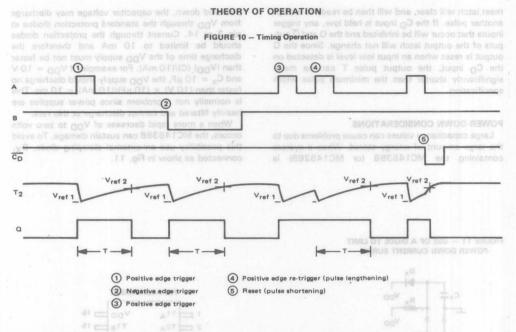


FUNCTION TABLE

	Inputs	an /	Outputs			
Reset	A	В	Q	ā		
H	5	7	7	7		
H	✓, \	J.\	Not Tr			
H	L, H, ℃	H L, H, J	Not Tr			
25	X	X	L Not Tr	H ggered		

FIGURE 9 - TYPICAL ERROR OF PULSE WIDTH





TRIGGER OPERATION

The block diagram of the MC14538B is shown in Figure 1, with circuit operation following.

As shown in Figures 1 and 10, before an input trigger occurs, the monostable is in the quiescent state with the Q output low, and the timing capacitor Cx completely charged to VDD. When the trigger input A goes from VSS to VDD (while inputs B and CD are held to VDD) a valid trigger is recognized, which turns on comparator C1 and N-Channel transistor N1 1. At the same time the output latch is set. With transistor N1 on, the capacitor Cx rapidly discharges toward VSS until Vref 1 is reached. At this point the output of comparator C1 changes state and transistor N1 turns off. Comparator C1 then turns off while at the same time comparator C2 turns on. With transistor N1 off, the capacitor CX begins to charge through the timing resistor, Rx, toward VDD. When the voltage across Cx equals Vref 2, comparator C2 changes state, causing the output latch to reset (Q goes low) while at the same time disabling comparator C2 2. This ends the timing cycle with the monostable in the quiescent state, waiting for the next trigger.

It should be noted that in the quiescent state C_X is fully charged to V_{DD} causing the current through resistor R_X to be zero. Both comparators are "off" with the total

device current due only to reverse junction leakages. An added feature of the MC14538B is that the output latch is set via the input trigger without regard to the capacitor voltage. Thus, propagation delay from trigger to Q is independent of the value of C_X , R_X , or the duty cycle of the input waveform.

RETRIGGER OPERATION

The MC14538B is retriggered if a valid trigger occurs 3 followed by another valid trigger 4 before the Q output has returned to the quiescent (zero) state. Any retrigger, after the timing node voltage at pin 2 or 14 has begun to rise from V_{ref 1}, but has not yet reached V_{ref 2}, will cause an increase in output pulse width T. When a valid retrigger is initiated 4, the voltage at T2 will again drop to V_{ref 1} before progressing along the RC charging curve toward V_{DD}. The Q output will remain high until time T, after the last valid retrigger.

RESET OPERATION

The MC14538B may be reset during the generation of the output pulse. In the reset mode of operation, an input pulse on \overrightarrow{CD} sets the reset latch and causes the capacitor to be fast charged to V_{DD} by turning on transistor P15. When the voltage on the capacitor reaches V_{ref} 2, the

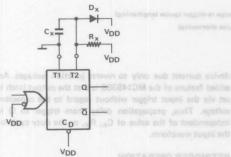
reset latch will clear, and will then be ready to accept powered down, the capacitor voltage may discharge another pulse. If the Cn input is held low, any trigger inputs that occur will be inhibited and the Q and Q outnuts of the output latch will not change. Since the Q output is reset when an input low level is detected on the Cn input, the output pulse T can be made significantly shorter than the minimum pulse width specification.

POWER-DOWN CONSIDERATIONS

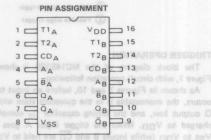
Large capacitance values can cause problems due to the large amount of energy stored. When a system containing the MC14538B (or MC14528B) is from VDD through the standard protection diodes at pin 2 or 14. Current through the protection diodes should be limited to 10 mA and therefore the discharge time of the VDD supply must not be faster than (V_{DD}) (C)/(10 mA). For example, if $V_{DD} = 10 \text{ V}$ and $C_x = 10 \mu F$, the V_{DD} supply should discharge no faster than (10 V) \times (10 μ F)/(10 mA) = 10 ms. This is normally not a problem since power supplies are heavily filtered and cannot discharge at this rate.

When a more rapid decrease of Vnn to zero volts occurs, the MC14538B can sustain damage. To avoid this possibility use an external clamping diode, Dx, connected as show in Fig. 11.

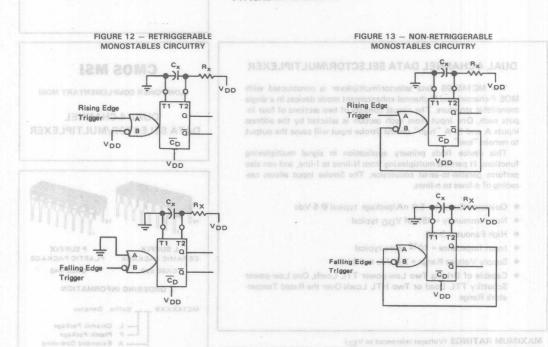
FIGURE 11 - USE OF A DIODE TO LIMIT POWER DOWN CURRENT SURGE



When the voltage on the capacitos reaches Viet 2, the



transistor N1 off, the capacitor Cy begins to charge



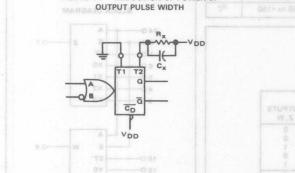


FIGURE 14 - REDUCTION OF POWER-UP

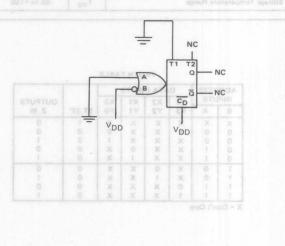


FIGURE 15 - CONNECTION OF UNUSED SECTIONS

DUAL 4-CHANNEL DATA SELECTOR/MULTIPLEXER

The MC14539B data selector/multiplexer is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. The circuit consists of two sections of four inputs each. One input from each section is selected by the address inputs A and B. A "high" on the Strobe input will cause the output to remain "low".

This device finds primary application in signal multiplexing functions, It permits multiplexing from N-lines to I-line, and can also perform parallel-to-serial conversion. The Strobe input allows cascading of n-lines to n-lines.

- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- Noise Immunity = 45% of VDD typical
- High Fanout > 50
- Input Impedance = 10¹² ohms typical
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range

MAXIMUM RATINGS (Voltages referenced to Vsc)

Rating	Symbol	Value	Unit
DC Supply Voltage	V _{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	Vin	-0.5 to V _{DD} + 0.5	Vdc
DC Current Drain per Pin	1	10	mAdc
Operating Temperature Range AL Device CL/CP Device	AT ME 16 -	-55 to +125 -40 to +85	°C
Storage Temperature Range	T _{stg}	-65 to +150	°C

TRUTH TABLE

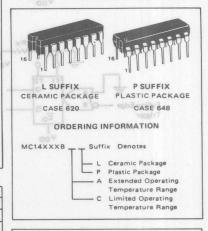
	RESS	D	ATAI	NPUTS	3				
INP	UTS	X3 X2 X		X1	XO		OUTPUTS		
В	A	Y3	Y2	Y1	YO	ST,ST'	Z, W		
X	X	X	· X	X	X	1	0		
0	0	OX V	X	X	0	0	0		
0	0	X	X	X	1	0	1		
0	1	X	X	0	X	0	0		
0	1	X	×	1	X	0	1		
1	0	X	0	X	X	0	0		
1	0	×	1	X	X	0	1		
1	1	0	X	X	X	0	0		
1	1	1	X	X	X	0	1		

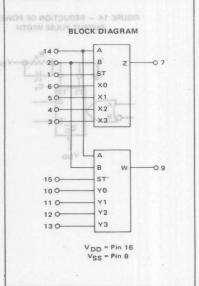
X = Don't Care

CMOS MS!

(LOW-POWER COMPLEMENTARY MOS)

DUAL 4-CHANNEL
DATA SELECTOR/MULTIPLEXER





ELECTRICAL CHARACTERISTICS

	dAL	1074	VDD	Tic	w*		25°C	olitalunt	h TCharm	igh *	
Characteristic		Symbol	Vdc	Min	Max	Min	Тур	Max	Min	Max	Unit
Output Voltage	"0" Level	VOL	5.0	-	0.05	-	0	0.05	+ 75 (34	0.05	Vdc
Vin VDD or 0	50	0.2	10		0.05	-	0	0.05	+ JQ (74	0.05	TATE.
08	4.0		15	-	0.05		0	0.05	+ 75 (40	0.05	1.172
	"1" Level	VOH	5.0	4.95	THIS	4.95	5.0	_	4.95	B/h[] III	Vdc
Vin O or VDD	001	OII	10	9.95	-	9.95	10	20 dS	9.95	an 8.51 -	MAG
007	08	-	15	14.95	-	14.95	15	an <u>B.E1</u>	14.95	n 37_0) =	STI
Input Voltage#	"O" Level	VIL						EN 856	15 (400	01 CC.07	Vdc
(Vo 4.5 or 0.5 Vdc)			5.0		1.5	-	2.25	1.5	<u>e</u> mi7	1.5	608901
(Vo 9.0 or 1.0 Vdc)			10	40	3.0	-	4.50	3.0	_344q1	3.0	Y,X
(VO = 13.5 or 1.5 Vdc)	210	-	15	-	4.0	-	6.75	4.0	1.7 ns/pF	4.0	(1d)
001	"1" Level	VIH					411	10.4 70.4	quan dest	1. 18d. h	1741
(VO = 0.5 or 4.5 Vdc)	-01		5.0	3.5		3.5	2.75	101	3.5	, THAL 'I	Vdc
(Vo 1.0 or 9.0 Vdc)			10	7.0	HJS	7.0	5.50	-	7.0	igruΩ of to	A Ing
(VO = 1.5 or 13.5 Vdc)	225		15	11.0	-	11.0	8.25	140 m	11.0	(sn Cl) -	1,197
Output Drive Current (AL	Device)	ГОН						80.23	Totade	FF DG. 01 T	mAdd
	Source	011	5.0	-3.0	-	-2.4	-4.2	an 08	-1.7	lan 8.0) -	1,192
(VOH = 4.6 Vdc)	245	-	5.0	-0.64	11147	-0.51	-0.88	Fit 091		(an C_f) =	Hdt
(VOH = 9.5 Vdc)	811		10	-1.6	_	-1.3	-2.25	82 m	-0.9	in 88_01 =	Hai
(VOH = 13.5 Vdc)	08	40	15	-4.2	-	-3.4	-8.8	_2n 88	-2.4	(an &LO) =	1493
(VOI = 0.4 Vdc)	Sink	IOL	5.0	0.64	HIM	0.51	0.88	_	0.36	or tugni	mAd
(V _{OL} = 0.5 Vdc)	145	0.	10	1.6	THAI	1.3	2.25		0.9	F JE191	1397
(VOL = 1.5 Vdc)	75	-	15	4.2	-	3.4	8.8	CA-LID P	2.4	triple."	TPL
Output Drive Current (CL/	CP Device)	ГОН	1				- 11	00-10	Tighter B.C	25661	mAde
	Source	011	5.0	-2.5	- 1	-2.1	-4.2	piger ent	1.7	svio-silun	not en
(VOH = 4.6 Vdc)			5.0	-0.52	-	-0.44	-0.88	-	-0.36	-	
(VOH = 9.5 Vdc)			10	-1.3	-	-1.1	-2.25	-	-0.9	-	
(V _{OH} = 13.5 Vdc)			15	-3.6	-	-3.0	-8.8	-	-2.4	-	
$(V_{OI} = 0.4 \text{ Vdc})$	Sink	IOL	5.0	0.52	-	0.44	0.88	-	0.36	-	mAde
$(V_{OL} = 0.5 \text{ Vdc})$		0.0	10	1.3	-	1.1	2.25	-	0.9	-	
(VOL = 1.5 Vdc)			15	3.6	-	3.0	8.8	-	2.4	-	
Input Current (AL Device)		lin	15	-	± 0.1	-	±0.00001	± 0.1	-	±1.0	μAdd
Input Current (CL/CP Devi	ce)	lin	15	-	± 0.3	-	±0.00001	'± 0.3	-	± 1.0	μAdd
Input Capacitance		Cin	IBAVW C	AA TIUS	HO TRET	2A - 13	5.0	7.5	-		pF
(V _{in} · 0)		-111				+					
Quiescent Current (AL Dev	ice)	IDD	5.0	-	5.0	- 0	0.005	5.0	-	150	μAdd
(Per Package)		.00	10		10	- "	0.010	10	-	300	
			15		20	-	0.015	20		600	
Quiescent Current (CL/CP	Device)	IDD	5.0	-	20	-	0.005	20	-	150	μAde
(Per Package)	-0.1007	.00	10		40		0.010	40	-0-	300	. MAGG
	7		15		80	_	0.015	80	_	600	
Total Supply Current**†		IT	5.0		, 00	1= 10	.85 μA/kH:		-0 0-	1	μAdd
(Dynamic plus Quiescer	it.	-	10				1.7 μA/kHz				MACIO
Per Package)	"		15				2.6 µA/kHz				
(C ₁ - 50 pF on all outp	uts, all					.1	SA-	0-1			
buffers switching)		6 1						-0-			

^{*}T_{low} -55°C for AL Device, -40°C for CL/CP Device.
Thigh = +125°C for AL Device, +85°C for CL/CP Device.

*Noise immunity specified for worst-case input combination.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range V_{SS} ≤ (V_{in} or V_{out}) € VDD.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD).

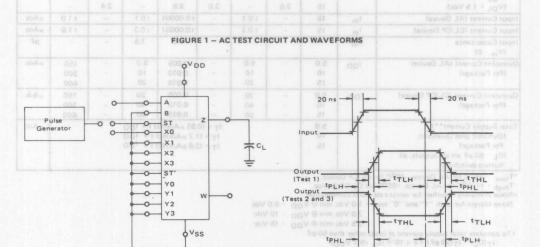
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ VDD = 5.0 Vdc 2.0 Vdc min @ VDD = 10 Vdc 2.5 Vdc min @ VDD = 15 Vdc

[†]To calculate total supply current at loads other than 50 pF: $1_T(C_L) = 1_T(50 \text{ pF}) + 2 \times 10^{-3} (C_L - 50) \text{ V}_{DD}$ where: 1_T is in μ A (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency. *The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS* (C1 = 50 pF, TA = 25°C)

Characteristic			Symbol	VDD	Min	Тур	Max	Unit
Output Rise Time	myT.	niiii	tTLH	Velo Min	Symbol		Characturisti	ns
tTLH = (3.0 ns/pF) CL + 30 ns				5.0	JoV	100	200	srlöV ragtu
tTLH = (1.5 ns/pF) CL + 15 ns				10	20	50	100	gV mV
tTLH = (1.1 ns/pF) CL + 10 ns			0.05	15	-	40	80	
Output Fall Time	5.0	4.98	THL	so I as	HOV	Inches Parket		ns
tTHL = (1.5 ns/pF) CL + 25 ns				5.0	- no.	100	200	60 2V
t _{THL} = (0.75 ns/pF) C _L + 12.5 ns				10	-	50	100	
t _{THL} = (0.55 ns/pF) C _L + 9.5 ns				15		40	80	
Propagation Delay Time	2.25	34	tPLH,	- 0.8	-		(sav 2.0 to	ns
X, Y Input to Output			tPHL	- 01				0.0 010
tPLH, tPHL = (1.7 ns/pF) CL + 125	ns		4.0	5.0	-	210	420	EVO 13.
tpLH, tpHL = (0.66 ns/pF) CL + 57	ns			10	HIV	90	180	Ger.
tpLH, tpHL = (0.55 ns/pF) CL + 45	ns	as		15	7910	70	140	20 - AVI
A Input to Output			tPLH	7.0			laby 0.6 m	ns v
tpLH = (1.7 ns/pF) CL + 140 ns				5.0	-	225	450	an ovi
tpl H = (0.66 ns/pF) C1 + 77 ns				10	-	110	220	
tpLH = (0.5 ns/pF) CL + 60 ns				15	HOI	85	170	avirO tuqti
tpHI = (1.7 ns/pF) C _I + 160 ns			tPHL	5.0	_	245	490	ns
tpHL = (0.66 ns/pF) CL + 82 ns		6.1-		10 01	_	115	230	6 = HOA)
tpHL = (0.5 ns/pF) CL + 65 ns				15		90	180	Nou = 13
Strobe Input to Output			tPLH.	so los	Jol	Simile	(sav)	o = ns v
tpLH tpHL = (1.7 ns/pF) CL + 60 n			tPHL	5.0	300	145		(Vol = 0.1)
tplH, tpHL = (0.66 ns/pF) CL + 42		3.6	2.77	C 10	_	75	150	IVOL = T
tpLH, tpHL = (0.5 ns/pF) CL + 35 n				15	_	60	120	10,1

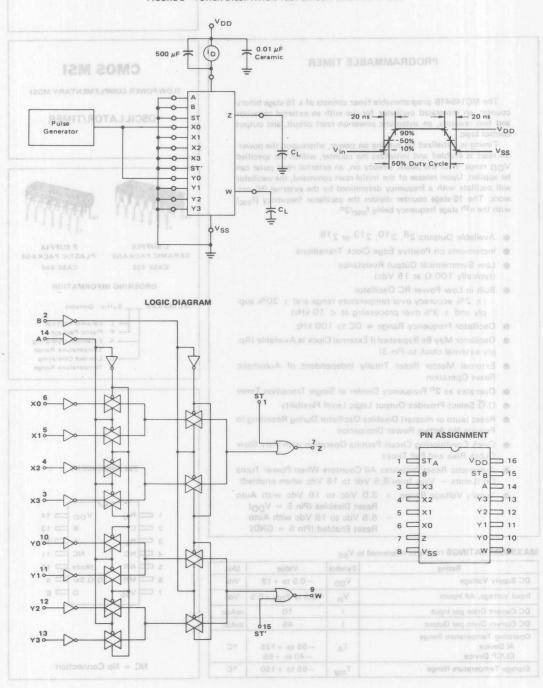
* The formulae given are for the typical characteristics only.



Still, typeword, shield altook to appellow a Input Connections for TTLH, TTHL, TPHL, TPHL, TPLH of Civilian and another than the shield of the control of th

TEST	STROBE	А	X0
2 3	Gnd	Gnd	P. G
	P. G.	Gnd	V _{DD}
	Gnd	P. G.	V _{DD}





MC14541B

PROGRAMMABLE TIMER

OWER DISSIPATION TEST CINCUIT AND WAVEFORM

The MC14541B programmable timer consists of a 16-stage bihary counter, an integrated oscillator for use with an external capacitor and two resistors, an automatic power-on reset circuit, and output control logic.

Timing is initialized by turning on power, whereupon the poweron reset is enabled and initializes the counter, within the specified VDD range. With the power already on, an external reset pulse can be applied. Upon release of the initial reset command, the oscillator will oscillate with a frequency determined by the external RC network. The 16-stage counter divides the oscillator frequency (fosc) with the nth stage frequency being fosc/2n.

- Available Outputs 28, 210, 213 or 216
- Increments on Positive Edge Clock Transitions
- Low Symmetrical Output Resistance (typically 100Ω at 15 Vdc)
- Built-in Low Power RC Oscillator (± 2% accuracy over temperature range and ± 20% supply and ± 3% over processing at < 10 kHz)
- Oscillator Frequency Range ≈ DC to 100 kHz
- Oscillator May Be Bypassed if External Clock Is Available (Apply external clock to Pin 3)
- External Master Reset Totally Independent of Automatic Reset Operation
- Operates as 2ⁿ Frequency Divider or Single Transition Timer
- Q/Q Select Provides Output Logic Level Flexibility
- Reset (auto or master) Disables Oscillator During Resetting to Provide No Active Power Dissipation
- Clock Conditioning Circuit Permits Operation with Very Slow CLock Rise and Fall Times
- Automatic Reset Initializes All Counters When Power Turns On (Limits - V_{DD} from 8.5 Vdc to 18 Vdc when enabled)
- Supply Voltage Range = 3.0 Vdc to 18 Vdc with Auto Reset Disables (Pin 5 = V_{DD}) = 8.5 Vdc to 18 Vdc with Auto
 - Reset Enabled (Pin 5 = GND)

MAXIMUM RATINGS (Voltages referenced to VSS

Rating	Symbol	Value	Unit	
DC Supply Voltage	V _{DD}	-0.5 to +18	Vdc	
Input Voltage, All Inputs	V _{in}	-0.5 to V _{DD} +0.5	Vdc	
DC Current Drain per Input	1	10	mAdo	
DC Current Drain per Output	1	45	mAdo	
Operating Temperature Range Al Device CL/CP Device	TA	-55 to +125 -40 to +85	°C	
Storage Temperature Range	T _{stg}	-65 to +150	°C	

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

OSCILLATOR/TIMER

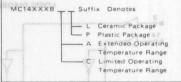




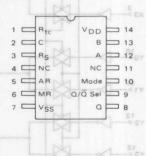
CERAMIC PACKAGE **CASE 632**

PLASTIC PACKAGE **CASE 646**

ORDERING INFORMATION



PIN ASSIGNMENT



NC = No Connection

ELECTRICAL CHARACTERISTICS

shint sold	Typ	51450	VDD	Tlow*		25°C		sississis	Thigh*		
Characteristic	1	Symbol	Vdc	Min	Max	Min	Тур	Max	Min	Max	Unit
Output Voltage	"0" Level	VOL	5.0	5.0	0.05	-	0	0.05	+ 10 (4)	0.05	Vdc
Vin = VDD or 0	0.0	02	10	01 _	0.05	-	0	0.05	+ 10 (No	0.05	BILLIA
08	.08		15	37 _	0.05	_	0	0.05	+ 10 (80	0.05	BUTT
203	"1" Level	Vон	5.0	4.95	JHITT	4.95	5.0	-	4.95	smiT Ils	Vdc
Vin = 0 or VDD	001	*OH	10	9.95	_	9.95	10	_an 89	9.95	un a.t) =	IHTI
VIN COLVEDO	99		15	14.95		14.95	15	12.5_ns	14.95	- (0 <u>7</u> 6 m	THIS
Input Voltage#	"0" Level	VIL		27				8.B ns	To tade	in earth	Vdc
(V _O = 4.5 or 0.5 Vdc)	O LOVE!	- IL	5.0		1.5	_	2.25	1.5	Closek to	1.5	spago
$(V_0 = 9.0 \text{ or } 1.0 \text{ Vdc})$	3.5		10	6.0	3.0		4.50	3.0	(Figlin V.	3.0	HUGI
$(V_0 = 13.5 \text{ or } 1.5 \text{ Vdc})$	1.25		15	01	4.0		6.75	4.0	Tq\sn 88.1	4.0	HINK
	0.0		15	-	4.0		0.75	4.0	Gehen 8.	11111	Vdc
	"1" Level	VIH		2.5	JH9!	2.5	2.75	0 (216	3.5	ion Delay	Vac
$(V_0 = 0.5 \text{ or } 4.5 \text{ Vdc})$	0.0		5.0	3.5 7.0	H_lgl	3.5	- Total (20)	$C_1 + 59$	7.0) = H1d1	11491
$(V_0 = 1.0 \text{ or } 9.0 \text{ Vdc})$	3.5		10	100		7.0	5.50 8.25	0 0 + 3	11.0	() = H_1q1	THE
$(V_0 = 1.5 \text{ or } 13.5 \text{ Vdc})$	2.0		15	11.0	-	11.0	8.25	30 4 13	11.0	0.00.000	Large .
Output Drive Current (AL	Device)	ІОН		0.8	D-M Der			-		ae Width	mAde
(VOH = 2.5 Vdc)	Source	300	5.0	7.96	(to)HIM	6.42	12.83	-	4.49	-	
(VOH = 9.5 Vdc)	28		10	4.19	-	3.38	6.75	-	2.37	-	
(VOH = 13.5 Vdc)	7.1	U.S.O.	15	16.3	-	13.2	26.33	-	9.24	-	-
(VOL = 0.4 Vdc)	Sink	loL	5.0	1.93	101	1.56	3.12	O KENEL O	1.09	autisti ass	mAd
(VOL = 0.5 Vdc)	12.50	OL.	10	4.96	_	4.0	8.0	-	2.8	_	
(VOL = 1.5 Vdc)	0.8		15	19.3		15.6	31.2		10.9	- ,	J. 6 0
Output Drive Current (CL/	CP Davisal	1000			(A)MM					10407100	mAd
(V _{OH} = 2.5 Vdc)		OHUE	5.0	5.1	_	4.27	12.83	_	3.5		mAd
	Source		10	The second		2.25	6.75		1.85		-
(V _{OH} = 9.5 Vdc)			15	2.69		8.8	26.33	ne typica	7.22	day gives	miol e
(V _{OH} = 13.5 Vdc)			-		_			_		_	
(V _{OL} = 0.4 Vdc)	Sink	INS OF 35	5.0	1.24	-	1.04	3.12	SSIPATE	0.85	1-13m	FIG
(V _{OL} = 0.5 Vdc)	WAVEFO		10	3.18	-	2.66	8.0	ROBEV	2.18	-	
(V _{OL} = 1.5 Vdc)			15	12.4	-	10.4	31.2	-	8.50	-	
Input Current (AL Device)		lin	15	-	±0.1	-	±0.00001	±0.1	-	±1.0	μAdd
Input Current (CL/CP Devi	ce)	lin	15	-	±0.3	-	±0.00001	±0.3	-	±1.0	μAde
Input Capacitance		Cin	-	-	-	-	5.0	7.5		-	pF
$(V_{in} = 0)$	-					11.15-4		-			
Quiescent Current (AL Dev	ice)	10781	0.000					25	-0-		μAdd
	BA -0-	103811	5.0		5.0	_	0.005	5.0		150	
(Pin 5 is High)		IDD	10	_	10	_	0,010	10		300	
Auto Reset Disabled	000	9 00	15	_	20	_	0.015	20	-0-0	600	
Quiescent Current (CL/CP	Daviss	1		-			0-0	Mods	-0-6		0 -1
dulescent Current (CL/CF)	Device)	0	5.0		20	12本	0.005	20	-0-0	150	μAd
(Die E is High)	8-0-	Inn	10	-	40	-	0.005	40	101	300	
(Pin 5 is High) Auto Reset Disabled		IDD	15	_	80	=	0.010	80		600	
			15	-	80		0,015	80	1	600	
Auto Reset Quiescent Curre	ent						-	1			μAdd
0-		and .		*	L LIST	10000	Vss.	Q-	-		
-sev ±		IDDR	10	-	250	-	30	250	-	1500	
(Pin 5 is low)			15	-	500	-	82	500	-	2000	
Supply Current**†	1.7		1000			1773					μAde
(Dynamic plus Quiescen	t)		5.0	1		ID = ((0.4 µA/kHz)	f + IDD	and Cte	(51)	
		-ID	10	$I_D = (0.8 \mu A/kHz) f + I_{DD}$							
	175	100	15				1.2 µA/kHz)				

eT_{low} = -55°C for AL Device, -40°C for CL/CP Device. T_{high} = +125°C for AL Device, +85°C for CL/CP Device. #Noise immunity specified for worst-case input combination.

Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc 2.0 Vdc min @ V_{DD} = 10 Vdc 2.5 Vdc min @ V_{DD} = 15 Vdc

tWhen using the on chip oscillator the total supply current (in μ Adc) becomes : I_T = I_D + 2 C_{tc} V_{DD} f x 10⁻³ where I_D is in μ A, C_{tc} is in

pF, VDD in Volts DC, and f in kHz. (see fig. 3)

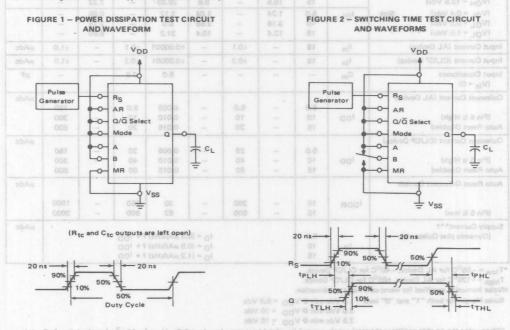
Dissipation during power-on with automatic reset enabled is typically 50µA @ VDD = 10Vdc.

**The formula given is for the typical characteristics only.

SWITCHING CHARACTERISITCS* (CL = 50 pF, TA = 25°C)

Characteristic	26°C		V _{DD} Symbol	Typical Vdc	Min	Тур	Max	Unit
Output Rise Time	gyT	- nife	tTLH	Miles Niles	Symbol		Cheresteration	ns
tTLH = (3.0 ns/pF) CL + 30 ns			80.0	5.0	Vol	100	200	rloV-tugtuC
tTLH = (1.5 ns/pF) CL + 15 ns			ap.o.	_ 10	-	50	100	V=mV
tTLH = (1.1 ns/pF) CL + 10 ns			0.05	_ 15	-	40	80	
Output Fall Time	0.8	4.95	tTHL	50.4 0.8	HOV	I leded "F"		ns
tTHL = (1.5 ns/pF) CL + 25 ns			1 - 1	5.0	-	100	200	Vin = 0.0
tTHL = (0.75 ns/pF) CL + 12.5 ns			- 1	10 at	-	50	100	
tTHL = (0.55 ns/pF) CL + 9.5 ns				15		40	80	and and acceptant
Propagation Delay, Clock to Q (28	Output)		tPLH	0.0	21,4	1000	laky 80 to 2	μs
tpLH, tpHL = (1.7 ns/pF) CL + 3415 ns			tPHL	5.0	-	3.5	10.5	
tpLH tpHL = (0.66 ns/pF) CL + 1217 ns			0.0	10	-	1.25	3.8	st = 0A)
tpLH, tpHL = (0.5 ns/pF) CL + 87	5 ns		4.6	15		0.9	2.9	. 0.,
Propagation Delay, Clock to Q (216	Output)	3.5	tPHL	20 01	1 111	The same of	i or 4.5 Vdc)	μs
tpHL tpLH = (1.7 ns/pF) CL + 5915 ns			tPLH	5.0	-	6.0	18	17 - 07/
tpHL tpLH = (0.66 ns/pF) CL + 3	467 ns			10	-	3.5	10	(VO = 1.
tpHL, tpLH = (0.5 ns/pF) CL + 24	75 ns		-	15	-	2.5	7.5	911
Clock Pulse Width	1	6.42	tWH(cl)	5.0	900	300	TalsV 3.1	ns
	12.83			10	300	100	Lib V de)	HOV
	8.75	3.38		15	225	85	700 V 03	HOV
Clock Pulse Frequency (50% Duty	Cycle)		fcl	5.0		1.5	A Vdel	MHz
				10	_101	4.0	-	
				15	-	6.0	(S Vde)	10 A
MR Pulse Width	2.76	0.01	twH(R)	5.0	900	300	100 / 01	ns
				10	300	100		winG pagrat
		4.27	-	15 0	225	85	(ab V d.)	(VOH =

* The formulae given are for the typical characteristics only.



EXPANDED BLOCK DIAGRAM - 8 HAUSIA

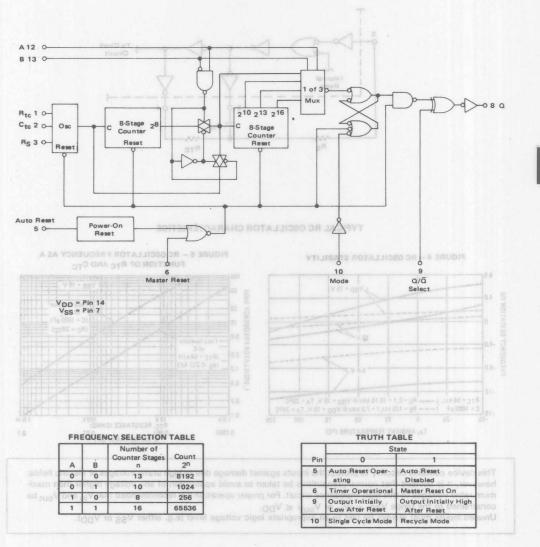
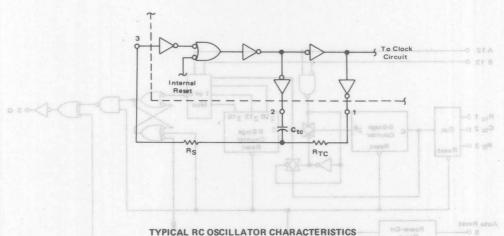
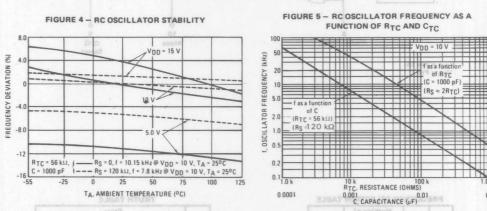


FIGURE 3 - OSCILLATOR CIRCUIT USING RC CONFIGURATION





This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields: however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leqslant (V_{in} \text{ or } V_{out}) \leqslant V_{DD}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g. either V_{SS} or V_{DD}).

OPERATING CHARACTERISTICS

With Auto Reset pin set to a "0" the counter circuit is initialized by turning on power. Or with power already on, the counter circuit is reset when the Master Reset pin is set to a "1". Both types of reset will result in synchronously resetting all counter stages independent of counter state. Auto Reset pin when set to a "1" provides a low power operation.

The RC oscillator as shown in Figure 3 will oscillate with a frequency determined by the external RC network i.e.,

ELBATTERS =
$$\frac{1}{2.3 \, \text{Rtc}^{\text{C}} \text{tc}}$$
 if (1 kHz \leq f \leq 100 kHz)

and
$$R_S \approx 2 R_{tc}$$
 where $R_S \geqslant 10 \text{ k}\Omega$

The time select inputs (A and B) provide a two-bit address to output any one of four counter stages (28, 210, 213 and 216). The 2ⁿ counts as shown in the Frequency Selection Table represents the Q output of the Nth stage of the counter. When A is "1", 216 is selected for both XO has XI advantaged and advantage states of B. However, when B is "0", normal counting is interrupted and the 9th counter stage receives its clock directly from the oscillator (i.e., effectively outputing 28).

The $\Omega/\overline{\Omega}$ select output control pin provides for a choice of output level. When the counter is in a reset condition and $\Omega/\overline{\Omega}$ select pin is set to a "0" the Ω output is a "0", correspondingly when $\Omega/\overline{\Omega}$ select pin is set to a "1" the Ω output is a "1".

When the mode control pin is set to a "1", the selected count is continually transmitted to the output. But, with mode pin "0" and after a reset condition the RS flip-flop (see Expanded Block Diagram) resets, counting commences, and after 2ⁿ⁻¹ counts the RS flip-flop sets which causes the output to change state. Hence, after another 2ⁿ⁻¹ counts the output will not change. Thus, a Master Reset pulse must be applied or a change in the mode pin level is required to reset the single cycle operation.

DIGITAL TIMER APPLICATION

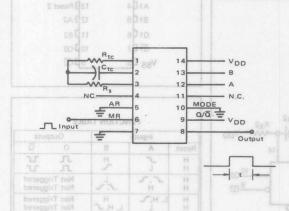
MOTOROLA

When Master Reset (MR) receives a positive pulse, the internal counters and latch are reset. The Q output goes high and remains high until the selected (via A and B) number of clock pulses are counted, the Q output then goes low and remains low until another input pulse is received.

This "one shot" is fully retriggerable and as accurate as the input frequency. An external clock can be used (pin 3 is the clock input, pins 1 and 2 are outputs) if additional accuracy is needed.

Notice that a setup time equal to the desired pulse width output is required immediately following initial power up, during which time Q output will be high.

3



With Auto Reset pin set to a "O" the counter circuit is

DUAL MONOSTABLE MULTIVIBRATOR (RETRIGGERABLE, RESETTABLE)

The MC14548B is identical in pinout to the MC14538B and the MC14528B.

This dual monostable multivibrator may be triggered by either the positive or the negative edge of an input pulse, and will produce an output pulse over a wide range of pulse widths. Because the device has conditioned trigger inputs, there are no trigger-input rise and fall time restrictions. The output pulse width is determined by the external timing components, Rx and Cx. The device has a reset function which forces the Q output low and Q output high, regardless of the state of the output pulse circuitry.

- Unlimited Rise and Fall Times Allowed on the Trigger Inputs
- Output Pulse Width is Independent of the Trigger Pulse Width
- Latched Trigger and Reset Inputs
 Annual Control of the Co
- Supply Voltage Range = 3.0 to 18.0 Vdc. at mig poster DVD market
- Recommended for all new designs in lieu of the 14528B and
- For pulse widths $< 1 \mu S$, use the HC4538 or MC14528B

MOTTANIANA BLOCK DIAGRAM MRx1eeH retasM nedW VDD oo leaster O output goes (S bne A sly) Trigger B1-7 01 and aidT -VDD eduq besies of to the desired pulse a totout is required immediately following initial 10_{:Q2} A2 12 Trigger B2_11 9 02 Inputs Reset 2 13 V_{DD}=Pin 16 VSS = Pin 1, Pin 8, Pin 15 R_X and C_X are external components

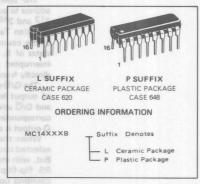
This document contains information on a new product. Specifications and information herein are subject to change without notice.

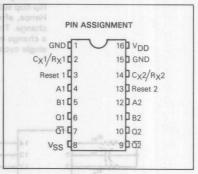
CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

DUAL

(RETRIGGERABLE, RESETTABLE) MONOSTABLE MULTIVIBRATOR





	Inputs	200	Outputs		
Reset	A	В	Q	ā	
H	7	7	7	T.	
H	√.~	プ.プ		ggered ggered	
H	L, H;_ L	L, H,		ggered ggered	
~~	X	X	L Not Tr	H	

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Oct. 1983 EUR

IMAXIMUM RATINGS (Voltages referenced to VSS)

	Rating	aeqyT lfA	Symbol	Value	Unit
DC Supply Voltage	e Mark	Тур	V _{DD}	-0.5 to +18	Vdc
Input Voltage, All	Inputs	100	-V _{in}	-0.5 to V _{DD} +0.5	Vdc
DC Current Drain	per Pin	0.6	-1	31 10 JHT	mAdo
Operating Tempera L Device P Device	ature Rang	200 200 100	-T _A	-55 to +125 -40 to +85	°C
Storage Temperat	ure Range		T _{stg}	-65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended that Vin and Vout be constrained to the range GND \geq (V_{in} or V_{out}) \geq V_{CC} .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or VCC).

ELECTRICAL CHARACTERISTICS

	10		V _{DD}	Tlo	w*		25°C		Thi	gh*	
Characteristic		Symbol	Vdc	Min	Max	Min	Тур	Max	Min	Max	Unit
Output Voltage	"O" Level	Vol	5.0	-	0.05	_	0	0.05	_	0.05	V
$V_{in} = V_{DD}$ or 0		OL.	10	_	0.05	-	0	0.05	-	0.05	
60 -			15	-	0.05	-	0	0.05		0.05	-051
	"1" Level	V _{OH}	5.0	4.95	-	4.95	5.0	_ 8	4.95	leset lesel	V
$V_{in} = 0 \text{ or } V_{DD}$		OII	10	9.95	-	9.95	10	-	9.95	_	
			15	14.95	- 1 - Tes	14.95	15	-	14.95	ut Rise and	net
Input Voltage**	"O" Level	VIL	- 6							1929	V
$(V_0 = 4.5 \text{ or } 0.5 \text{ Vdc})$		- IL	5.0	_	1.5	_	2.25	1.5	_	1.5	
$(V_0 = 9.0 \text{ or } 1.0 \text{ Vdc})$			10		3.0	-	4.50	3.0	_	3.0	
(V _O = 13.5 or 1.5 Vdc)	timit o		15	-	4.0	-	6.75	4.0	-	4.0	gal
2.11	"1" Level	VIH						10 10	O - risbiv	saturi ruga	V
$(V_0 = 0.5 \text{ or } 4.5 \text{ Vdc})$	CONTRACT	*IH	5.0	3.5	_	3.5	2.75	_ 4	3.5	= (5 pF.	(O
$(V_0 = 1.0 \text{ or } 9.0 \text{ Vdc})$	210		10	7.0		7.0	5.50		7.0		
$(V_0 = 1.5 \text{ or } 13.5 \text{ Vdc})$	640		15	11.0		11.0	8.25	_	11.0	_	
V 1611	8.08		0.2	11.0		1110	0.20	- 034.5	B- 18.	H 50.0 -	X .
Output Drive Current	Sauras	Іон	5.0	-3.0	- 1	-2.4	-4.2		-1.7		mA
$(V_{OH} = 2.5 \text{ Vdc})$ $(V_{OH} = 4.6 \text{ Vdc})$	Source		5.0	-0.64		-0.51	-0.88	-	-0.36		
$(V_{OH} = 9.5 \text{ Vdc})$	6.8		10	-1.6		-1.3	-2.25	<u> 200</u> 0	-0.9	1.0 µF.	CX
$(V_{OH} = 3.5 \text{ Vdc})$	86		15	-4.2		-3.4	-8.8	_	-2.4		
			-								-
$(V_{OL} = 0.4 \text{ Vdc})$	Sink	IOL	5.0	0.64	- JŦ	0.51	0.88	voni s nee	0.36	VI resiVV os	mA
$(V_{OL} = 0.5 \text{ Vdc})$	12		10	1.6	7 -	1.3	2,25 8.8	08.0	2.4	Same_sac	.3
$(V_{OL} = 1.5 \text{ Vdc})$			15			3.4	0.0		2.4		8.00
				1			±				
Input Current, Pin 2 or 14		lin	15	-	±0.05	-	0.00001	±0.05	NOTTION	±0.5	μА
							±				
Input Current, Other Inputs	- 1	o lin	15	-	±0.1	-	0.00001	±0.1	netEledR g	±1.0	μА
Input Capacitance, Pin 2 or	14 -	C _{in}		-	o - [-	25	- 6	g Cap in ane	nimit lanns	pF
Input Capacitance, Other In	outs of the menture	C _{in}	o th at the		olt to noll d bli m rla y		5.0	7.5	euriste ra euriste ra	orra Tuoyal I	-pF
$(V_{in} = 0)$.QM	1 > XHS	acour fo	ignals may	d noise 4	ally induce	matxs of y	nilldir
Quiescent Current, Standby	State	IDD	5.0	-		-	10	20	-		μА
(Q = Logic 0)			10	SCEIPT	BCI TNIA	-	25	40	-		
$(\overline{Q} = \text{Logic 1})$	ad at hot or a	Thora and	15	-		-	50	80	-		
Quiescent Current, Active S	tate	IDD	5.0	-	-	-		_	-	-	μА
(Q = Logic 1)	115) - Extern	ns f anifi)	10	-	Sebera	raiai—A ,	dugni repul	e o dg e te	vines9 —	Pins 4-12	LAZ-
$(\overline{Q} = \text{Logic 0})$	a to ground thro	are descharg	15	-	921010	GENERAL DE	egger the	H LLLY S	miq_eserI)	lo_ verbie	no Is

^{*} T_{low} = -55°C for L Device, -40°C for P Device.

Thigh = +125°C for L Device, +85°C for P Device.

** Noise immunity specified for worst-case input combination.

Noise Margin for both "1" and "0" level = 1.0 Vdc min at V_{DD} = 5.0 Vdc:

2.0 Vdc min at V_{DD} = 10 Vdc

2.5 Vdc min at V_{DD} = 15 Vdc

				zirU		udaV.	osleny2	All Types		
	Character	ristic			mbol	V _{DD} Vdc	Min	Тур	Max	Unit
Output Transition Ti	me .	ternion Jur	TE	-						ns
Q or Q				ob V t-	TLH.	V 05.00-	niV-	100	200	us Voltage.
				t	THL	10	-	50	100	
operation it is reco				mAdi:		01 15	1 -	40	80	Current Dra
Propagation Delay T	imes niV 16			4. 6	PLH [,]				serature Rang	ns meT gridet
A or B to Q or Q				20	PHL	5.0	AT-	200	400	L Device
						10	H A'	100	200	
						15	1	80	160	P Davice
Reset to Q or Q		ND or Vc		30		-85 to	gzsT .		rature Range	ns
				-		5.0	I Bis.	185	370	
				- 1		10	-	90	180	
						15	-	75	150	
Input Pulse Width				P	Win	5.0	50	25 181	HARACTER	ns ns
A, B or Reset					wol ^T	10	30 20	15 10	_	
Retrigger Time	M xsVi	Typ	rillin	xalifi	t _{rr}	5.0	Symbol		oltzh <u>e</u> toenn	ns
Input A or B				0.05		10	VOL	firveJ "O"	-	put Voltage
- 0.05	0.05	0	-	0.05	-	15	1		- 010	noV = of
Recovery Time	0.06	0		30.9	rec	5.0			_	ns
Reset Inactive to A	A or B			-	38		HoV	level "1"	-	
96 - 36	.0	10	9.95		85	15			- 00	V 10 0 = m
Input Rise and Fall T	ime		14.95	-t	r, tfee	15 14				
Reset						5	_JvL	laveJ "0"	15	μs
				1.5		10	1 1	_	(ab 4 8.0 1	Va - 4.5 0
		4.50		3.0		15	1 -	_	10040	0.0
Input A or B	0.8	6.75	-	4.0		157	ne	o limit	or 1.5 Vdcl.	μs
Output Pulse Width					T		1	1240		μs
$C_X = 15 pF, R_X =$	5 ΚΩ					5.0	HILY	1340	feding 2 h s	Va = 0.5
				1 -		10	1	710		0.1 = 0.0
						15		540	CHU P DT	2 1
$C_X = 0.01 \mu\text{F}, R_X$	= 10 ΚΩ			-		5.0	1	90.5		ms
			-2.4			10	HOI	77	menu	
			18.0-				-	100000000000000000000000000000000000000	(ab)	VOH = 2.5
$C_X = 1.0 \mu F$, $R_X =$	100 ΚΩ					5.0		58	Vdc)	B.A SHOV
- 4.5						10 15		56 49	5 Vdo)	$V_{OH} = 9.6$ $V_{OH} = 13$
Pulse Width Match b	etween circ	uits in	0.61	T ₁	- T2	5.0	161	Sink	(de)	4.0 - InV
the same package					T1 8.	5.0	-	±1	- (abV	8.0 % INV
$C_X = 0.1 \mu F, R_X =$	100 kΩ			-	S	10	-	±1	- lobV	8.1 - 10V
						15	-	±1		
PERATING CONDITI	ONS									
		1 2								
External Timing Resis	stance			03	RX	_81	5.0	_	Other Impote	kΩ

* The maximum allowable values of R_X and C_X are a function of the leakage of capacitor C_X, the leakage of the MC14548B, and leakage due to board layout and surface resistance. Values of R_X and C_X should be chosen so that the maximum current into pin 2 or pin 14 is 10 mA. Susception tibility to externally induced noise signals may occur for $R_X < 1 M\Omega$.

PIN DESCRIPTIONS

INPUTS

A1, A2 (Pins 4, 12) — Positive-edge trigger inputs. A rising-edge signal on either of these pins will trigger the corresponding multivibrator when there is a high voltage level on the B1 or B2 input.

B1, B2 (Pins 5, 11) — Negative-edge trigger inputs. A falling-edge signal on either of these pins will trigger the corresponding multivibrator when there is a low voltage level on the A1 or A2 input.

Reset 1, Reset 2 (Pins 3, 13) — Reset inputs (active low). When a low voltage is applied to one of these pins, the Q output of the corresponding multivibrator is reset to a low voltage and the Q output is

ponents. These pins are tied to the common points of the external

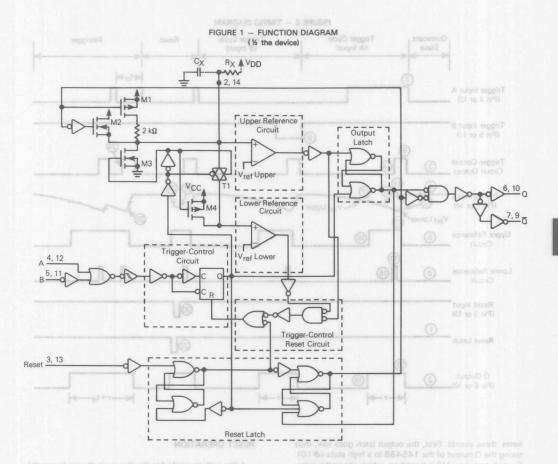
timing resistors and capacitors (see the Block Diagram).

GND (Pins 1 and 15) — External ground. The external timing capacitors discharge to ground through these pins.

Q1, Q2 (Pins 6, 10) - Noninverted monostable outputs. These pins (normally low) pulse high when the multivibrator is triggered at either the A or the B input. The width of the pulse is determined by the external timing components, R_X and C_X.

\$\overline{\text{Q1}}\$ (Pins 7, 9) — inverted monostable outputs. These pins

CX1/RX1 and CX2/RX2 (Pins 2 and 14) — External timing com-



CIRCUIT OPERATION

Figure 4 shows the 14548B configured in the retriggerable mode. Briefly, the device operates as follows (refer to Figure 1). In the quiescent state, the external timing capacitor, Cx, is charged to VpD. When a trigger occurs, the Q output goes high and Cx discharges quickly to the lower reference voltage (Vref Lower $\approx 1/3$ VpD). Cx then charges, through Rx, back up to the upper reference voltage (Vref Upper $\approx 2/3$ VpD), at which point the one-shot has timed out and the Q output goes low.

The following, more detailed description of the circuit operation refers to both the function diagram (Figure 1) and the timing diagram (Figure 2).

QUIESCENT STATE Ought of send regular

In the quiescent state, before an input trigger appears, the output latch is high and the reset latch is high (# 1 in Figure 2). Thus the Q output (pin 6 or 10) of the monostable multivibrator is low (# 2, Figure 2).

The output of the trigger-control is low (#3), and transistors M1, M2, and M3 are turned off. The external timing capacitor, Cx, is charged to Vpp (#4), and the upper reference circuit has a low output (#5). Transistor M4 is turned on and transmission gate T1 is turned off. Thus the lower reference circuit has Vpp at the noninverting input and a resulting low output (#6).

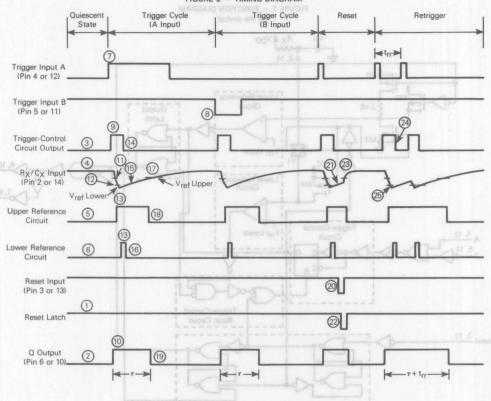
In addition, the output of the trigger-control reset circuit is low.

TRIGGER OPERATION

The 14548B is triggered by either a rising-edge signal at input A (#7) or a falling-edge signal at input B (#8), with the unused trigger input and the Reset input held at the voltage levels shown in the Function Table. Either trigger signal will cause the output of the trigger-control circuit to go high (#9).

The trigger-control circuit going high simultaneously in-





tiates three events. First, the output latch goes low, thus taking the Q output of the 14548B to a high state (#10). Second, transistor M3 is turned on, which allows the external timing capacitor, Cx, to rapidly discharge toward ground (#11). (Note that the voltage across Cx appears at the input of the upper reference circuit comparator). Third, transistor M4 is turned off and transmission gate T1 is turned on, thus allowing the voltage across Cx to also appear at the input of the lower reference circuit comparator).

When C_X discharges to the reference voltage of the lower reference circuit (#12), the outputs of both reference circuits will be high (#13). The trigger-control reset circuit goes high, resetting the trigger-control circuit flip-flop to a low state (#14). This turns transistor M3 off again, allowing C_X to begin to charge back up toward V_{DD}, with a time constant $t = R_X C_X$ (#15). In addition, transistor M4 is turned on and transmission gate T1 is turned off. Thus a high voltage level is applied to the input of the lower reference circuit comparator, causing its output to go low (#16). The monostable multivibrator may be retriggered at any time after the trigger-control circuit goes low.

When C_X charges up to the reference voltage of the upper reference circuit (#17), the output of the upper reference circuit goes low (#18). This causes the output latch to toggle, taking the Q output of the 14548B to a low state (#19), and completing the time-out cycle.

RESET OPERATION

A low voltage applied to the Reset pin always forces the Q output of the 14548B to a low state.

The timing diagram illustrates the case in which reset occurs (#20) while C_X is charging up toward the reference voltage of the upper reference circuit (#21). When a reset occurs, the output of the reset latch goes low (#22), turning on transistor M1. Thus C_X is allowed to quickly charge up to V_{DD} (#23) to await the next trigger signal.

capacitor, Cx, is charged to VDD. When a trigger

RETRIGGER OPERATION Was A MOUNTED ASSOCIATION

When used in the retriggerable mode (Figure 4), the 14548B may be retriggered during timing out of the output pulse at any time after the trigger-control circuit flip-flop has been reset (#24). Because the trigger-control circuit flip-flop resets shortly after Cx has discharged to the reference voltage of the lower reference circuit (#25), the minimum retrigger time, t_{T} (Figure 1) is a function of internal propagation delays and the discharge time of Cx.

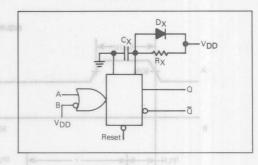
Figure 5 shows the device configured in the non-retriggerable mode.

POWER-DOWN CONSIDERATIONS

Large values of C_X may cause problems when powering down the 14548B because of the amount of energy stored in the capacitor. When a system containing this device is powered down, the capacitor may discharge from V_{DD} through the input protection diodes at pin 2 or pin 14. Current through the protection diodes must be limited to 10 mA, therefore, the turn-off time of the V_{DD} power supply must not be faster than $t=V_{DD}, C_X/(10 \text{ mA})$. For example, if V_{DD} = 5 V and C_X = 15 μ F, the V_{DD} supply must turn off no faster than $t=(5 \text{ V}) \text{e}(15 \mu\text{F})/10 \text{ mA} = 7.5 \text{ ns}$. This is usually not a problem because power supplies are heavily filtered and cannot discharge at this rate.

When a more rapid decrease of V_{DD} to zero volts occurs, the 14548B may sustain damage. To avoid this possibility, use an external clamping diode, D_X , connected as shown in Figure 3.

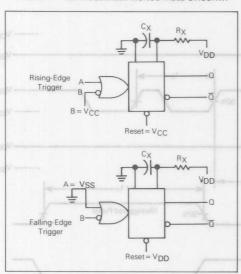
FIGURE 3 — LATCH-UP PROTECTION DURING POWER DOWN

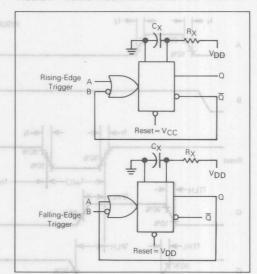


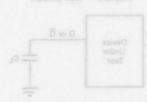
TYPICAL APPLICATIONS

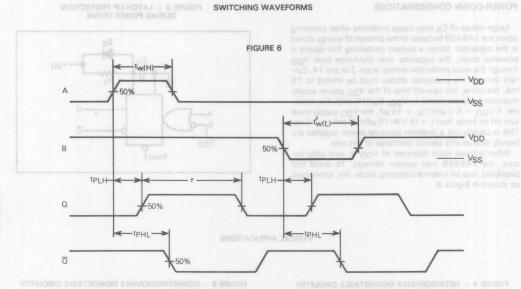
FIGURE 4 - RETRIGGERABLE MONOSTABLE CIRCUITRY

FIGURE 5 - NONRETRIGGERABLE MONOSTABLE CIRCUITRY









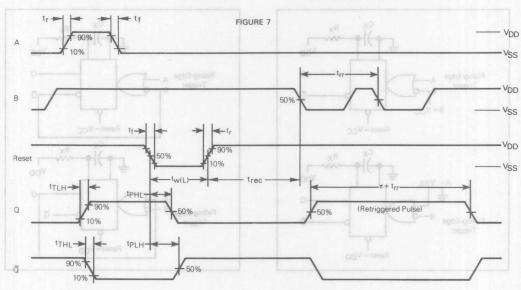
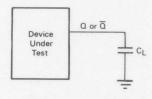


FIGURE 8 - TEST CIRCUIT





QUAD 2-INPUT ANALOG MULTIPLEXER/DEMULTIPLEXER

The MC14551B is a digitally controlled analog switch. It is an effective 4 PDT switch with low ON impedance and very low OFF leakage current. Control of analog signals up to the complete supply voltage range can be achieved.

- High On/Off Output Ratio 65 dB typical
- Quiescent Current = 5.0 nA/Package typical at 5 Vdc
- Low Crosstalk Between Switches 80 dB typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Analog Voltage Range (V_{DD}-V_{EE}) = 3 to 18 V
 Note: V_{FE} must be ≤ V_{SS}
- Transmits Frequencies Up To 65 MHz
- Linearized Transfer Characteristics, $\Delta R_{\mbox{ON}} < 60~\Omega$ for $V_{\mbox{in}}$ at $V_{\mbox{DD}}$ to $V_{\mbox{EE}}$ at 15 Vdc
- Low Noise 12 n/V√Cycle, f ≥ 1 kHz typical

MAXIMUM RATINGS (Voltages referenced to VSS)

Rating	Symbol	Value	Unit
DC Supply Voltage VDD - VEE	VDD	-0 5 to +18	Vdc
Input Voltage, All Inputs	A Bavin =	-0.5 to V _{DD} + 0.5	Vdc
Through Current	010 1	25	mAdd
Operating Temperature Range AL Device CL/CP Device	TA_	-55 to +125 -40 to +85	°C
Storage Temperature Range	T _{stg}	-65 to +150	°C

CMOS MSI

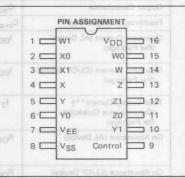
(LOW-POWER COMPLEMENTARY MOS)

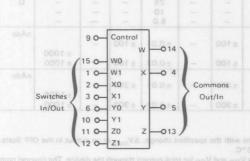
QUAD 2-INPUT ANALOG MULTIPLEXER/ DEMULTIPLEXER



CASE 620
L SUFFIX
CERAMIC PACKAGE

CASE 648
P SUFFIX
PLASTIC PACKAGE





Control	ON
0	W0 X0 Y0 Z0
1	W1 X1 Y1 Z1

V_{DD} = Pin 16 0 90 40 00 V_{SS} = Pin 8 14 10 000 000 000 000 V_{EE} = Pin 7 10 000 000 000 V_{EE} = Pin 7

Note: Control Input referenced to V_{SS} , Analog Inputs and Outputs reference to V_{EE} . V_{EE} must be $\leq V_{SS}$.

ELECTRICAL CHARACTERISTICS (VEE = VSS)

			V _{DD}		w*		25°C			Thigh*	
	Characteristic	Symbol	Vdc	Min	Max	Min	Тур	Max	Min	Max	Unit
(Output Voltage "0" Level	VOL	5.0	_	0.05	_	0	0.05	_	0.05	Vdc
	V _{in} = V _{DD} or O	OL	10	_	0.05	_	0	0.05	_	0.05	
	III DD		15	_	0.05	-	0	0.05	_	0.05	
	"1" Level	VOH	5.0	4.95	_	4.95	5.0	_	4.95	_	Vdc
	V _{in} = 0 or V _{DD}		10	9.95	-	9.95	10	-	9.95	-	
	OW POWER COMPEGNENTARYING	20	15	14.95	-	14.95	15	-	14.95	- 1	
1	nput Voltage (Control) "O" Level	VIL									Vdc
• '	$(V_O = 4.5 \text{ or } 0.5 \text{ Vdc})$	*IL	5.0	_	1.5	_	2.25	1.5	0_	1.5	Vuc
	(V _O = 9.0 or 1.0 Vdc)		10	_83	3.0	MULT	4.50	3.0	MULT	3.0	1
	(V _O = 13.5 or 1.5 Vdc)		15	_	4.0	-	6.75	4.0	-	4.0	
	"1" Level	1/	- 0	0 0 0 0	g swite	plans-bi	Hert near	tigitelly	1 5 ti 6	MOTHOR	1/1-
		VIH	5.0	3.5	nd very	3.5	2.75	wel din	3.5	TOP P a	Vdc
	$(V_0 = 0.5 \text{ or } 4.5 \text{ Vdc})$	and the same of	10	7.0	gmas s	7.0	2.75 5.50	olamo to	7.0	current, (Jeakage
	$(V_O = 1.0 \text{ or } 9.0 \text{ Vdc})$ $(V_O = 1.5 \text{ or } 13.5 \text{ Vdc})$		15	11.0		11.0	8.25	bak	11.0	180 <u>3</u> 9051	voltage
			13	11.0		11.0			11.0		
lı	nput Current (Control)	line .	4.5			Ispical	86±8	Ratio -	prichar	HO/nO d	pill @
	(AL Device)	lin	15	7dd	±0.1	niavi e	0.00001	±0.1	= tossa	±1.0	μAdc
I	nput Current (Control)				Indiana	86 08	±	w2 non	putaR s	totanes) v	01.8
	(CL/CP Device)	lin	15	-	±0.3		0.00001	±0.3	k Betw	±1.0	μAdc
l	nput Capacitance	C _{in}					611	especial men	ING RIDS	00/01/1 00	pF
	(V _{in} = 0)	111			1	PA 31	O Vac to	8 = 9	pa Rang	stleV ylqu	113 D
	Control, Inhibit	825	-	-	-4/ E	3-0.1	5.0	7.5	ne fran	aslod Volta	hA e
	Switch Inputs (Inhibit = 1)		-	-	-	-	10	21.0	शर्त tax	m aāV se	old .
(Output Capacitance	C _{out}	10	_	_	- 21	M 17 0	.qU.se	onsup	nsmiles Fre	pf
F	eedthrough Capacitance	C _{in-out}	10	_101	Ω Q3	иея/	0.10	haract) ro <u>t</u> en	nT basinss	pF
-	Quiescent Current (AL Device)		5.0		5.0		0.005	5.0	JV of	150	μAdc
	(Per Package)	IDD	10	_	10	NT Dist	0.005	10	12-00	300	μAdc
	31 Carrier of the control of the con		15		20	_	0.015	20	_	600	
-	Quiescent Current (CL/CP Device)	l	5.0	-	20		0.005	20		150	иAdc
	(Per Package)	IDD	10		40		0.005	40		300	μΑαс
	(Fel Fackage)		15		80		0.015	80	registio V	600	MUM
7	otal Supply Current**†	1	5.0		pule V	1 10				000	
1	(D	I _T	10	81-			0.07 μA/kh				μAdc
	Per Package)		15	-).20 μA/kH).36 μA/kH				boario)
	OF COUNTY AND TO S		48.60	1	100	1 10	7.00 µA/KI	12/11/1	Q	E-1240 07	1200011019
C	In Resistance (AL Device)	RON	5.0		800	-	250	1050	-	1300	Ω
			10	-027	400	- A	120	500	JA_ 98	550	ma T gan
	the state of the s		15	_ 28	220	-	80	280	40 <u>1</u> 10	320	
C	On Resistance (CL/CP Device)	RON	5.0	- 081	880	-6)s	250	1050	-	1200	Ω
			10	-	450	-	120	500	-	520	
			15	-	250	_	80	280	-	300	
Δ	ON resistance Between Any	Δ R _{ON}	5.0	-	-	-	25	-	-		Ω
	Two Channels		10	-	-	-	10	-	-	-	
			15	-	_	-	5.0	-	_	-	
C	FF Channel Leakage Current	-						tenned	-0.8		nAdc
	(AL Device)		15	-	±100	- /	±0.01	±100	-		
	Any Channel					1				±1000	
	II Channels OFF:	Jewne0	15	-	±100	-	±0.02	± 100	-0.61	±1000	
C	OFF Channel Leakage Current	÷	J			1	" Grand X	144	-01		nAdc
	(CL/CP Device)		15	-	±300	mo2	±0.01	±300	2.9	8	
	Any Channel				/tin	no)		1.8	3.0-	±1000	1
Δ	II Channels OFF:		15	i -	±300	- 8	±0.02	±300	1.50	±1000	

^{*} T_{low} = -55°C for AL Device, -40°C for CL/CP Device.

Thigh = +125°C for AL Device, +85°C for CL/CP Device.

Noise immunity is defined as the control input voltage coincident with the specified change, ΔV_{out}, at an output in the OFF State.

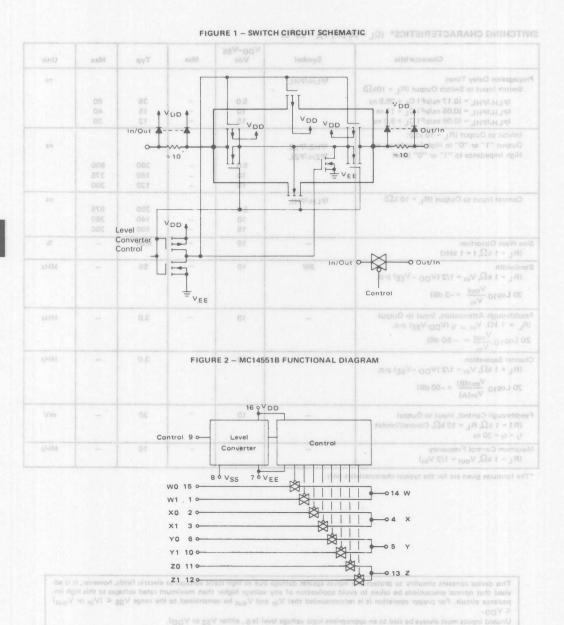
* The formulae given are for the typical characteristics only at 25°C.

[†] Total Supply Current, I_T, is the current drawn at device terminals V_{DD} and V_{SS} for total current through the device. The channel component (Vin-Vout)/RON, should not be included.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in} \text{ or } V_{out})$ $\le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD).

^{*}The formulas given are for the typical characteristics only.



THUORIS TEST LANDTEST CIRCUITS MARS - 6 SHUDIS



FIGURE 4 – PROPAGATION DELAY TIMES, CONTROL AND INHIBIT TO OUTPUT

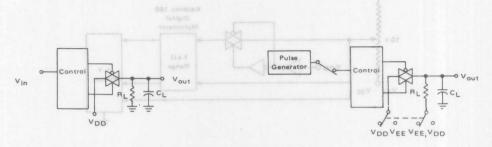


FIGURE 5 – BANDWIDTH AND FEEDTHROUGH ATTENUATION

FIGURE 11 - VOD @ 5.0V, VEE @ -5.0 V

Control input used to turn ON or OFF the switch under test.

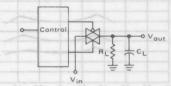
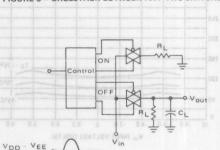
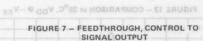


FIGURE 6 - CROSSTALK BETWEEN ANY TWO SWITCHES

FIGURE 10 - VOD @ 7.5 V. VEE @ -7.5V





SIGNAL OUTPUT

FIGURE 8 - MAXIMUM CONTROL FREQUENCY

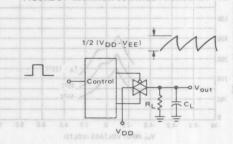
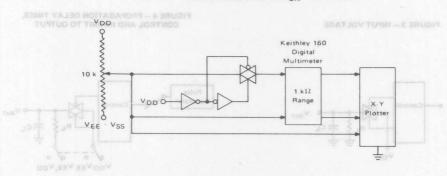
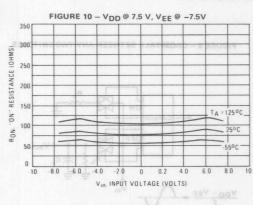
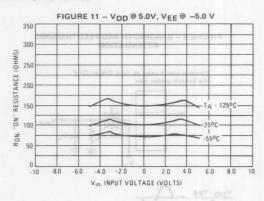


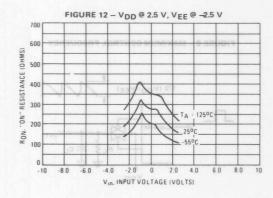
FIGURE 9 - CHANNEL RESISTANCE (RON) TEST CIRCUIT

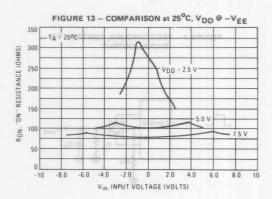


TYPICAL RESISTANCE CHARACTERISTICS











MC14553B

THREE-DIGIT BCD COUNTER

The MC14553B three-digit BCD counter consists of three negative edge triggered BCD counters that are cascaded synchronously. A quad latch at the output of each counter permits storage of any given count. The information is then time division multiplexed, providing one BCD number or digit at a time. Digit select outputs provide display control. All outputs are TTL compatible.

An on-chip oscillator provides the low-frequency scanning clock which drives the multiplexer output selector.

This device is used in instrumentation counters, clock displays, digital panel meters, and as a building block for general logic applications.

- TTL Outputs
- On-Chip Oscillator
- Cascadable
- Clock Disable Input
- Pulse Shaping Permits Very Slow Rise Times on Input Clock
- Output Latches
- Master Reset

MAXIMUM RATINGS (Voltages referenced to VSS)

Rating	Symbol	Value	Unit
DC Supply Voltage	VDD	-0.5 to +18	Vdc
Input Voltage, All Inputs	Vin	-0.5 to V _{DD} + 0.5	Vdc
DC Current Drain per Pin	0.0.0.0	10	mAdo
DC Current per Pin, All Outputs	01 4.0	20	mAdc
Operating Temperature Range — AL Device CL/CP Device	TA	-55 to +125 -40 to +85	°C
Storage Temperature Range	T _{stg}	-65 to +150	°C

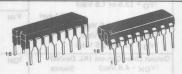
325	T	RUTH TABL	E	50
	INPU	TS 000.0		100
MASTER RESET	CLOCK	DISABLE	LE	OUTPUTS
0		+ (=101\An	8.0	No Change
0	700	TEONAL	0	Advance
0	×	1	×	No Change
0	1		0	Advance
0	1	_	0	No Change
0	0	×	X	No Change
0	×	×	_	Latched
0	×	×	1	Latched
1	×	×	0	Q0 = Q1 = Q2 = Q3 = 0

X = Don't Care

CMOS LSI

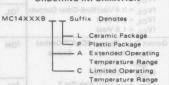
(LOW-POWER COMPLEMENTARY MOS)

THREE-DIGIT BCD COUNTER

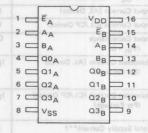


CERAMIC PACKAGE PLASTIC PACKAGE CASE 620 CASE 648

ORDERING INFORMATION



PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that Vin and Vout be constrained to the range VSS ≤ (Vin or Vout) ≤ VDD.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD).

ELECTRICAL CHARACTERISTICS

		VDD	Tie	ow*		25°C		Thi	gh*	111111
Characteristic	Symbol	Vdc	Min	Max	Min	Тур	Max	Min	Max	Unit
Output Voltage "0" Level	VOL	5.0	-	0.05	-	0	0.05	-	0.05	Vdc
Vin = Vnn or 0	OL	10	-	0.05	-	0	0.05	-	0.05	
CMOS ESP		15	_	0.05	223731	0	0.05	2250117	0.05	
"1" Level	VOH	5.0	4.95	_	4.95	5.0	-	4.95	_	Vdc
Vin = 0 or VDD	OTON	10	9.95	some to	9.95	10	OB-rioil	9.95	NCHISE	
- III	•	15	14.95	panadami	14.95	15	on aigh	14.95	loo Tooni	edos te
nput Voltage# "0" Level	VIL		yns to	2021032	imieg '	strues de	t of ear	the outpu	76 riot	Vdc
(V _O = 4.5 or 0.5 Vdc)	- IL	5.0	bessle	1.5	sivile on	2.25	1.5	nolmi ed	1.5	navio
(V _O = 9.0 or 1.0 Vdc)	-	10	STUTTURE	3.0	(Cl. Tami	4.50	3.0	murr GO	3.0	ibivoro
(V _O = 13.5 or 1.5 Vdc)		15	- august	4.0	trieston	6.75	4.0	lestenes	4.0	and the same
"1" Level	VIH		sloots o	- 3813.12	inguisari	1.1 1918 200	abivoso	notelfican	V Ditt28 (L/	Vdc
(VO = 0.5 or 4.5 Vdc)	*IH	5.0	3.5	ry scannin	3.5	2.75	north and	3.5	gido-no	
(V _O = 1.0 or 9.0 Vdc)		10	7.0		7.0	5.50	ter outp	7.0	rives the	
(VO = 1.5 or 13.5 Vdc)	194	15	11.0	i, clock c	11.0	8.25	nuntani	11.0	device	This
			pipel li	397190 30	black	priistrud	6 26 D	etars, an	n Janso	Istipib
Output Drive Current (AL Device) (VOH = 4.6 Vdc) Source	ЮН	5.0	-0.64	100	-0.51	0.00		0.20	lons.	mAdc
		5.0	-0.64		-0.51 -1.3	-0.88 -2.25	_	-0.36 -0.9	Buotu O	JTT .
(V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc)	CERAL	15	-4.2		-3.4	-8.8		-2.4		
	-					0.88		13/2/2015	baO aidi	0-mO 0
(VOL = 0.4 Vdc) Sink-Pin 3	IOL	5.0	0.5	-	0.4	2.25	_	0.28	edable	mAdc
(V _{OL} = 0.5 Vdc)	4	10 15	1.1		0.9	8.8	_	0.65	_	e Cloc
(V _{OL}) ≈ 1.5 Vdc) 4/4 DM/H3GRO		-				-		1.20	-	
(VOL = 0.4 Vdc) Sink-Other Outputs	IOL	5.0	3.0	Input Clos	2.5	4.0	Na Ara A	211.1.6.9	nigade (mAdc
(V _{OL} = 0.5 Vdc)	MCTES	10	6.0	-	5.0	8.0	-	3.5	ota Late	e Out
(V _{OL} = 1.5 Vdc)		15	18	_	15	20	_	10	- 23	
Output Drive Current (CL/CP Device)	ІОН								STORES IN	mAdc
(VOH = 4.6 Vdc) Source		5.0	-0.52	-	-0.44	-0.88	-	-0.36	-	
(VOH = 9.5 Vdc)		10	-1.3	-	-1.1	-2.25	-	-0.9	-	-
(V _{OH} = 13.5 Vdc)		15	-3.6	-	-3.0	-8.8	-	-2.4	STATE A	BELLAAL
(VOL = 0.4 Vdc) Sink-Pin 3	IOL	5.0	0.23	-	0.2	0.88	10131012	0.16	2011 2 201	mAdc
(V _{OL} = 0.5 Vdc)		10	0.60	eulaV	0.5	2.25	-	0.40	-	
(V _{OL} = 1.5 Vdc)		15	1.80	+ 01-5-0-	1.5	8.8	-	1.20	-eps1	oV ylags
(VOL = 0.4 Vdc) Sink-Other Outputs	IOL	5.0	2.4	90 V 01 8	2.0	4.0	-	1.6	ugr4 IIA	mAdc
(V _{OL} = 0.5 Vdc)		10	3.8	0 H	3.0	8.0	-	2.5	9 rep nis	greent Di
(VOL = 1.5 Vdc)		15	10	20	8.4	20	-	7.0	Pin All	or tropy
nput Current (AL Device)	lin	15	-	±0.1	-	±0.00001	±0.1	_	±1.0	μAdc
nput Current (CL/CP Device)	lin	15	-	±0.3	- A	±0.00001	±0.3	Tu /C	±1.0	μAdc
nput Capacitance	Cin	-00	- 0	11+ 07-88-	- 812	5.0	7.5	- 990	A STUDE	pF
(Vin = 0) 8 ^A A8 = 8	-in	L		11 107 EB-	Bis	0.0	7.0	350	NET STUTE!	derak, a
Quiescent Current (AL Device)	IDD	5.0	_	5.0	_	0.010	5.0	_	150	μAdc
(Per Package)	.00	10	_	10		0.020	10		300	pr.130
11 = a10 ASD = a		15	_	20	_	0.030	20	_	600	
	1									
Quiescent Current (CL/CP Device)	DD	5.0		50	-	0.010	50		375	μAdc
(Per Package)		10		100		0.020	100	-	750	a last
		15	-	200		0.030	200	7.83	1500	
otal Supply Current**†	IT	5.0	1		11-10	.35 µA/kHz		,	RES	μAdc
(Dynamic plus Quiescent,	or like to 1	10	1			.85 µA/kH2				155
Per Package)		15		eonaybA	IT = (1	.50 μA/kHz) f + DE)		
(C _L = 50 pF on all outputs, all					N N	1			0	
buffers switching)	Tini	100		manus la di		-				

^{*}T_{low} = -55°C for AL Device, -40°C for CL/CP Device. Thigh = +125°C for AL Device, +85°C for CL/CP Device. =Noise immunity specified for worst-case input combination.

[#]Noise immunity specified for worst-case input combination.

Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc

2.0 Vdc min @ V_{DD} = 10 Vdc

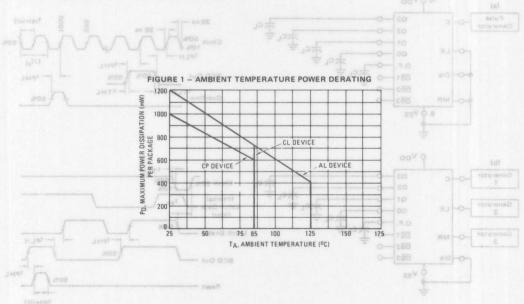
2.5 Vdc min @ V_{DD} = 15 Vdc

[†]To calculate total supply current at loads other than 50 pF: $|T(C_L)| = |T(50 \text{ pF}) + 4 \times 10^{-3} \text{ (}C_L - 50) \text{ VDD}^{\dagger}$ where: |T| is in μ A (per package), |C| in |F|, |V| in Vdc, and f in kHz is input frequency. *The formulas given are for the typical characteristics only at 25°C.

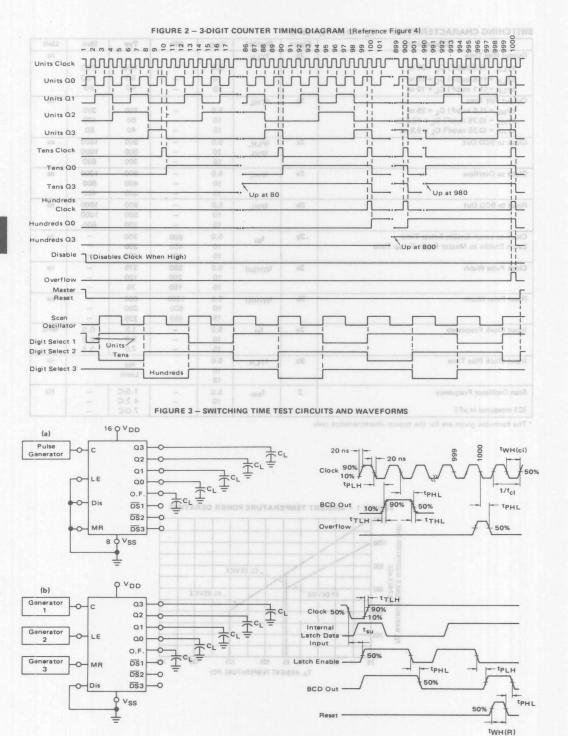
CWITCHING	CHARACTERISTICS	# 10.	- 50 SE T 250CI	
2MII CHING	CHARACIERISTICS	101	= 50 pr, 1A = 25°C)	

8 8 8 8 8 Characteristic	Figure	Symbol	VDD	Min	Тур	Max	Unit
Output Rise Time ttl = (3.0 ns/pF) Ct + 30 ns	3a	tTLH	5.0	mm	100	200	ns Capi Cippi
t _{TLH} = (1.5 ns/pF) C _L + 15 ns t _{TLH} = (1.1 ns/pF) C _L + 10 ns	HUL		10	اللحالة	50 40	100	Units 120
And the second s	2-	-	10	NOTE:		others.	0.0716621
Output Fall Time tth= (1.5 ns/pF) CL + 25 ns	3a	THL	5.0	- 11	100	200	ns
t _{THL} = (0.75 ns/pF) C _L + 12.5 ns t _{THL} = (0.55 ns/pF) C _L + 9.5 ns		E	10 15		50 40	100	Daire
Clock to BCD Out	3a	tPLH,	5.0	- 11	900 500	1800	ns Tens Clock
		tPHL	15		300	600	
Clock to Overflow	3a	tPHL	5.0		600 400	1200 800	ns
080 is qu - 1		08 to gu **	15	-	200	400	LI STORY
Reset to BCD Out	3b	tPHL	5.0	-	900	1800	ns
			10 15	_	500 300	100ò 600	of aberba
Clock to Latch Enable Setup Time	.3b	t _{su}	5.0	600	300		ns
atch Enable to Master Reset Setup Time			10 15	400	200	AND TO	Disabil
Clock Pulse Width	3a	tWH(cl)	5.0	550	275	-	ns
J	-		10	200	100 75		O vertibar
Reset Pulse Width	21	-	-	150	-	-	edseld.
reset Pulse Wigth	3b	tWH(R)	5.0	1200 600	300	_	ns
			15	450	225	-	Scan
nput Clock Frequency	3a	fcl	5.0	-	1.5	0.9	MHz
			10	1 -	7.0	2.5	Select
nput Clock Rise Time	3b	tTLH	5.0		No		ns
			10	lundreds	Limit		toning II
Scan Oscillator Frequency	2	fosc	5.0	-	1.5/C 4.2/C	-	Hz
(C1 measured in µF)	BOOKS TO	NE THEFT	15/3	FIGURE 3	7.0/C		

^{*} The formulae given are for the typical characteristics only.





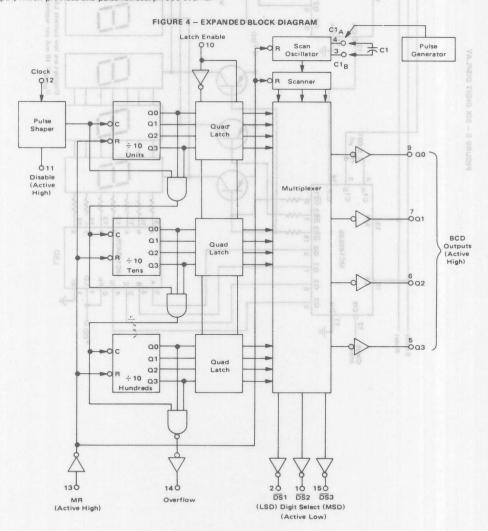


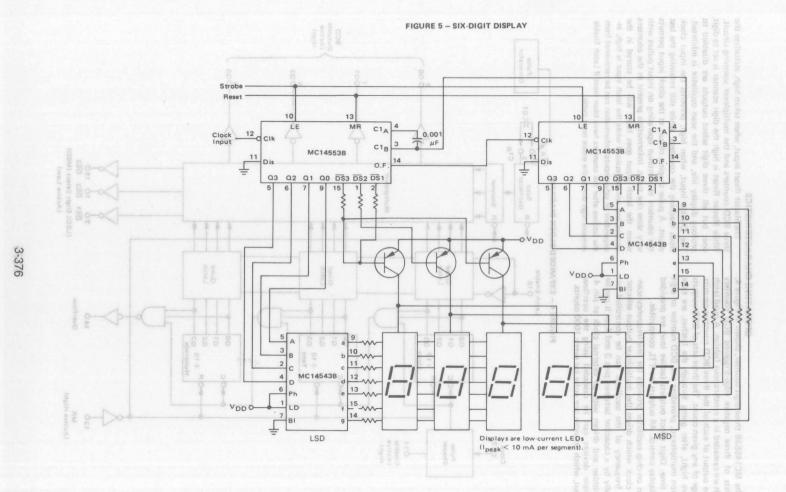
OPERATING CHARACTERISTICS

The MC14553B three-digit counter, shown in Figure 4, consists of three negative edge-triggered BCD counters which are cascaded in a synchronous fashion. A quad latch at the output of each of the three BCD counters permits storage of any given count. The three sets of BCD outputs (active high), after going through the latches, are time division multiplexed, providing one BCD number or digit at a time. Digit select outputs (active low) are provided for display control. All outputs are TTL compatible.

An on-chip oscillator provides the low frequency scanning clock which drives the multiplexer output selector. The frequency of the oscillator can be controlled externally by a capacitor between pins 3 and 4, or it can be overridden and driven with an external clock at pin 4. Multiple devices can be cascaded using the overflow output, which provides one pulse for every 1000 counts.

The Master Reset input, when taken high, initializes the three BCD counters and the multiplexer scanning circuit. While Master Reset is high the digit scanner is set to digit one; but all three digit select outputs are disabled to prolong display life, and the scan oscillator is inhibited. The Disable input, when high, prevents the input clock from reaching the counters, while still retaining the last count. A pulse shaping circuit at the clock input permits the counters to continue operating on input pulses with very slow rise times. Information present in the counters when the latch input goes high, will be stored in the latches and will be retained while the latch input is high, independent of other inputs. Information can be recovered from the latches after the counters have been reset if Latch Enable remains high during the entire reset cycle.







2-BIT BY 2-BIT PARALLEL BINARY MULTIPLIER

The MC14554B 2 x 2-bit parallel binary multiplier is constructed with complementary MOS (CMOS) enhancement mode devices. The multiplier can perform the multiplication of two binary numbers and simultaneously add two other binary numbers to the product. The MC14554B has two multiplicand inputs (X0 and X1), two multiplier inputs (Y0 and Y1), five cascading or adding inputs (K0, K1, M0, M1, and M2), and five sum and carry outputs (S0, S1, S2, C1 [S3], and C0). The basic multiplier can be expanded into a straightforward m-bit by n-bit parallel multiplier without additional logic elements

Application areas include arithmetic processing (multiplying/ adding, obtaining square roots, polynomial evaluation, obtaining reciprocals, and dividing), Fast Fourier Transform processing, digital filtering, communications (convoluation and correlation), and process and machine controls.

- Diode Protection on All Inputs
- All Outputs Buffered
- Quiescent Current = 5.0 nA typical @ 5 Vdc
- Straight-forward m-Bit By n-Bit Expansion
- No Additional Logic Elements Needed for Expansion
- Multiplies and Adds Simultaneously
- Positive Logic Design
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- · Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range

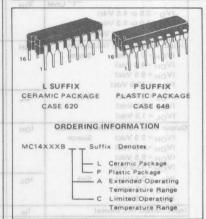
MAXIMUM RATINGS (Voltages referenced to Vss)

008 Rating 04 01	Symbol	Value	Unit
DC Supply Voltage	V _{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs GGI + LGHS	Vin	-0.5 to V _{DD} + 0.5	Vdc
DC Current Drain per Pin	W 100 1 1	10	mAdc
Operating Temperature Range AL Device CL/CP Device	TA	-55 to +125 -40 to +85	°C
Storage Temperature Range	T _{stg}	-65 to +150	°C

CMOS MSI

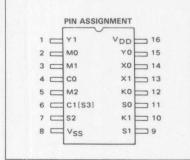
(LOW-POWER COMPLEMENTARY MOS)

2-BIT BY 2-BIT PARALLEL BINARY MULTIPLIER



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that Vin and V_{out} be constrained to the range V_{SS} ≤ (V_{in} or V_{out}) ≤ V_{DD}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD).



Noise Margin for both "I" and "O" level "O" level "O" bits "I" mid not margin second

S = (X x Y) + K + M 9 mm oby 3 S

Where:

Then:

- x Means Arithmetic Times.
- + Means Arithmetic Plus.
- S = S3 S2 S1 S0, X = X1X0, Y = Y1Y0,

K = K1 K0, M = M1 M0 (Binary Numbers).

Example: Given:

X = 2(10), Y = 3(11)K = 1(01), M = 2(10)

 $S = (2 \times 3) + 1 + 2 = 9$

 $S = (10 \times 11) + 01 + 10 = 1001$

Note: CO connected to M2 for this size multiplier.

See general expansion diagram for other size multipliers.

MOTOROLA

ELECTRICAL CHARACTERISTICS

		VDD	Tlo	w*		25°C		Thi	gh *	
Characteristic	Symbol	Vdc	Min	Max	Min	Тур	Max	Min	Max	Unit
Output Voltage "0" Level	VOL	5.0	-	0.05	-	0	0.05	-	0.05	Vdc
V _{in} V _{DD} or 0		10	-	0.05	-	0	0.05	-	0.05	
1986 90650		15	-	0.05	-	0	0.05	- 1	0.05	
1284 20 Level	VOH	5.0	4.95	NT HUN	4.95	5.0	LARAS	4.95	YE TIE-	Vdc
Vin · 0 or VDD	030	10	9.95	-	9.95	10	-	9.95	-	
The state of the s		15	14.95	and Table	14.95	15	- ATT 0	14.95	NACTE OF	2
nput Voltage# "0" Level	VIL		-			- Jan 1935	101 001			Vdc
(VO = 4.5 or 0.5 Vdc)	2	5.0	pyrces. Th	1.5	memean	2.25	1.5	sentary -	1.5	12199
(VO = 9.0 or 1.0 Vdc)		10	edmun.	3.0	d to no	4.50	3.0	nomed i	3.0	lum
(V _O = 13.5 or 1.5 Vdc)		15	pripara 4	4.0	dmon y	6.75	4.0	ie Alisnos	4.0	bne
"1" Level	VIH		SHAFT CLASS	T.X. 19115	DEC) ELLER	m brisalto	BRUFF OF	17 KENT CH	ECATON	2217.1
(VO = 0.5 or 4.5 Vdc)		5.0	3.5	rudei su	3.5	2.75	MI_ILY	3.5	alugni 1	Vdc
(VO = 1.0 or 9.0 Vdc)		10	7.0	(12) 811	7.0	5.50	ice soil b	7.0	M1,_und	DIM
(VO = 1.5 or 13.5 Vdc)	Direction	15	11.0	ornLbsb	11.0	8.25	sic could	11.0	00 bns .	[83]
Output Drive Current (AL Device)	ТОН	0	not Isno	Willes Jo	HINW W	Harrium I	HILESON T	d-n vd	ru-m bis	mAde
(V _{OH} = 2.5 Vdc) Source	20 1	5.0	-3.0		-2.4	-4.2		-1.7	-arms	nais
(VOH = 4.6 Vdc)	a Day	5.0	-0.64	m) -oros	-0.51	-0.88	abeloni	-0.36	oitesilaa	13
(VOH = 9.5 Vdc)		10	-1.6	one Hardi	-1.3	-2.25	OO'T SIG	-0.9		Bibe
(VOH = 13.5 Vdc)		15	-4.2	(1000mm)	-3.4	-8.8	003 S16	-2.4	eldo pr	4 50 L254
The state of the s	A. (2) (2) (3)		100000	121907070	THE PERSON S	100231013		-	21803133	mAd
	APIOL	5.0	0.64	s,(moite	0.51	0.88	1002) 5155	0.36	moz, gni	DOTAY.
(VOL = 0.5 Vdc)		10 15	1.6	-	1.3	2.25	-	0.9	nachīne.	bris .
(V _{OL} = 1.5 Vdc)		15	4.2	-	3.4	8.8	_	2.4		
Output Drive Current (CL/CP Device)	ІОН					210	ant IIA	a naitas		mAde
(V _{OH} = 2.5 Vdc) Source		5.0	-2.5	-	-2.1	-4.2	- b	-1.7	untuO II	A 8
1.0H 1.0 1007	MC14	5.0	-0.52		-0.44	-0.88	-	-0.36		
(V _{OH} = 9.5 Vdc)		10	-1.3		-1.1	-2.25	5.0-nA	-0.9	Tubesetm	20
(V _{OH} = 13.5 Vdc)		15	-3.6	-	-3.0	-8.8	a value	-2.4	PRINTER	8 0
(VOL = 0.4 Vdc) Sink	IOL	5.0	0.52	nālene	0.44	0.88	entid3 o	0.36	o Additio	mAde
(V _{OL} = 0.5 Vdc)		10	1.3	~	1.1	2.25	Simulta	0.9	nailoista.	10
(V _{OL} = 1.5 Vdc)		15	3.6	-	3.0	8.8	OT SPILING	2.4	altiplies	
nput Current (AL Device)	lin	15		± 0.1		±0 00001	± 0.1	Isañ DiB	± 1.0	μAdd
nput Current (CL/CP Device)	lin	15	-	± 0.3	DDV.	±0.00001	±0.3	Tage_Hai	±1.0	μAdo
nput Capacitance	Cin	- 1	WOR WO.	974) 2	so_LIT	5.0	7.5	Driving	o stdeck	OF
(V _{in} = 0)	-III		some Th		navO sta	el ITH	WT no I	and JT		2
Quiescent Current (AL Device)	uli tee	5.0		5.0		0.005	5.0	- 4	150	μAdo
(Per Package)	IDD	10		10		0.003	10		300	MAGG
ad mornegary famion redr beliebs a	n I	15		20		0.015	20	_	600	
101 102 0	in .				-	0.005	-	HoVI 2D	100 000	
Quiescent Current (CL/CP Device)	DD D	5.0		20	- (8	0.005	20		150	μAde
and the same of th	Sint 1	10	- 3	40	Totaling	0.010	40	(H10207	300	
ration it is recommended that Vin and	37 .	15	- Ris	80	1 204		80		600	Wign-
Total Supply Current**†	ev IT	5.0	180 to			.0 μA/kHz)				μAde
(Dynamic plus Quiescent,		10				.0 μA/kHz)				them
Per Package) will from study best		15	0.00		IT = (3	.0 μA/kHz)	f + IDD			of posts
(CL 50 pF on all outputs, all	le M									- Smith
buffers switching)	9.		401	07 01	and in some		Ziveu 10			

¹T_{low} -55°C for AL Device, -40°C for CL/CP Device. Thigh = +125°C for AL Device, +85°C for CL/CP Device.

#Noise immunity specified for worst-case input combination.

*Noise immunity specified for worst-case input combination.

Noise Margin for both "1" and "0" level = 1.0 Vdc min @ VDD = 5.0 Vdc

2.0 Vdc min @ VDD = 10 Vdc

2.5 Vdc min @ VDD = 15 Vdc

†To calculate total supply current at loads other than 50 pF:

| T(CL) = | T(50 pF) + 3.5 x 10⁻³ (CL -50) VDDf

where: | T is in µA (per package), CL in pF, VDD in Vdc, and f in kHz is input frequency.

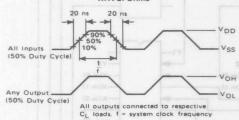
**The formulas given are for the typical characteristics only at 25°C.

SWITCHING	CHARACTERISTICS*	$(C_1 = 50 \text{ pF } T_A = 25^{\circ}C)$

Characteristic	Symbol	VDD	Min	Тур	Max	Unit
Output Rise Time	tTLH					ns
t _{TLH} = (3.0 ns/pF) C _L + 30 ns		5.0	-	100	200	1000
tTLH = (1.5 ns/pF) CL + 15 ns	Bingey Much	10	es sistem	50	100	
t _{TLH} = (1.1 ns/pF) C _L + 10 ns		15	-	40	80	
Output Fall Time	tTHL	V and V				ns
t _{THL} = (1.5 ns/pF) C _L + 25 ns		5.0	-	100	200	1
t _{THL} = (0.75 ns/pF) C _L + 12.5 ns	-	10	-	50	100	
t _{THL} = (0.55 ns/pF) C _L + 9.5 ns		15	-	40	80	
Propagation Delay Time	tPLH,		200	(Netro)		ns
K0 to C0	tPHL		and the same of th			
tpLH, tpHL = (1.7 ns/pF) CL + 185 ns	900	5.0	-	270	675	100
tpLH, tpHL = (0.66 ns/pF) CL + 82 ns	OX-	10	-	115	290	
tpLH, tpHL = (0.5 ns/pF) CL + 60 ns M0 to S2		15		85	215	
tpLH, tpHL = (1.7 ns/pF) CL + 595 ns		5.0	-	680	1700	
tpLH, tpHL = (0.66 ns/pF) CL + 247 ns		10	-	280	750	
tpLH, tpHL = (0.5 ns/pF) CL + 185 ns		15	-	210	570	

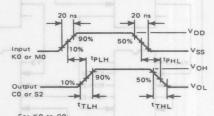
^{*} The formulae given are for the typical characteristics only.

FIGURE 1 - DYNAMIC POWER DISSIPATION WAVEFORMS



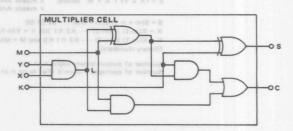
LOGIC DIAGRAM MO 9 31 M Multiplier Cell 12 -0 K0 C0 0 M2 0 M 13 -0 X 1 Multiplier X Multiplier Cell Cell 10 09 C1(S3) S2 SO

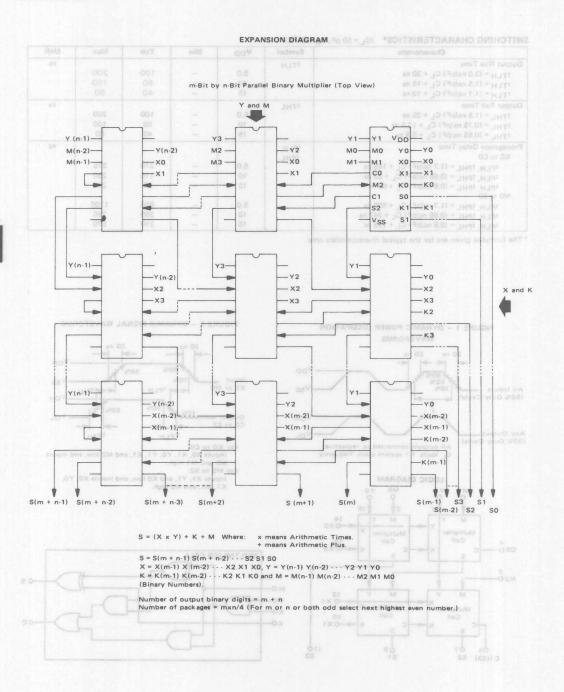
FIGURE 2 - DYNAMIC SIGNAL WAVEFORMS



For K0 to C0: Inputs X0, X1, Y0, Y1, K1, and M2 low, and inputs M0 and M1 high. For M0 to S2:

Inputs X1, Y1, and K0 low, and inputs X0, Y0, K1, M1, and M2 high.







DUAL BINARY TO 1-0F-4 DECODER/DEMULTIPLEXER

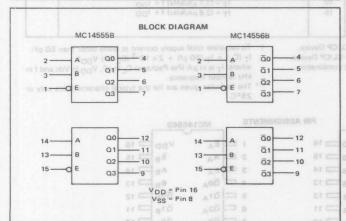
The MC14555B and MC14556B are constructed with complementary MOS (CMOS) enhancement mode devices. Each Decoder/ Demultiplexer has two select inputs (A and B), an active low Enable input (E), and four mutually exclusive outputs (Q0, Q1, Q2, Q3). The MC14555B has the selected output go to the "high" state, and the MC14556B has the selected output go to the "low" state. Expanded decoding such as binary-to-hexadecimal (1-of-16), etc., can be achieved by using other MC14555B or MC14556B devices.

Applications include code conversion, address decoding, memory selection control, and demultiplexing (using the Enable input as a data input) in digital data transmission systems.

- Diode Protection on All Inputs
- Noise Immunity = 45% of VDD Typical
- Active High or Active Low Outputs
- Low Quiescent Current 5.0 nA/package typical @ 5 Vdc
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered
- · Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range

MAXIMUM RATINGS (Voltages referenced to VSS)

Rating	Symbol	Value	Unit
DC Supply Voltage	V _{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	Vin	-0.5 to V _{DD} + 0.5	Vdc
DC Current Drain per Pin	- 1	10	mAdc
Operating Temperature Range – AL Device CL/CP Device	T _A	-55 to +125 -40 to +85	°C
Storage Temperature Range	Tstg	-65 to +150	°C



MC14555B MC14556B

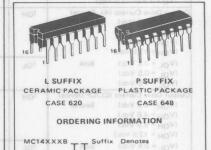
C14555BoMC14556B

CMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

DUAL BINARY TO 1-OF-4 DECODER/DEMULTIPLEXER

Active High Outputs - MC14555B Active Low Outputs - MC14556B



										1	
-		TRU	тн	TAI	BLE	_	_	_	-	_	
INI	PUTS	3	0	OUTPUTS				OUTPUTS			
ENABLE	SEI	LECT	_	_	155	15012	MC14556B				
Ē	В	Α	03	02	01	00	Q3	ā2	Ō1	ão	
0	0	0	0	0	0	1	1	1	1	0	
0	0	1	0	0	1	0	1	1	0	1	
0	1	0	0	1	0	0	1	0	1	1	

Ceramic Package

Temperature Range

Plastic Package Extended Operating Temperature Range C Limited Operating

1 1 0 0 0 0 1 1 0 0 0 0 1 1 1 1 XX

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that Vin and Vout be constrained to the range VSS ≤ (Vin or Vout) ≤ VDD.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD).

ELECTRICAL CHARACTERISTICS

		VDD	TI	ow*		25°C		Th	igh *	
Characteristic	Symbol	Vdc	Min	Max	Min	Тур	Max	Min	Max	Unit
Output Voltage "0" Level	VOL	5.0	-	0.05	-	0	0.05	_	0.05	Vdc
Vin VDD or 0		10		0.05	-	0	0.05	-	0.05	
CMOS 22 GO	1	15	-	0.05	-	0	0.05	-	0.05	
"1" Level	VOH	5.0	4.95	- 1	4.95	5.0	N1를 기7	4.95	-	Vdc
V _{in} 0 or V _{DD}		10	9.95	- 813	9.95	10	DEE/D	9.95	_	
TOOM THE PRINCE THE PRINCE AS	200	15	14.95	-	14.95	15	_	14.95	-	
Input Voltage# "0" Level	VIL		elamos r	trw bars	constru	еть 8888	d Micha	ts BB88	se MC14	Vdc
(Vo = 4.5 or 0.5 Vdc)	"-	5.0	abo-ode	1.5	livel - sb	2.25	1.5	80H01	1.5	men
(VO = 9.0 or 1.0 Vdc)	1G	10	denti w	3.0	s la br	4.50	3.0	built more	3.0	meG
(V _O = 13.5 or 1.5 Vdc)		15	4000 TOO	4.0	Debugan	6.75	4.0		4.0	. ioni
Harris - Harris "1" Level	VIH			15 2 1 117				10 march 17	REPORT OF	adT
(VO = 0.5 or 4.5 Vdc)		5.0	3.5	high" e "law"	3.5	2.75	e selecte	3.5	LANGE & PELL	Vdc
(V _O = 1.0 or 9.0 Vdc)		10	7.0	Wel a	7.0	5.50	stanise s	7.0	AC14556	431.12
(VO = 1.5 or 13.5 Vdc)		15	11.0	(81-70-1	11.0	8.25	as formas	11.0	ed decod	bush
Output Drive Current (AL Device)	ГОН	-	1	tivab 99	241.5W	0.20	COSA vari	11.0	nd bavoid	mAdc
(V _{OH} = 2.5 Vdc) Source	тОН	5.0	-3.0	mibasob	-2.4	-4.2	o sboo	-1.7	pplication	MAGC
(V _{OH} = 4.6 Vdc)	Stor	5.0	-0.64	Enable	-0.51	-0.88	demulti	-0.36	tion gont	saleo
(V _{OH} = 9.5 Vdc)		10	-1.6		-1.3	-0.86 -2.25	late trac	-0.36	ni (tuqni	stab
(VOH = 13.5 Vdc)	MI	15	-4.2	_	-3.4	-8.8	enn± III A	-0.9	any 9 abo	0.0
			-	-		-	136137 2123			-
(V _{OL} = 0.4 Vdc) Sink	IOL	5.0	0.64	-	0.51	0.88	V-10 %	0.36	imntt seid	mAdc
(V _{OL} = 0.5 Vdc)		10	1.6	-	1.3	2.25 8.8	D Would	0.9	igiti svita	A e
(*OL -1.5 vdc)		15	4.2	UXBL	3.4	8.8	-	2.4		1
Output Drive Current (CL/CP Device)	ЮН				1311	1			And the same	mAdc
(VOH = 2.5 Vdc) Source		5.0	-2.5	-	-2.1	-4.2	-	-1.7	Mospued:	3 0
(V _{OH} = 4.6 Vdc)		5.0	-0.52	-	-0.44	-0.88	0,2 = 80	-0.36	foV7 lqq	S
(VOH - 9.5 VOC)		10	-1.3	-	-1.1	-2.25	-	-0.9	dugiuO t	A 10
(V _{OH} = 13.5 Vdc)		15	-3.6		-3.0	-8.8	_	-2.4	-	
(VOL = 0.4 Vdc) Sink	IOL	5.0	0.52	3 800 %	0.44	0.88	DWT TO	0.36	TO SIGNA	mAdc
(V _{OL} = 0.5 Vdc)		10	1.3	eta E sate	1.1	2.25	_	0.9	NOTIE Y	10
(V _{OL} = 1.5 Vdc)		15	3.6	-	3.0	8.8	-	2.4	great su	10
Input Current (AL Device)	lin	15	-	± 0.1	-	±0.00001	±0.1	-	± 1.0	μAdc
Input Current (CL/CP Device)	lin	15	_	± 0.3		±0.00001	± 0.3	-	±1.0	μAdc
Input Capacitance	Cin	_	1	-	- 1	5.0	7.5	110/4) 88	MITEARI	pF
(V _{in} = 0)	-111		-	-	1	0.0000000000000000000000000000000000000	7.0	110-21 00	2017-7471	100
Quiescent Current (AL Device)	1	5.0		5.0	todas	0.005	5.0	Brus	150	μAdc
(Per Package)	IDD	10	91-	10	00	0.003	10		300	идис
		15	8.0 4	20	mV	0.015	20	_ 11	600	Voltag
October 10 Control (CL) (CR) Desire)	Town I	_		-	1			1		10 9100
Quiescent Current (CL/CP Device)	IDD	5.0	1 20	20	1	0.005	20	- spinsA	150	μAdc
(Per Package)	BAMB	10	30	40	-A7	0.010	40	13	300	Ber / S
the the blocker leaders to a Lat		15	- 00	80		0.015	80	1	600	-
Total Supply Current**†	IT	5.0	001			.85 μA/kHz		Sgru		μAdc
(Dynamic plus Quiescent,	0	10				.7 μA/kHz)				
Per Package)	0 11	15			IT = (2	.6 μA/kHz)	f + IDD			
(CL = 50 pF on all outputs, all	0 11		1							
buffers switching)				STREET, F.	100			5533	0.7.09.4	

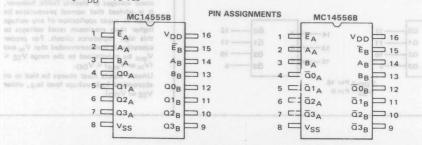
 $T_{low} = -55$ °C for AL Device, -40°C for CL/CP Device.

Thigh = +125°C for AL Device, +85°C for CL/CP Device.
Noise immunity specified for worst-case input combination. Noise Margin for both "1" and "0" level =

1.0 Vdc min @ V_{DD} = 5.0 Vdc 2.0 Vdc min @ V_{DD} = 10 Vdc 2.5 Vdc min @ V_{DD} = 15 Vdc

† To calculate total supply current at loads other than 50 pF: I_T (C_L) = I_T (50 pf) + 2×10^{-3} (C_L -50) V_{DD}f. where: I_T is in μ A (Per Package) C_L in pF, V_{DD} in Vdc and f in kHz is input frequency.

** The formulae given are for the typical characteristics only at 25°C.





Characteristic	Symbol	VDD	Min	Тур	Max	Unit
Output Rise Time tTLH = (3.0 ns/pF) CL + 30'ns tTLH = (1.5 ns/pF) CL + 15 ns tTLH = (1.1 ns/pF) CL + 10 ns	^t TLH	5.0 10 15	-	100 50 40	200 100 80	ns
Output Fall Time tTHL = (1.5 ns/pF) CL + 25 ns tTHL = (0.75 ns/pF) CL + 12.5 ns tTHL = (0.55 ns/pF) CL + 9.5 ns	THL THL Whose langth and 64. The	5.0 10 15	cked wriel show	100 50 40	200 100 80	ns anT
Propagation Delay Time — A, B to Output tp_H, tpHL = (1.7 ns/pF) CL + 135 ns tp_H, tpHL = (0.66 ns/pF) CL + 62 ns tp_H, tpHL = (0.5 ns/pF) CL + 45 ns	tPLH, tPHL	5.0 10 15	(11) #2 14	95	440 190 140	haddens haldens had sent
Propagation Delay Time — E to Output tp[H, tpHL = (1.7 ns/pF) CL + 115 ns tpLH, tpHL = (0.66 ns/pF) CL + 52 ns tpLH, tpHL = (0.5 ns/pF) CL + 40 ns	to the state of th	5.0 10 15	rovided to all the lity. — used for validation was	200 85 65	400 170 130	Isolins.

^{*} The formulae given are for the typical characteristics only.

FIGURE 1 - DYNAMIC POWER DISSIPATION SIGNAL WAVEFORMS

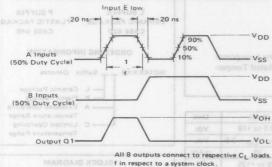
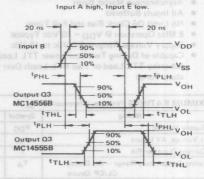
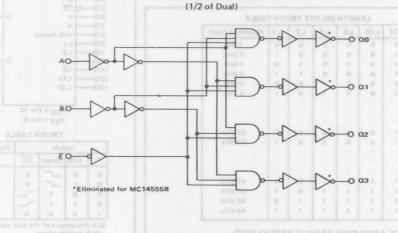


FIGURE 2 - DYNAMIC SIGNAL WAVEFORMS

MOTOROLA



LOGIC DIAGRAM



MC14557B

MOTASSES MOTASSES

1-TO-64 BIT VARIABLE LENGTH SHIFT REGISTER

The MC14557B is a static clocked serial shift register whose length may be programmed to be any number of bits between 1 and 64. The number of bits selected is equal to the sum of the subscripts of the enabled Length Control inputs (L1, L2, L4, L8, L16, and L32) plus one. Serial data may be selected from the A or B data inputs with the A/B select input. This feature is useful for recirculation purposes. A Clock Enable (CE) input is provided to allow gating of the clock or negative edge clocking capability.

The device can be effectively used for variable digital delay lines or simply to implement odd length shift registers. characteristics can be found on the Family Data Sheet.

- Quiescent Current = 10 nA/package typical @ 5 Vdc
- 1-64 Bit Programmable Length
- Q and Q Serial Buffered Outputs
- Asynchronous Master Reset
- All Inputs Buffered
- No Limit On Clock Rise and Fall Times
- 8 MHz Operation @ VDD = 10 Vdc Typical
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range

MAXIMUM RATINGS (Voltages referenced to Vss)

Rating	Symbol	Value	Unit
DC Supply Voltage	V _{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	Vin	-0.5 to V _{DD} + 0.5	Vdc
DC Current Drain per Pin	CONT PRO	10	mAdc
Operating Temperature Range AL Device CL/CP Device	Тд	-55 to +125 -40 to +85	°C
Storage Temperature Range	T _{stg}	-65 to +150	°C

LENGTH	SELECT	TRUTH	TABLE
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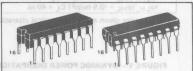
L32	L16	L8	L4	L2	L1	Register Length
0	0	0	0	0	0	1-Bit
0	0	0	0	0	1	2-Bits
0	0	0	0	- 1	0	3-Bits
0	0	0	0	1	1	4-Bits
0	0	0	11	.0	0	5-Bits
0	0	0	1	0	1	6-Bits
						* 11
1	0	0	0	0	0	33 Bits
1	0	0	0	0	1	34-Bits
						-
1	1.00	0-	0.1	-0<	0	61-Bits
1	1	1	1	0	1	62-Bits
1	1	1	1	1	0	63-Bits
1	1	1	1	1	1	64-Bits

Note: Length equals the sum of the binary length control subscripts plus one.

CMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

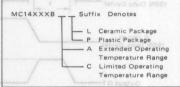
1-TO-64 BIT VARIABLE LENGTH SHIFT REGISTER



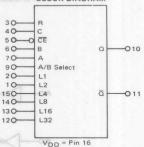
LSUFFIX CERAMIC PACKAGE PLASTIC PACKAGE CASE 620

PSHEELY **CASE 648**

ORDERING INFORMATION



BLOCK DIAGRAM



VSS = Pin 8 TRUTH TABLE

-	Inj	Output		
R	A/B	Clock	CE	Q
0	0		0	В
0	1	_	0	A
0	0	1	~	В
0	1	1	~	A
1	×	X	×	. 0

Q is the output of the first selected shift register stage. X = Don't Care.

ELECTRICAL CHARACTERISTICS

			VDD	Tie	ow*	AT. 3QI	25°C	SOLISI	Th	igh*	HOTH
Characterist	ic 9YT	Symbol	Vdc	Min	Max	Min	Тур	Max	Min	Max	Unit
Output Voltage	"O" Level	VOL	5.0	-	0.05	-	0	0.05	-	0.05	Vdc
Vin VDD or 0	08	10	10	8 -	0.05	-	0	0.05	+ 10 (3)	0.05	HATE
001	40	-	15	-	0.05	-	0	0.05	+ 12 (36	0.05	UT!
	"1" Level	VOH	5.0	4.95	_	4.95	5.0	20.01	4.95	15/11/1/17	Vdc
Vin Oor VDD		011	10	9.95	-	9.95	10	-	9.95	aft Lene	tugtu
200	100		15	14.95	CHILD	14.95	15	_2n 25	14.95	Me (Lf) =	DHTT
Input Voltage#	"0" Level	VIL	12.54					12,5.05	ेक स्वरा	m d1,0) =	Vdc
(Vo = 4.5 or 0.5 Vdc)			5.0	_	1.5	-	2.25	1.5	13[90]	1.5	HTT
(VO = 9.0 or 1.0 Vdc)			10	-	3.0	-	4.50	3.0	-ami	3.0	reporto
(VO = 13.5 or 1.5 Vdc			15	-	4.0	-	6.75	4.0	-(0)	4.0	10 3)
1000	"1" Level	VIH	0	-			\$0.011	+ J3 (R	ion T.P. v	JIMSE HJ	25
(Vo = 0.5 or 4.5 Vdc)			5.0	3.5	-	3.5	2.75	J2 (Ra)	3.5	JH92 HJ	Vdc
(VO = 1.0 or 9.0 Vdc)	159	-	10	7.0		7.0	5.50	+ 10 (%)	7.0	JHW HJ	27
(Vo = 1.5 or 13.5 Vdd			15	11.0	-	11.0	8.25	-	11.0	10-10 D	no (81)
Output Drive Current (AL		ГОН	- 0	11.0		11.0	an UE	F 101146	En V.13 *	15197-14.1	mAdo
(VOH = 2.5 Vdc)	Source	HO	5.0	-3.0	_	-2.4	-4.2	12 136	-1.7	JHW HJ	IIIAG
(V _{OH} = 4.6 Vdc)	DAT	141	5.0	-0.64		-0.51	-0.88	+ 10 (%)	-0.36	JHT HJ	12
(VOH = 9.5 Vdc)	220	440	10	-1.6	DHHUT	-1.3	-2.25	-	-0.9	mibally sel	ioctc Pu
(V _{OH} = 13.5 Vdc)	80	136	15	-4.2	Service of	-3.4	-8.8		-2.4	_	
011	200	2007		-		-	0.00		-		0 -1
(V _{OL} = 0.4 Vdc)	Sink	IOL	5.0	0.64		0.51	0.88		0.36	rinbaw sal	mAdd
(V _{OL} = 0.5 Vdc)	002	008	10	1.6	BHHAP	1.3	2.25	-	0.9	ALLESS SE	14 1905
(V _{OL} = 1.5 Vdc)			15	4.2	-	3.4	8.8	-	2.4	-	
Output Drive Current (CL		ТОН	- 4		-			-			mAdd
$(V_{OH} = 2.5 \text{ Vdc})$	Source		5.0	-2.5	102	-2.1	-4.2	-	-1.7	Bupsa 4 od	lock: Pi
(V _{OH} = 4.6 Vdc)	0.8		5.0	-0.52	-	-0.44	-0.88	-	-0.36	-	
(V _{OH} = 9.5 Vdc)	10.6		10	-1.3	-	-1.1.	-2.25	-	-0.9	-	1105
$(V_{OH} = 13.5 \text{ Vdc})$			15 0	-3.6	HJTF	-3.0	-8.8	- 9	-2.4	ne Pres,er	lock Pa
(VOL = 0.4 Vdc)	Sink	IOL	5.0	0.52	1997	0.44	0.88	-	0.36	-	mAde
(V _{OL} = 0.5 Vdc)			10	1.3	-	1.1	2.25	-	0.9	-	
$(V_{OL} = 1.5 \text{ Vdc})$	250	006	15	3.6	+80	3.0	8.8	0 0-8 10	2.4	urea-don!	of siz
Input Current (AL Device	067	lin	15	-	± 0.1	-	± 0.00001	± 0.1	F16-F33	± 1.0	μAdd
Input Current (CL/CP De	vice)	lin	15	-	± 0.3	-	±0.00001	± 0.3	_	± 1.0	μAdd
nput Capacitance (V _{in} = 0)	-180	Cin	- 0		ML.	-	5.0	7.5	1,16, L32	2, L4, L8,	pF
Quiescent Current (AL De	evice)	IDD	5.0	-	5.0	-	0.010	5.0	-	150	μAdd
(Per Package)	-	.00	10	-	10	-	0.020	10	_	300	etst F
	-	100	15	-	20	-	0.030	20	-	600	
Quiescent Current (CL/CF	Device)	IDD	5.0		50	-	0.010	50		375	μAdo
(Per Package)		.00	10		100	to switch	0.020	100	not see no	750	μΑσι
		200	15	-	200	_	0.030	200	_	1500	
Total Supply Current**†		IT	5.0	WARDAI	G DRIME	I= - /4	1				μAdd
(Dynamic plus Quiesce	ent	.1	10				.75 μA/kHz 1.5 μA/kHz)		-		μΑσο
Per Package) (C _L = 50 pF on all out			15		1		.25 µA/kHz				

L8

L16

L32

30

0

-30

9

17

33

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in} \text{ or } V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD).

SETUP TIME CHART

The nature of the length select logic causes the setup time to vary with the number of bits selected. The following table summarizes the typical variation at V_{DD} = 10 V, T_A = 25°C.

^{*}Tlow = L55°C for AL Device, -40°C for CL/CP Device.

Thigh = +125°C for AL Device, +85°C for CL/CP Device.

=Noise immunity specified for worst-case input combination.

Noise Margin for both "1" and "0" level = 1.0 Vdc min @ VDD = 5.0 Vdc

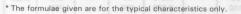
^{2.0} Vdc min @ V_{DD} = 10 Vdc

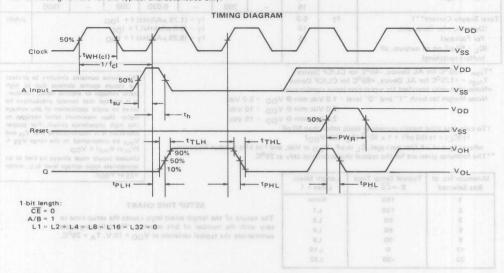
^{2.5} Vdc min @ VDD = 15 Vdc

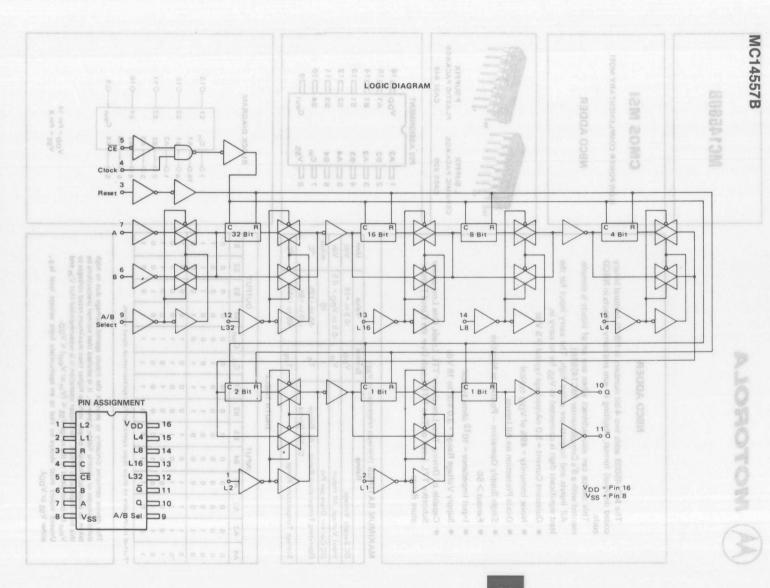
[†]To calculate total supply current at loads other than 50 pF. $I_{T}(C_{L}) = I_{T}(50 \text{ pF}) + 1 \times 10^{-3} \cdot (C_{L} - 50) \text{ V}_{DD}$ where: I_{T} is in μ A (per package), C_{L} in pF, V_{DD} in Vdc, and f in kHz is input frequency. **The formulas given are for the typical characteristics only at 25°C.

Minimum No. of Typical Setup Time B → CE ns Length Select Bits Selected Lines = 1 180 None 120 L1 3 90 L2. 5 60 L4

Characteristic			Symbol	VDD	Vdc	Min	Тур	Max	Unit
Output Rise Time	1 0		20.0		0.8	Joy	Imag. J 1011	51	ns
tTLH = (3.0 ns/pF) CL + 30 ns			t _{TLH}	5.0	ari	1 20	100	200	
tTLH = (1.5 ns/pF) CL + 15 ns			- 80.0	10	35	-	50	100	
tTLH = (1.1 ns/pF) CL + 10 ns				15	0.8	TiesV	40	80	
Output Fall Time	01	20.0		2.0	91			onV	o ns V
tTHL = (1.5 ns/pF) CL + 25 ns			tTHC	5.0	31	-	100	200	
tTHL = (0.75 ns/pF) CL + 12.5 n	S			10		-0V	50	100	neut Voltage
tTHL = (0.55 ns/pF) CL + 9.5 ns	acc		85 1	15	0.8	711/2	40	80	E & - AVI
Propagation Delay Time	4.50	-	tPLH.		01			1.0 V dc 1	
(C or CE to Q or Q)			tPHL		81			or 1.5 Vac)	
tPLH, tPHL = (1.7 ns/pF) CL	+ 415 ns			5.0		HIV	300	1000	
tPLH, tPHL = (0.66 ns/pF) C	+ 167 ns			10	0.8	-	200	400	E.0 - oVI
tPLH tPHL = (0.5 ns/pF) CL	+ 125 ns	0.1		15	01		150	300	0.1 = aV)
(R to Q or Q)		0.11		0.11	81			or 13.5 Vec	ns
tpLH tpHL = (1.7 ns/pF) CL	+ 390 ns		-	5.0		Teol	475	550	BALL Drive
tPLH tPHL = (0.66 ns/pF) C	+ 157 ns			10	5.0	730	190	380	Wan = Z
tPLH, tPHL = (0.5 ns/pF) CL	+ 115 ns			15	0.6		140	280	A - LOVI
Clock Pulse Width	05.5-	6.1-	twH(C)	5.0	0.5	440	220	HabW 6	ns vi
				10	87	136	68	tably a	(VGH o T
				15	0.8	100	50	Total V I	0 = 1600
Reset Pulse Width	2.25	6.7	twH(R)	5.0	0.0	600	300	-(abV)	ns
				10	en	180	90	HobV 8	THE IOVE
				15		120	60	V 100 Tesopor	way () tunted
Clock Pulse Frequency	2.6	1.8-	fcl	5.0	0.2	_	2.5	1.7	MHz
			_ 8	10	0.8	-	8.0	5.0	A NOV
				15	01	_	10.5	6.7	
Clock Pulse Rise and Fall Time	8.6	0.8-	tTLH,	5.0	15			(abV d.	(Very = 1)
			tTHL	20 10	0.8		No Limit		0 = 10V)
				15	01				
Data to Clock Setup Time (A or B to	C or CE)	3.0	t _{su}	5.0	āt	900	250	-JobV 6	ns
L1, L2, L4, L8, L16, L32 = 0			-50	10	81	360	180		nggi Current
			200	15	44	170	135	-0.50	5
Data to Clock Hold Time (A or B to	C or CE)		th	5.0		-225	-450		ns
L1, L2, L4, L8, L16, L32 = 0			-n	10		- 90	-180	(000)	
-,,,,,,,,,,				15		- 60	-135		(0 = g(V)
Reset Fall Time	010.0		1	5.0	-0-0	901	- 100	15	118
			t _{THL}	10	01			5	μs
			20	15	61			4	







ACTASS78

NBCD ADDER

The MC14560B adds two 4-bit numbers in NBCD (natural binary coded decimal) format, resulting in sum and carry outputs in NBCD code

This device can also subtract when one set of inputs is complemented with a 9's Complementer (MC14561B).

All inputs and outputs are active high. The carry input for the least significant digit is connected to VSS for no carry in.

- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- Noise Immunity = 45% of Vpp typical
- Diode Protection on All Inputs
- Single Supply Operation Positive or Negative
- Fanout > 50
- Input Impedance = 10¹² ohms typical
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range

MAXIMUM RATINGS (Voltages referenced to VSS)

Rating	Symbol	Value	Unit
DC Supply Voltage	VDD	-0.5 to +18	Vdc
Input Voltage, All Inputs	Vin	-0.5 to V _{DD} + 0.5	Vdc
DC Current Drain per Pin		10	mAdo
Operating Temperature Range — AL Device CL/CP Device	TA	-55 to +125 -40 to +85	°C
Storage Temperature Range	T _{stg}	-65 to +150	oc

TRUTH TABLE*

	INPUT								OUTPUT					
A4	A3	A2	A1	B4	В3	B2	B1	Cin	Cout	54	S3	S2	S1	
0	0	0	0	0	0	0	0	0	0	0	0	0	0	
0	0	0	0	0	0	0	0	1	0	0	0	0	1	
0	1	0	0	0	0	1	1	0	0	0	1	1	1	
0	1	0	0	0	0	1	1	1	0	1	0	0	0	
0	1	1	1	0	1	0	0	0	1/	0	0	0	1	
. 0	1	1	1	0	.1 .	0	0	1	1	0	0	1	0	
1	0	0	0	0	1	0	1	0	1	0	0	1	1	
0	1	1	0	1	0	0	0	0	1	0	1	0	0	
1	0	0	1	m1 ee	0	0 -	1	1	1	1	0/	0	1	

*Partial truth table to show logic operation for representative input values.

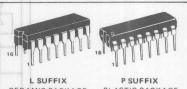
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

CMOS MSI

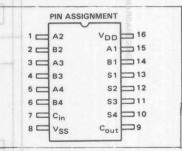
(LOW-POWER COMPLEMENTARY MOS)

NBCD ADDER

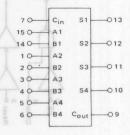


L SUFFIX P SU
CERAMIC PACKAGE PLASTIC
CASE 620 CAS

P SUFFIX PLASTIC PACKAGE CASE 648







V_{DD} = Pin 16 V_{SS} = Pin 8

3

ELECTRICAL CHARACTERISTICS

tinU		dA.	nilli.	·VDD	Tic	ow*		25°C		The Character	igh °	
	Characteristic		Symbol	Vdc	Min	Max	Min	Тур	Max	Min	Max	Unit
Output Volta	age	"0" Level	VOL	5.0	-	0.05	-	0	0.05	* 1271.48	0.05	Vdc
Vin Vo	D or 0	0.9		10	-	0.05	-	0	0.05	# 10 (34)	0.05	TILH
	08	40		15	_	0.05	-	0	0.05	+ 10 (34	0.05	HUTT
		"1" Level	VOH	5.0	4.95	JHTE	4.95	5.0	_	4.95	BURN J. THE	Vdc
Vin 0 o	or VDD	001	OH	10	9.95	-	9.95	10	25 ns	9.95	= (1.5 ms	HTT
	100	50		15	14.95	_	14.95	15	12.5 ms	14.95	- (<u>0</u> .75 n	1613
Input Voltage	p.#	"0" Level	VIL	- 0					- EN 0.8	30 (Jahr	(dg.0) ×	Vdc
	or 0.5 Vdc)		12	5.0		1.5		2.25	1.5	Time	1.5	(consgat)
	or 1.0 Vdc)			10		3.0	-	4.50	3.0	_	3.0	Tio A
-	.5 or 1.5 Vdc)	750		15	_	4.0	-	6.75	4.0	T.T walpf	4.0	9 191
0	900	"1" Level	VIH	0				30 33	21 101	dreu earn	- Thidt	1731
(Vo = 0.5	or 4.5 Vdc)	220	-110	5.0	3.5		3.5	2.75	101 + 101	3.5	" JEHRI	Vdc
	or 9.0 Vdc)			10	7.0	_	7.0	5.50	_	7.0	100 01	8 10 A
-	or 13.5 Vdc)	680		15	11.0	_	11.0	8.25	00 ± 50	11.0	TOTAL T	191
	Current (AL	Davical	ГОН	- W	1110		11.0	211.11	TYDE	q\zn ou.u	- JH91	mAdo
(V _{OH} = 2		Source	ЮН	5.0	-3.0	1 2	-2.4	-4.2	BF + 10 (-1.7	12Mg1	H ISH
(VOH = 4		Cource		5.0	-0.64		-0.51	-0.88	_	-0.36	1400	Cin to
(VOH = 9		550		10	-1.6		-1.3	-2.25	C, ±46	-0.9	tejer =	191
(VOH = 1		220		15	-4:2	_	-3.4	-8.8	1 + 10 19	-2.4	terus a	1911
(VOL = 0	A V/del	Sink Gat	la.	5.0	0.64	_	0.51	0.88	EL 7 10 (0.36	7 35491	mAd
(VOL = 0	= Vde	SINK	IOL	10	1.6	H 192	1.3	2.25	-	0.36	of subsidiary Til	Omu
(VOL = 1				15	4.2	-	3.4	8.8	_	2.4	_ 8	Cin to
		000		15	4.2		3.4	0.0	20.515	2.4	W. S. E.	
	Current (CL/	71000	ЮН	- 0	0.5				en 191 +	13 (3p)	a aa oi =	mAde
(V _{OH} = 2		Source		5.0	-2.5	-	-2.1	-4.2	215 mi	-1.7	= (0,5 ns	191
(V _{OH} = 4				5.0	-0.52	0.201	-0.44	-0.88	-	-0.36	Dulay Tu	O-mu
(VOH = 9				10	-1.3	7(H)91	-1.1	-2.25	-	-0.9	2	Girs 10
(V _{OH} = 1		088		15	-3.6	-	-3.0	-8.8	- 300	-2.4	4	-
(VOL = 0	.4 Vdc)	Sink	IOL	5.0	0.52	-	0.44	0.88	+ 197 ns	0.36	n 23 0) ×	mAde
$(V_{OL} = 0)$.5 Vdc)	170		10	1.3	-	1.1	2.25	145 ms	0.9	an 3.01 +	1497
(V _{OL} = 1	5 Vdc)			15	3.6	-	3.0	8.8	-	2.4	-	1030
Input Curren	t (AL Device)		lin	15	-	± 0.1	THU BUILDI	±0.00001	± 0.1	101 316 D	± 1.0	μAdd
nput Curren	t (CL/CP Devi	ce)	lin	15	-	± 0.3	-	±0.00001	± 0.3	-	±1.0	μAdd
Input Capacit	tance		Cin	_	19.	-	_	5.0	7.5	-	-	pF
(Vin = 0)												
	rrent (AL Dev	ice)	IDD	5.0	-	5.0	-	0.005	5.0	-	150	μAde
(Per Packa			טטי	10		10	_	0.010	10	_	300	1
	-3			15	-	20	-	0.015	20	-	600	108
Outesant Cu	rrent (CL/CP	Davisal	lee	5.0	_			0.005	20			0.4
(Per Packa		Device	IDD	10		20	SMROS	0.005	40	POWER	150 300	μAd
(rer rack)	age/			15		40 80	-	0.010	80	-		
	0		-		-	80	1 - 11				600	1
Total Supply			IT	5.0				.68 μA/kHz				μAde
	plus Quiescen	ι,		10				.35 μA/kHz				
Per Packa		90%		15	1 74 1		IT = (5	.03 μA/kHz				
(0) = 50	pF on all outp	uts, all	4	tuain) Aung								

^{*} T_{low} = -55°C for AL Device, -40°C for CL/CP Device. T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

*Noise immunity specified for worst-case input combination.

Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_DD = 5.0 Vdc

2.0 Vdc min @ V_DD = 10 Vdc

2.5 Vdc min @ V_DD = 15 Vdc

†To calculate total supply current at loads other than 50 pF: T_{CL} = T_{CD} =

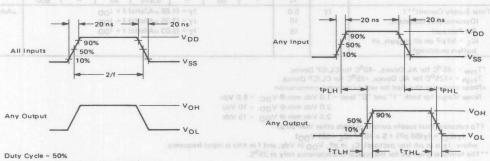
SWITCHING	CHARACTERISTICS*	10.	= 50 nF	T = 250C1

Characteristic			Symbol	1	VDD	W Pu	Min	Тур	Max	Unit
Output Rise Time t _{TLH} = (3.0 ns/pF) C _L + 30 ns t _{TLH} = (1.5 ns/pF) C _L + 15 ns t _{TLH} = (1.1 ns/pF) C _L + 10 ns	9 VT 0 0 0	Min	80.0 80.0 80.0	ristrit	5.0	5.0 10 10	Symbol VOL	100 50 40	200 100 80	ns sloV rugsut
Output Fall Time t _{THL} = (1.5 ns/pF) C _L + 25 ns t _{THL} = (0.75 ns/pF) C _L + 12.5 ns t _{THL} = (0.55 ns/pF) C _L + 9.5 ns	5.0 10 15	4.95 9.95 14.95	tTHL	4.95 9.85 14.95	5.0	0.8 01 21	HO ^V	100 50 40	200 100 80	ns o o _{ni} v
Propagation Delay Time A or B to S tp_H, tp_H = (1.7 ns/pF) C_ + 669 tp_H, tpHL = (0.66 ns/pF) C_ + 29 tp_H, tpHL = (0.5 ns/pF) C_ + 198	97 ns	āt	tPLH,	5.0		5.0 10 21	- Env	750 330 220	2100 900 675	ns ns ns ns ns ns ns ns ns ns ns ns ns n
A or B to C _{out} tp_H, tpHL = (1.7 ns/pF) C _L + 569 tp_H, tpHL = (0.66 ns/pF) C _L + 19 tp_H, tpHL = (0.5 ns/pF) C _L + 14	5 ns 97 ns			7.0	5.0 10 15	9f 8f	Ној	650 230 170	1800 600 450	B. r = QVI
C _{in} to C _{out} tp _{LH} , tp _{HL} = (1.7 ns/pF) C _L + 46: tp _{LH} , tp _{HL} = (0.66 ns/pF) C _L + 13: tp _{LH} , tp _{HL} = (0.5 ns/pF) C _L + 13:	87 ns			1.6 -4.2 -4.2	5.0 10 15	9.0 10 15	-	550 220 160	1500 600 450	5 = HOVI 1 = HOVI 1 = HOVI
Turn-Off Delay Time C _{in} to S tpLH = (1.7 ns/pF) CL + 715 ns tpLH = (0.66 ns/pF) CL + 197 ns tpLH = (0.5 ns/pF) CL + 215 ns	2.25 8.8 -4.2	3.4	tPLH	1.6	5.0 10 15	10	1101	800 350 240	2250 975 750	o nsyl
Turn-On Delay Time C _{in} to S tpHL = (1.7 as/pF) CL + 565 ns tPHL = (0.66 ns/pF) CL + 197 ns tpHL = (0.5 ns/pF) CL + 145 ns	-2.25 -8.8 0.68 2.25	-1.1 -3:0 0:44 1.1	tphL .	-1,3 -3,6 1,3	5.0 10 15	10 15 5,0 10	101	650 230 170	1800 600 450	0 = 10A) 0 = 10A) 0 = 10A)

^{*} The formulae given are for the typical characteristics only.

FIGURE 1 - POWER DISSIPATION WAVEFORMS

FIGURE 2 - SWITCHING TIME WAVEFORMS



Duty Cycle = 50%
All outputs connected to respective C_ loads
f = System clock frequency

MOTOROLA

53

81 82

В3 B4 Cout

FUNCTIONAL EQUIVALENT LOGIC DIAGRAM

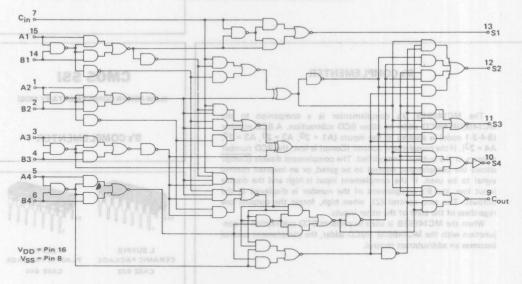
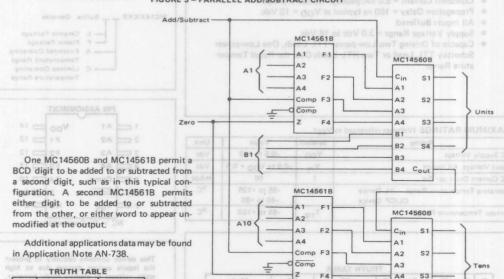


FIGURE 3 - PARALLEL ADD/SUBTRACT CIRCUIT



Zero	Add/Subtract	Result
0	ne to no realign	B plus A
0	1.	B minus A
1V.	and had X	В

X = Don't Care

B10



MC14561B

BUDGALUM

9's COMPLEMENTER

The MC14561B 9's complementer is a companion to the MC14560B NBCD adder to allow BCD subtraction. A BCD number (8-4-2-1 code) is applied to the inputs (A1 = 2^0 , A^2 = 2^1 , A^3 = 2^2 , A^4 = 2^3). If the complement control (Comp) is low, the BCD number appears at the outputs unmodified. The complement disable (Comp) allows the complement control to be gated, or an inverted control signal to be used. If the complement input is high and the disable input low, the 9's complement of the number is displayed at the outputs. The zero control (Z), when high, forces the outputs low regardless of the state of the other inputs.

When the MC14561B is used to perform BCD subtraction in conjunction with the MC14560B NBCD adder, the complement control becomes an add/subtract control.

- Propagation Delay = 160 ns typical at VDD = 10 Vdc
- All Inputs Buffered
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range

MAXIMUM RATINGS (Voltages referenced to VSS)

Rating	Symbol	Value	Unit
DC Supply Voltage	VDD	-0.5 to +18	Vdc
Input Voltage, All Inputs	Vin	-0.5 to V _{DD} + 0.5	Vdc
DC Current Drain per Pin	1	10	mAdc
Operating Temperature Range AL Device CL/CP Device	STATA	-55 to +125 -40 to +85	°C .
Storage Temperature Range	T _{stg}	-65 to +150	°C

TRUTH TARLE

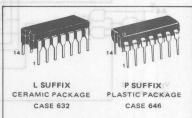
	-	_	_	_		and the second second second	The second secon
Z	Comp	Comp	F1	F2	F3	F4	Mode
0	0	0					-
0	0	1	A1	A2	A3	A4	Straight-through
0	1	1		9			
0	1	0	Ā1	A2	A2A3 + A2A3	Ā2Ā3Ā4	Complement
1	×	×	0	0	0	0	Zero

X = Don't Care.

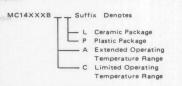
CMOS SSI

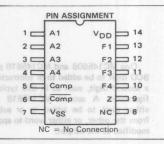
(LOW-POWER COMPLEMENTARY MOS)

9's COMPLEMENTER



ORDERING INFORMATION





This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD).

ELECTRICAL CHARACTERISTICS

	xel/t	qyY	midit	VDD	TI	ow*wo		25°C	SHOWE	Thi	gh *	
20	Characteristi	С	Symbol	Vdc	Min	Max	Min	Тур	Max	Min	Max	Unit
Output Vo	Itage	"0" Level	VOL	5.0	-	0.05	-	0	0.05	J01399	0.05	Vdc
Vin V	DD or 0	50	-	10	-	0.05	-	0	0.05	- JOLI Roll	0.05	LITE
	08	0.04		15	-	0.05	-	0	0.05	Jal/3d/	0.05	1177
		"1" Level	VOH	5.0	4.95	JHT ²	4.95	5.0	-	4.95	gent'Elle?	Vdc
Vin 0	or VDD	001	-	10	9.95	-	9.95	10	49.85	9.95	en 8.41 -	HT/
		08	-	15	14.95	-	14.95	15	H (121) H	14.95	TT.00 -	HTT
Input Volta	age#	"0" Level	VIL	- 61					an a.e.	Takkdis	\$0.00 m	Vdc
(VO = 4	1.5 or 0.5 Vdc)			5.0	-	1.5		2.25	1.5	eani?	1.5	appropries
(VO = 9	9.0 or 1.0 Vdc)	400	- 1	10	-	3.0	-	4.50	3.0	Robba F. U	3.0	Total
(VO = 1	3.5 or 1.5 Vdc)		7	15	-	4.0	-	6.75	4.0	than 28.01	4.0	199
		"1" Level	VIH	01				30)		iglan d.G	* TH35.	1997
).5 or 4.5 Vdc)			5.0	3.5	- , yit	3.5	2.75	the typic	3.5	vig m alum	Vdc
(Vo = 1	1.0 or 9.0 Vdc)			10	7.0	-	7.0	5.50	-	7.0	-	
(VO = 1	1.5 or 13.5 Vdc)			15	11.0	-	11.0	8.25	****	11.0	-	
Output Dri	ve Current (AL	Device)	ГОН									mAdd
(VOH =	2.5 Vdc)	Source		5.0	-3.0	-	-2.4	-4.2	-	-1.7	-	
(VOH =	4.6 Vdc)			5.0	-0.64	-	-0.51	-0.88	-	-0.36	-	
(VOH =	9.5 Vdc)			10	-1.6		-1.3	-2.25	-	-0.9	-	
(VOH =	13.5 Vdc)			15	-4.2	-	-3.4	-8.8	-	-2.4	-	
(VOL =	0.4 Vdc)	Sink	IOL .	5.0	0.64		0.51	0.88	-	0.36	-	mAde
(VOL =	0.5 Vdc)			10	1.6	-	1.3	2.25	-	0.9	-	
(VOL =	1.5 Vdc)			15	4.2	-	3.4	8.8	-	2.4	-	
Output Dri	ve Current (CL/	CP Device)	ГОН									mAde
(VOH =	2.5 Vdc)	Source		5.0	-2.5	-	-2.1	-4.2	-	-1.7	-	
(VOH =	4.6 Vdc)			5.0	-0.52	-	-0.44	-0.88	-	-0.36	-	1
(VOH =	9.5 Vdc)			10	-1.3	-	-1.1	-2.25	-	-0:9	-	
(VOH =	13.5 Vdc)		216	1015 A	-3.6	MILOTIN	-3.0	-8.8		-2.4	-	1
(VOL =	0.4 Vdc)	Sink	IOL	5.0	0.52	-	0.44	0.88	-	0.36	-	mAdd
(VOL =	0.5 Vdc)			10	1.3		1.1	.2.25	-	0.9	-	
(VOL =	1.5 Vdc)			15	3.6	-	3.0	8.8	-	2.4	-	
Input Curre	ent (AL Device)		lin	15	-	± 0.1	-	±0.00001	±0.1	-	± 1.0	μAdd
Input Curre	ent (CL/CP Devi	ice)	lin	15	-	±0.3	-	±0.00001	± 0.3		± 1.0	μAdd
Input Capa (V _{in} = (Cin	-		-	-	5.0	7.5	-	-	pF
	Current (AL Dev	vice)	IDD	5.0		5.0	_601	0.005	5.0	-	150	μAdo
(Per Pac		ggV	יטטי	10		10		0.010	10	-	300	A
				15	1	20	_	0.015	20	VAT.	600	
Quiescent (Current (CL/CP	Device)	IDD	5.0	4	20	-	0.005	20	-	150	μAdo
(Per Pac		28	.00	10		40	_	0.005	40		300	ДАОС
,, ,, , ,				15	1-2	80	- н.	0.015	80		600	
Total Supp	ly Current**†	ноУ	- IT -	5.0				1.5 µA/kHz			000	μAdo
	nic plus Quiescer			10			1 = (3.0 μA/kHz	1 + 100			μΑσο
Per Pac			son	15				4.5 μA/kHz				
(CL = 5	0 pF on all outp switching)	outs, all						promite				

^{*}Tlow = -55°C for AL Device, -40°C for CL/CP Device.
Thigh = +125°C for AL Device, +85°C for CL/CP Device.
=Noise immunity specified for worst-case input combination.

Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc

2.0 Vdc min @ V_{DD} = 10 Vdc

2.5 Vdc min @ V_{DD} = 15 Vdc

†To calculate total supply current at loads other than 50 pF:

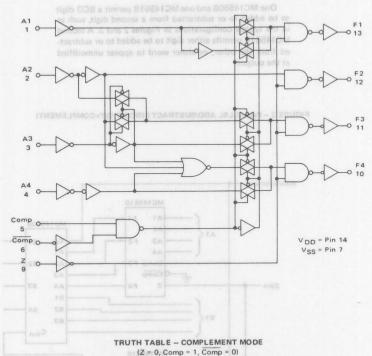
| T_C(C_L) = | T₁(50 pF) + 4 × 10⁻³ (C_L -50) V_{DD}f

where: | T₁ is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

WITCHING CHARACTERISTICS	(CF =	50 pF, TA	(= 25°C)		85			DIR LOGGE
Characteristic	3008		Symbol	VDD	Min	Тур	Max	Unit
Output Rise Time			tTLH	Note: 188	Symbol		Characteristi	ns
tTLH = (3.0 ns/pF) CL + 30 ns			80:0	5.0	JOV	100	200	rioV rugtu
tTLH = (1.5 ns/pF) CL + 15 ns			80.0	10	-	50	100	v .v
tTLH = (1.1 ns/pF) CL + 10 ns			0.05	15	-	40	80	
Output Fall Time	6.8	4.95	tTHL .	1 8.8	NGV I	level "I"		ns
tTHL - (1.5 ns/pF) CL + 25 ns			- 1 86	5.0	- 1	100	200	0 . V
tTHL = (0.75 ns/pF) CL + 12.5 ns			- 36	10	- 1	50	100	
tTHL = (0.55 ns/pF) CL + 9.5 ns				15	TiV	40	80	seda V zuar
Propagation Delay Time	2:25		tPLH,	- I b.a			(ab V 2.0 to 8	ns
tpLH, tpHL = (1.7 ns/pF) CL + 315	ns		tPHL	5.0	-	400	1000	I VO S
tpLH, tpHL = (0.66 ns/pF) CL + 12	7 ns		0.4.	10	-	160	400	CV - CV)
to to (0 5 ne/nE) C. + 05 m			The second second	15		120	300	100

tpLH, tpHL = (0.5 ns/pF) CL + 95 ns $(V_Q=0.8 \text{ at 4.5 Vdc})$ $(V_Q=1.0 \text{ at 9.0 Vdc})$ * The formulae given are for the typical characteristics only. FIGURE 1 - SWITCHING TIME WAVEFORMS (VOH = 13,5 Vde) -20 ns - 20 ns - VDD 7 90% 50% Any Input 010% Vss -tpLH--tPHL 90% 50% Any Output 10% Tipy -55°C for AL Davigs, -40°C for CL/Cr-1HTT.

Think - 125°C for AL Davigs, *85°C for CL/Cr Davigs TLH



nal valent Outpu Inputs Outputs Decir Dec F3 A4 A2 A1 F4 F2 F1 A3 Illegal BCD

0 0

1 0

1 1 0

Input 12

Codes

0 0 1 1

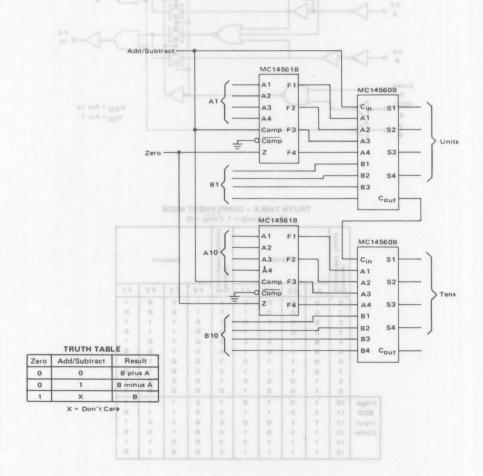
0 0

0 0

TYPICAL APPLICATIONS

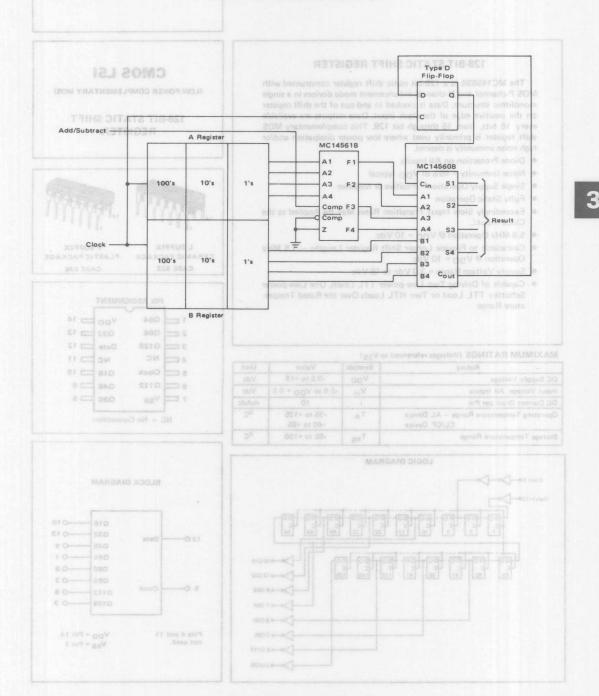
One MC14560B and one MC14561B permit a BCD digit to be added to or subtracted from a second digit, such as in the typical configurations in Figures 2 and 3. A second MC14561B permits either digit to be added to or subtracted from the other, or either word to appear unmodified at the output.

FIGURE 2 - PARALLEL ADD/SUBTRACT CIRCUIT (10's COMPLEMENT)



MC14562B

FIGURE 3 - SERIAL ADD/SUBTRACT CIRCUIT



MC14562B

128-BIT STATIC SHIFT REGISTER

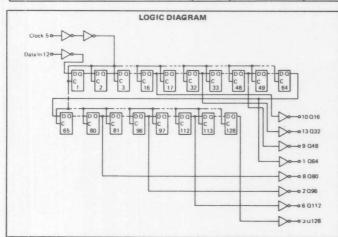
FIGURE 3 - SERIAL ADDISHBTRACT CIRCUIT

The MC14562B is a 128-bit static shift register constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. Data is clocked in and out of the shift register on the positive edge of the clock input. Data outputs are available every 16 bits, from 16 through bit 128. This complementary MOS shift register is primarily used where low power dissipation and/or high noise immunity is desired.

- Diode Protection on All Inputs
- Noise Immunity = 45% of VDD typical
- Single Supply Operation Positive or Negative
- Fully Static Operation
- Exceedingly Slow Input Transition Rates May Be Applied to the Clock Input:
- 5.6 MHz Operation @ VDD = 10 Vdc
- Cascadable to Provide Longer Shift Register Lengths 1.5 MHz Operation @ Vpp = 10 Vdc
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range

MAXIMUM RATINGS (Voltages referenced to VSS)

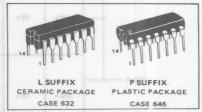
Rating	Symbol	Value	Unit
DC Supply Voltage	VDD	-0.5 to +18	Vdc
Input Voltage, All Inputs	Vin	-0.5 to V _{DD} + 0.5	Vdc
DC Current Drain per Pin	1	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	TA	-55 to +125 -40 to +85	°C
Storage Temperature Range	T _{stg}	-65 to +150	°C

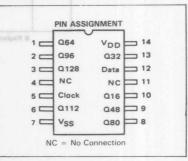


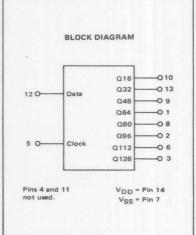
CMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

128-BIT STATIC SHIFT REGISTER.







3

ELECTRICAL CHARACTERISTICS

	Mex	gyT	niM	VDD	TIO	ow*		25°C	aitsiyet	Thi	gh°	
	Characteristi	c	Symbol	Vdc	Min	Max	Min	Тур	Max	Min	Max	Unit
Output V		"O" Level	VOL	5.0	-	0.05	-	0	0.05	+ 75 (30	0.05	Vdc
Vin	V _{DD} or 0	09		10	-	0.05	-	0	0.05	# 1513d	0.05	HJT2
		40		15	-	0.05	-	0	0.05	4 10 (4d	0.05	11177
		"1" Level	VOH	5.0	4.95	1872	4.95	5.0	-	4.95	omij lie	Vdc
Vin	0 or VDD	100	-	10	9.95	-	9.95	10	25 ng	9.95	an 8.1) =	HIT
	100	69	-	15	14.95	-	14.95	15	12. <u>5</u> ns	14.95	= (0.75 n	HITE
Input Vol	tage#	"0" Level	VIL	0					277 (6.0)	Harrida	N 60.07 *	Vdc
(Vo	4.5 or 0.5 Vdc)		- 1	5.0	-	1.5	-	2.25	1.5	<u>bmiT</u>	1.5	Seedot
(Vo	9.0 or 1.0 Vdc)			10		3.0	-	4.50	3.0	-	3.0	Ciack
(Vo	13.5 or 1.5 Vdc)	009		15	-	4.0	-	6.75	4.0	an [_1] =	4.0	1
		"1" Level	VIH					501 / 1.7	30,1401	97 SIQUAZI =	DRA HI	1
(Vo =	0.5 or 4.5 Vdc)	170		5.0	3.5	-	3.5	2.75	+ 10 170	3.5	JHT HU	Vdc
(Vo =	1.0 or 9.0 Vdc)	300	000	10	7.0	14792	7.0	5.50	-	7.0	18 NUMBER	P Asoli
(VO =	1.5 or 13.5 Vdc)	011	230	15	11.0	-	11.0	8.25	-	11.0	DAIN DAU	(B03)
Output D	rive Current (AL	Device)	10Н									mAdd
(VOH	= 2.5 Vdc)	Source	011	5.0	-3.0	151	-2.4	-4.2	-	-1.7	tupo <u>u</u> ? sal	P Asol
(VOH	= 4.6 Vdc)	8.8		5.0	-0.64	-	-0.51	-0.88	-	-0.36	-	
(VOH	= 9.5 Vdc)	0.8	-	10	-1.6		-1.3	-2.25	_	-0.9	-	
(VOH	= 13.5 Vdc)	-170	-20	15 0	-4.2	(1)1007	-3.4	-8.8	-	-2.4	um2=cott	07 876
(VOI	= 0.4 Vdc)	Sink	loL	5.0	0.64	-	0.51	0.88	-	0.36	_	mAde
	= 0.5 Vdc)	00-	0	10	1.6	-	1.3	2.25	_	0.9	_	
	= 1.5 Vdc)	18-	-20	15 0	4.2	10100	3.4	8.8	-	2.4	-	
Output D	rive Current (CL/	(CP Device)	ГОН									mAdo
	= 2.5 Vdc)	Source	011	5.0	-2.5	-	-2.1	-4.2	-	-1.7		
(VOH	= 4.6 Vdc)	263	380	5.0	-0.52	(11)=0	-0.44	-0.88	-	-0.36	Held-tool	of sist
(VOH	= 9.5 Vdc)	103	165	10	-1.3	-	-1.1	-2.25	-	-0.9	-	
(VOH	= 13.5 Vdc)	100	165	15	-3.6	-	-3.0	-8.8	-	-2.4	-	
(VOI	= 0.4 Vdc)	Sink	IOL	5.0	0.52	1017	0.44	0.88	_	0.36	-	mAdo
	= 0.5 Vdc)	007	200	10	1.3	-	1.1	2.25	-	0.9	-	
	= 1.5 Vdc)	203	0.01	15 8	3.6	-	3.0	8.8	-	2.4		
Input Cur	rent (AL Device)		lin	15	-	± 0.1	no imital	±0.00001	± 0.1	not e ra n	± 1.0	μAdd
Input Cur	rent (CL/CP Dev	icel	lin	15	-	± 0.3	-	±0.00001	± 0.3		± 1.0	μAdo
Input Cap		1007	Cin		-	-		5.0	7.5	-	- 1.0	pF
(Vin =			Cin					5.0	7.5			Pr
	Current (AL Dev	vice)	577 1 878 6	5.0	10 #29 Y	5.0	210-951	0 010	5.0	_	150	μAdo
	ackage)	vice/	IDD	10	700	10	10110	0.020	10	_	300	MAGG
1.6.1	ucge,			15		20	-	0.020	20	_	600	
O	Courses ICI ICB	Davise	lee	5.0	-	50			50			1
	Current (CL/CP	Device)	IDD	-	-	100	-	0.010			375	μAdd
(Per Pa	ackage)			10 15		200		0.020	100	_	750 1500	1
T1 C	1.0					200						-
	ply Current**†		IT	5.0			T = (1	94 µA/kHz	f + IDD	E/EQ		μAdd
	mic plus Quiescei	nt,		10				.81 μA/kHz				
	ackage) 50 pF on all outp	aute all		15			1T = (5	.52 μA/kHz				
	rs switching)	outs, all			1							

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in} \text{ or } V_{out})$ < VDD.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD).

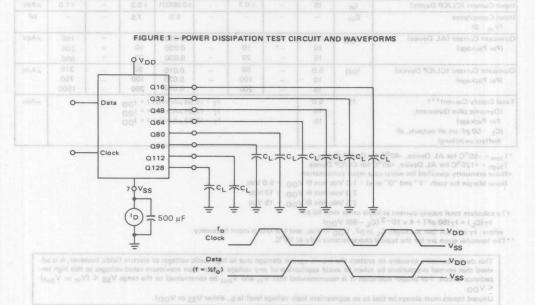
^{*}T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
Thigh = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination

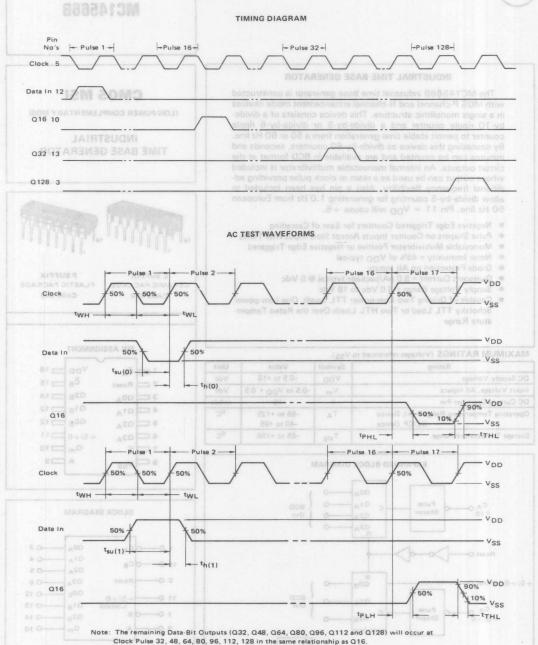
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ VDD = 5.0 Vdc

Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc 2.0 Vdc min @ V_{DD} = 10 Vdc 2.5 Vdc min @ V_{DD} = 15 Vdc 1 To calculate total supply current at loads other than 50 pF: \(\frac{1}{17}(C_L) = \frac{1}{17}(50 \text{ pF}) + 4 \times 10^{-3} (C_L \text{ -50}) V_{DD}f \\
\text{where: } \(\frac{1}{17} \) is in \(\text{ A} \) (Per package), \(C_L \) in \(\text{ F}, V_D \) in Vdc, and f in kHz is input frequency. \(\text{**The formulas given are for the typical characteristics only at 25^OC.} \)

	" rigid T Char	racteristic			Symbol	IT.	1	/DD	Vese	Min	Тур	Max	Unit
Output Rise	Time	Hall.	179	Min	tTLH	- 0	ilvi.		Vde	Symbol		Characteristi	ns
	3.0 ns/pF) CL						-	5.0	5.0	Tov	100	200	neV mani
	1.5 ns/pF) CL			1				10	01	-	50	100	Vin V
tTLH = (1.1 ns/pF) CL	+ 10 ns						15	15	-	40	80	
Output Fall			5.0	4.95	tTHL	3	3.5	1	5.0	HOV	leve.1 "1"		ns
tTHL = (1.5 ns/pF) CL	+ 25 ns		9.95		8	9.9	5.0	10	1 -	100	200	o 0 niV
	0.75 ns/pF) C			14.95		- 8	2.6.1	10	18	-	50	100	
THL = (0.55 ns/pF) C	L + 9.5 ns						15		ToV	40	80	pesta V. suoja
Propagation	Delay Time	1.5	2.25		tPLH.				6.0			(sbV 8.0 to	ns v
Clock to		0.6			TPHL				01			(SBV 0.1 to	
	tPHL = (1.7 r							5.0	31	-	600	1200	Et aVI
	tPHL = (0.66					-	-	10		HIV	250	500	
tPLH,	tPHL = (0.5 m	s/pF) CL +	145 ns	20			EE.	15	na.	-	170	340	8.0 aV1
Clock Pulse I			6.50	7.0	twH		7.0	5.0	10	600	300	(ab\≠0.0 no	
(50% Du	ty Cycle)			0.11			17.0	10	35	220	110	lobV #.E1 to	(Vo - 18
								15		150	75	EAI Transact	burner Oxide
Clock Pulse	Frequency	200	-4.2	-2.4	fcl	0	E-	5.0	5.0	-	1.9	1.1 _{by 8}	MHz
				18.0-		45	1.0-	10	0.8	- 1	5.6	3.0 by a	A HOVE
	- 0.9-	-	-2.25	1.3		8	1-	15	or	-	8.0	4.0 by 8	R = HOVI
Data to Cloc	k Setup Time			-3.A	t _{su} (1)	2		5.0	81	-20	-170	5.5 Vd=	ns VI
				18.0		9		10	5.0	-10	-64	HobV A	0 × 10Vi
				1.3			1.6	15	10	0	-60	TobV 8	0 = 10 V)
				3.6	t _{su} (0)		4.5	5.0	15	-20	-91	5 Vdc)-	ns V
				1			-	10		-10	-58	LJD) Therough	evisO tootus
				1.8-		a		15	5.0	0	-48		(Venez = 2
Data to Cloc	k Hold Time		88.0-	14.0-	th(1)	12	1.0	5.0	5.0	350	263	-(abV 8	ns
				1.1-		8		10	10	165	109		e = HOV)
				-3.0		â		15	15	155	100		HOV)
				0.64	th(0)	- 5	0.5	5.0	5.0	350	267	Uob∀ 5	ns V
				1.1	-		5.1	10	or	200	140	-√stv 8	0 = 10 VI
				3.0				15	81	140	93		f = myVl

* The formulae given are for the typical characteristics only.







MC14566B

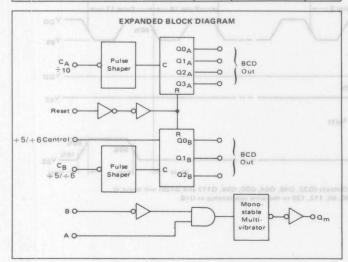
INDUSTRIAL TIME BASE GENERATOR

The MC14566B industrial time base generator is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. This device consists of a divide-by-10 ripple counter and a divide-by-5 or divide-by-6 ripple counter to permit stable time generation from a 50 or 60 Hz line. By cascading this device as divide-by-60 counters, seconds and minutes can be counted and are available in BCD format at the circuit outputs. An internal monostable multivibrator is included whose output can be used as a reset or clock pulse providing additional frequency flexibility. Also a pin has been included to allow divide-by-5 counting for generating 1.0 Hz from European 50 Hz line. Pin 11 = $V_{\mbox{DD}}$ will cause $\div 5$.

- Negative Edge Triggered Counters for Ease of Cascading
- Pulse Shapers on Counter Inputs Accept Slow Input Rise Times
- Monostable Multivibrator Positive or Negative Edge Triggered
- Noise Immunity = 45% of VDD typical
- Diode Protection on All Inputs
- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range

MAXIMUM RATINGS (Voltages referenced to Vos.)

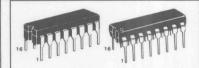
Rating	Symbol	Value	Unit
DC Supply Voltage	V _{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	Vin	-0.5 to V _{DD} + 0.5	Vdc
DC Current Drain per Pin	- 1	10	mAdd
Operating Temperature Range - AL Device CL/CP Device	ТА	-55 to +125 -40 to +85	°C
Storage Temperature Range	T _{stg}	-65 to +150	°C



CMOS MSI

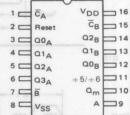
(LOW-POWER COMPLEMENTARY MOS)

INDUSTRIAL
TIME BASE GENERATOR

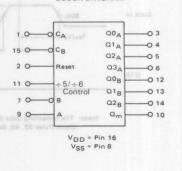


L SUFFIX CERAMIC PACKAGE CASE 620 P SUFFIX
PLASTIC PACKAGE
CASE 648

PIN ASSIGNMENT



BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

	वश्र	21(50)	VDD	Tie	ow*		25°C	2072010	Thi	gh°	
Characteristic		Symbol	Vdc	Min	Max	Min	Тур	Max	Min	Max	Unit
Output Voltage	"0" Level	VOL	5.0		0.05	-	0	0.05	+ 75 (46	0.05	Vdd
Vin VDD or 0	06		10	-	0.05	-	0	0.05	+ J2 (34	0.05	BUTT
- 08	40		15	-	0.05	-	0	0.05	+ 15 (46	0.05	1712
	"1" Level	VOH	5.0	4.95	JRT	4.95	5.0	_	4.95	BUTTLE ING	Vdd
Vin O or VDD	100	0	10	9.95	_	9.95	10	80 (8)	9.95	un distin	INT?
	50	-	15	14.95	_	14.95	15	12.5 at	14.95	= (0 <u>.</u> 75 m	HTT
Input Voltage#	"0" Level	VIL	-					831.010	20 1301	0.00.01	Vdc
(V _O = 4.5 or 0.5 Vdc)			5.0	_	1.5	-	2.25	1.5	Firms, Class	1.5	ogsqc1
$(V_0 = 9.0 \text{ or } 1.0 \text{ Vdc})$	1460	-	10	-	3.0	_	4.50	3.0	30\an \7.4	3.0	1,197
(V _O = 13.5 or 1.5 Vdc)	520	11 1	15	-	4.0	_	6.75	4.0	Tightin_88.0	4.0	4,392
110 10.0 0. 1.0 100,	"1" Level	VIH			4.0		0.70	DES Y JU	THE PROPERTY.	_ JR4	1,191
(Vo = 0.5 or 4.5 Vdc)	. 20101	*10	5.0	3.5	инф.	3.5	2.75	4 to 03 A	3.5	on Delay	Vdc
(V _O = 1.0 or 9.0 Vdc)	008	-	10	7.0	_	7.0	5.50	20 SH	7.0	Van 5_11 =	Hat
(VO = 1.5 or 13.5 Vdc)	318	-	15	11.0	_	11.0	8.25	282_56	11.0	or 88.01 -	Inda.
Output Drive Current (AL	Davios	Jan	15	11.0		11.0	0.25	101 00	11.0	10.01	mAde
	Source	ІОН	5.0	-3.0	(e)144V [†]	-2.4	-4.2		-1.7	drowy se	MAGG
(V _{OH} = 4.6 Vdc)	Source	1200	5.0	-0.64	III) I HAV	-0.51	-0.88	_	-0.36		
	128	SUN	10	-1.6		-1.3	-2.25	_	-0.36	_	
(V _{OH} = 9.5 Vdc)	00	270	15	-4.2		-3.4	-8.8	_	-2.4		
(V _{OH} = 13.5 Vdc)			-	-	-	-			-	arrichal	-
	Sink	IOL	5.0	0.64	19164971	0.51	0.88	-	0.36	MINEDAL DE	mAd
(V _{OL} = 0.5 Vdc)	125	400	10	1.6	-	1.3	2.25	-	0.9	-	1811
(V _{OL} = 1.5 Vdc)		UUP	15	4.2	_	3.4	8.8	-	2.4	-	
Output Drive Current (CL/		ІОН									mAde
011	Source		5.0	-2.5	19-	-2.1	-4.2	-	-1.7	Mahara es	19 at 50 l
(V _{OH} = 4.6 Vdc)	0.1		5.0	-0.52	-	-0.44	-0.88	-	-0.36	-	
(V _{OH} = 9.5 Vdc)	2.5	. 44	10	-1.3	-	-1.1	-2.25	-	-0.9	-	
(V _{OH} = 13.5 Vdc)	4.2	-	15	-3.6	-	-3.0	-8.8	-	-2.4	-	
(VOL = 0.4 Vdc)	Sink	IOL	5.0	0.52	14,149	0.44	0.88	_ 9	0.36	es neigh so	mAde
(VOL = 0.5 Vdc)			10	1.3	SHIFT	1.1	2.25	-	0.9	-	
(VOL = 1.5 Vdc)	JimiJ elf		15	3.6	-	3.0	8.8	-	2.4	-	
Input Current (AL Device)		lin	15	-	± 0.1	-	±0.00001	±0.1	-	± 1.0	μAdd
Input Current (CL/CP Devi	ce)	lin	15	- 1	± 0.3	-	±0.00001	± 0.3	07.50/613	±1.0	μAdo
Input Capacitance	0000	Cin	_			-	5.0	7.5	-		pF
(V _{in} = 0)	900	300	- 0				3.0	7.5			Di.
Quiescent Current (AL Dev	rice)	IDD	5.0	-	5.0	no Tolta	0.005	5.0	tol mp r	150	μAdd
(Per Package)		00	10	-	10	THE SOURCE	0.010	10	-	300	1
			15	-	20	-	0.015	20	-	600	
Quiescent Current (CL/CP	Device)	IDD	5.0	-	20	_	0.005	20	-	150	μAdo
(Per Package)	MAG	BVAW CD	10	0 1637	40	NO SAW	0.005	40		300	Ande
	71110	2 - 201 - 200	15	- 16.711	80	110 11011	0.015	80		600	
Total Supply Current**†		- I-	5.0		00	1 14				000	
(Dynamic plus Quiescen		JT.	10				0 μA/kHz)				μAdd
Per Package)	etog 4		15				0 μA/kHz)				
(C ₁ = 50 pF on all outp		4	15			1T = (3	.0 μA/kHz)	T+ DD			
buffers switching)	uts, all	N									

^{*}Tlow = -55°C for AL Device, -40°C for CL/CP Device.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{In} and V_{Out} be constrained to the range V_{SS} < (V_{In} or V_{Out}) < V_{OD}.

Junused inputs must always be tied to an

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD).

Thigh = +125°C for AL Device, +85°C for CL/CP Device. =Noise immunity specified for worst-case input combination.

Noise Margin for both "1" and "0" level = 1.0 Vdc min @ VDD = 5.0 Vdc

^{2.0} Vdc min @ V_{DD} = 10 Vdc 2.5 Vdc min @ V_{DD} = 15 Vdc

[†]To calculate total supply current at loads other than 50 pF:

I_T(C_L) = I_T(50 pF) + 1 x 10⁻³ (C_L -50) V_{DD}

where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.

**The formulas given are for the typical characteristics only at 25°C.

SWITCHING	CHARAC	TERISTICS*	$(C_1 = 50 \text{ pF})$	TA = 250C)

"dpi	Charact	teristic	2890		Symbol	VDI	D	Min	Тур	Max	Unit
Output Rise Time	niN	MaM	Typ	niM	TTLH	pilVi	2BV	Symbol		iliteires par sont D	ns
tTLH = (3.0 ns/	pF) CL+	30 ns			80.0	5.0	5.0	Tev	100	200	stlpV tugtu
tTLH = (1.5 ns/	pF) CL+	15 ns			0.05	10		70	50	100	OV mV
tTLH = (1.1 ns/	pF) CL+	10 ns			80.0	15	15	-	40	80	111
Output Fall Time	4.95		6.6	4.95	THL	4.9	0.2	HOV	lave J "T"		ns
tTHL = (1.5 ns/						5.0	0.00	==	100	200	vo 0 miV
tTHL = (0.75 ns						10	81	- 1	50	100	
tTHL = (0.55 n	s/pF) CL+	9.5 ns				15		T-cV	40	80	encelow run
Propagation Delay					tPLH,		0.8			0 5 Vec1	ns ns
tPLH, tPHL = (TPHL	5.0		-	1450	1000	(VQ - 9.0)
tPLH, tPHL = (0.4	10	81	-	530	1500	IVO - 13.4
tPLH, tPHL = (0.5 ns/pF)	CL + 295	ns			15		NIV.	320	1000	
Propagation Delay	Time, Res	et to Q3A	2.78	3.6	tPHL	8.6	0.8			or 4.5 Vde)	ns
tpHL = (1.7 ns/	pF) CL+	845 ns				5.0	10	-	930	3000	0.1 - QVI
tpHL = (0.66 ns	s/pF) CL+	282 ns				10	a:	-	315	1000	No - 15
tpHL = (0.5 ns/	pF) CL+	185 ns				15		Tool	210	750	Tenis Clause
Clock Pulse Width	-1.7		-4.2	-2.6	tWH(cl)	-3.0	0.8		Source	(abV de)	s ns
					A	5.0	0.8	1200	400	TobV 2	(VOH = 4)
						10	101	400	125		IVOH = 3
					- 1	15	15	270	90	5 Vdet	
Reset Pulse Width	8.36		88.0	18.0	tWH(R)	18.0	0.8	lou	Sinte	Vdel	o ns
						5.0	10 (1200	400	TobV	0 - 10V)
				3.4	- 1	10	ins i	400	125		(Val. = 1.5
						15		270	90	Liol Thans	swint Ingti
Clock Pulse Freque	ency				fcl	1 - 2	0.8		Source	(abV i	MHz
				-0.44	- 2	5.0	0.0	-	1.0	0.3	IA-HOVI
				1.1-		10	01	_	2.5	1.0	(VOH - 3
	-2.4	-	8.8-	0.8		15	- 81	-	4.2	1.5	(YOH = E
Clock Pulse Rise ar	nd Fall Tin	ne	88.0	0.44	tTLH,	18.0	s.d	301	Sink	Vdcl	(Vot = 0.4
					THL	5.0					(Vol = 0.
			8.8		-	e 8 10			No Limit		T = JOY
21.0 pdde		1.04	100000.0+		600	15	31			(AL Device)	smarting the
Monostable Multiv	ibrator Pul	se Width			tWH(Qm)	-1	ar.	4000	2000	CL/CP Davi	ns
						5.0		1200	2800	0.30	tideas Dans
						10		400	900	-	(0 - mV)
			l character	AND DESCRIPTION OF		15		300	600	ent IAL Dev	riescent Cuci

^{*} The formulae given are for the typical characteristics only.

FIGURE 1 - POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

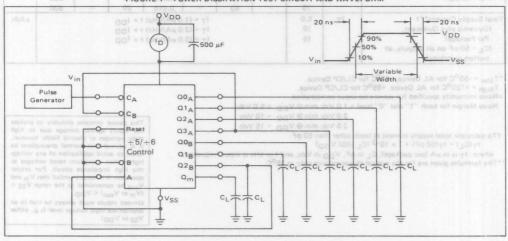
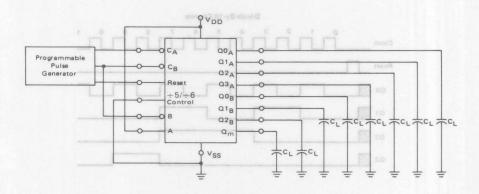
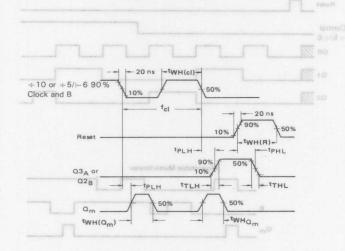


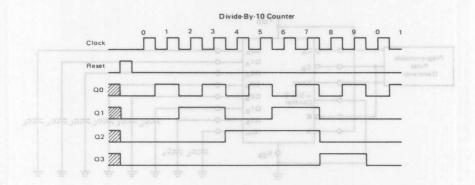
FIGURE 2 - SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

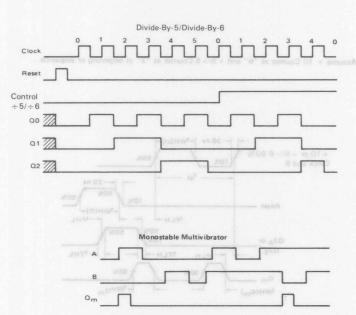




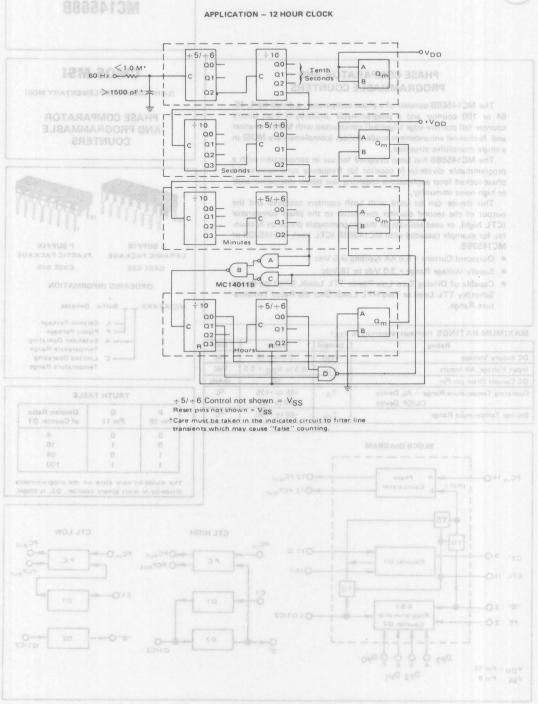


ZMROPEVAN GAATI TIMING DIAGRAM





= Don't Care



MC14568B

PHASE COMPARATOR AND PROGRAMMABLE COUNTERS

The MC14568B consists of a phase comparator, a divide-by-4, 16, 64 or 100 counter and a programmable divide-by-N 4-bit binary counter (all positive-edge triggered) constructed with MOS P-channel and N-channel enhancement mode devices (complementary MOS) in a single monolithic structure.

The MC14568B has been designed for use in conjunction with a programmable divide-by-N counter for frequency synthesizers and phase-locked loop applications requiring low power dissipation and/ or high noise immunity.

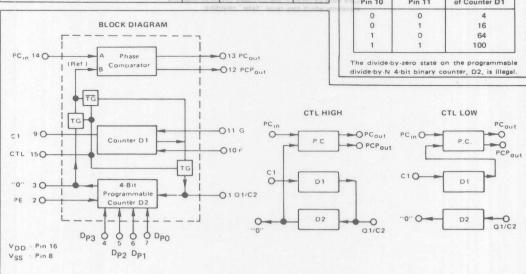
This device can be used with both counters cascaded and the output of the second counter connected to the phase comparator (CTL high), or used separate of the programmable divide-by-N counter, for example cascaded with MC14569B (CTL low), MC14522B or MC14526B

- Quiescent Current = 5.0 nA typ/pkg @ 5 Vdc
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-Power TTL Loads, One Low-Power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range.

MAXIMUM RATINGS (Voltages referenced to VSS)

3

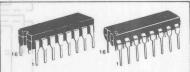
	00		
Rating	Symbol	Value	Unit
DC Supply Voltage	VDD	-0.5 to +18	Vdc
Input Voltage, All Inputs	Vin	-0.5 to V _{DD} + 0.5	Vdc
DC Current Drain per Pin	1-	10	mAdc
Operating Temperature Range AL Device CL/CP Device	TA	-55 to +125 -40 to +85	°C n loune:
Storage Temperature Range	T _{stg}	-65 to +150	°C



CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

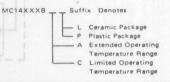
PHASE COMPARATOR AND PROGRAMMABLE COUNTERS



I SHEELY CERAMIC PACKAGE CASE 620

PRIJETY PLASTIC PACKAGE CASE 649

ORDERING INFORMATION

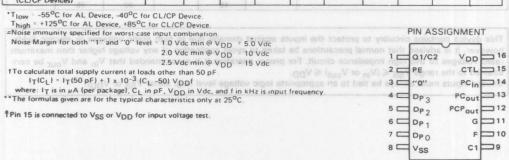


TRUTH TABLE

F Pin 10	G Pin 11	Division Ratio of Counter D1
0	0	4
0	1	16
1	0	64
1	1	100

ELECTRICAL	CHARACT	ERISTICS

rint? - self - qy	Y mitte	VDD		ow*		25°C		h	igh °	
Characteristic	Symbol	Vdc	Min	Max	Min	Тур	Max	Min	Max	Unit
Output Voltage "0" Leve	I VOL	5.0	-	0.05	-	0	0.05	-	0 05	Vdc
V _{in} V _{DD} or 0		10	-	0.05	-	0	0.05	-	0.05	
130 000 111		15	-	0.05		0	0.05	_	0.05	
"1" Leve	VOH	5.0	4.95	JHIT	4.95	5.0	_	4.95	BITEL 1 / 10	Vdc
Via O or VDD		10	9.95		9.95	10		9.95		
08 01	-	15	14.95	-	14.95	15		14.95		
Input Voltage#† "0" L	evel VIL		0	HW	1	STATISTICS THE	102, 01 P	D, TU, 0	DAVA BOUND	Vdc
(VO 4.5 or 0.5 Vdc)	TIL TIL	5.0	DI .	1.5		2.25	1.5		1.5	VIC
(VO 9.0 or 1.0 Vdc)		10	Bit	3.0		4.50	3.0		3.0	
(VO = 13.5 or 1.5 Vdc)	15	15	1. 5.0	4.0	-	6.75	4.0	and Fall	4.0	numix
"1" L	evel VIH	10		THIL	-	0.75		rugas as	24 10 3221	D.AU
(VO 0.5 or 4.5 Vdc)	AIH AIH	5.0	3.5	-	2.5	2.75		3.5		Vdc
(VO - 1.0 or 9.0 Vdc)		10	7.0	-	3.5		-	7.0	ARAGMO	Vac
(VO = 1.5 or 13.5 Vdc)		15 21		neri	7.0	5.50		and the second		off no
			11.0	(172)	11.0	8.25		11.0	75/10/21	
Output Drive Current (AL Device)		18	5.0 10					Coupled	DO , yel-with	mAdd
(VOH = 2.5 Vdc) Source	8 4 5	5.0	-1.2	1897	-1.0	-1.7	-	-0.7	on Thelso	mo m
(V _{OH} = 4.6 Vdc)	r	5.0	-0.25	-	-0.2	-0.36		-0.14	and PCP as	Progus
(V _{OH} = 9.5 Vdc)	1 -	10	-0.62	-	-0.5	-0.9	-	-0.35	-	
(V _{OH} = 13.5 Vdc)	3	15	-1.8	-Zat	-1.5	-3.5	-	-1.1	Jan Turk	NO.
(VOL = 0.4 Vdc) Sink		5.0	0.64	-	0.51	0.88	-	0.36	and PCP	mAde
(VOL = 0.5 Vdc)		10	1.6	-	1.3	2.25	-	0.9	-	1
(VOL = 1.5 Vdc)		15	4.2	-	3.4	8.8	N 1673 00	2.4	MEANY	1.300
Output Drive Current (CL/CP Device	1 ОН									mAde
(VOH = 2.5 Vdc) Source	011	5.0	-1.0	10	-0.8	-1.7	900	-0.6	Clock Pul	759,2751.86
		5.0	-0.2	-	-0 16	-0.36	- 00	-0.12	n Ratio =	Countie
(Va. = 9.5 Vdc)		10	-0.5	-	-0.4	-0.9	_	-0.3		
(V _{OH} = 13.5 Vdc)	10	15	-1.4	-	-1.2	-3.5		-1.0		
(VOI = 0.4 Vdc) Sink	10.1	5.0	0.52	-	0.44	0.88		0.36	DOTE STORY	mAdo
	IOL.	10	1.3		1.1	2.25		0.36	Ī	mAdd
(V _{OL} = 0.5 Vdc) (V _{OL} = 1.5 Vdc)	5.0	15	3.6		3.0	8.8		2.4		
		1-	3.0	111111	3.0		manua c	STATE OF THE PARTY	Tuelon o	· ·
Input Current (AL Device)	lin	15	40 0	± 0.1	la de	± 0.00001	±01	L sola 1	± 1.0	μAdc
Input Current (CL/CP Device)	lin	15	11 - 1	±03	1	±0.00001	± 0.3	-	± 1.0	μAdc
Input Capacitance 030	Cin	-	HE.			5.0	7.5			pF
(V _{in} = 0)			4.8						2 0 m8 o	Manual Tr
Quiescent Current (AL Device)	_	5.0	DF 1	5.0	-	0.005	5.0		150	μAdo
(Per Package) 004 00		10		10	-	0.010	10		300	-
1 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2		15		20	GETIN	0.015	20	ιοινιο	600	ASIDI
Quiescent Current (CL/CP Device)	1	5.0		125	Login	0.005	20			
(Per Package)	IDD	10	0.6	20		0.005	40	ne Frequen	150	μAdo
(Fer Fackage)	3.0	15	Dr.	40		0.015	80		300	(Figure
	0.5	122	12	80					600	
Total Supply Current**1	IT.	5.0	6.0	HUST	1T = (C).2 µA/kHz)	f + IDD			μAdd
(Dynamic plus Quiescent,	-	10	00-).4 µA/kHz)				(Figur
Per Package)		15	27		IT = (0).9 µA/kHz)	f + IDD			
(CL = 50 pr on all outputs, all			5.0	31497					Delay Time	(FO-m)
buriers switching/				Arre			-		1.5	
Three-State Leakage Current, Pins 1, (AL Device)	13 ITL	15	11 -	± 0.1	-	± 0.00001	± 0.1	-	± 3.0	μAdd
Three-State Leakage Current, Pins 1, (CL/CP Devices)	13 I _{TL}	15	01 - 10	± 1.0	-	± 0.00001	± 1.0	-	± 7.5	μAdo



SWITCHING CHARACTERISTICS (C1 = 50 pF, TA = 25°C)

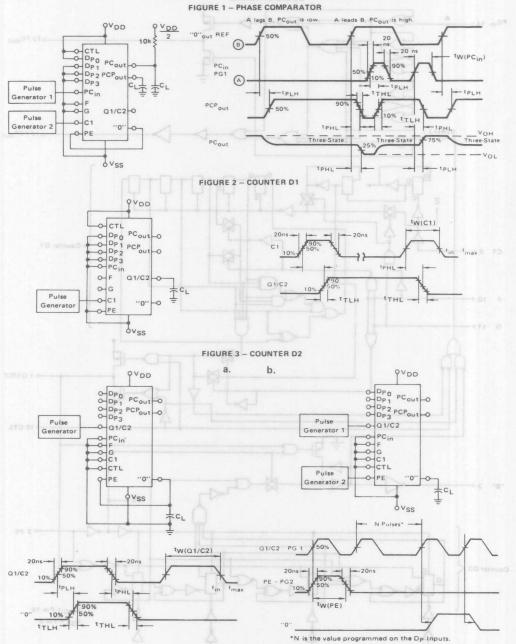
Character	istic	ores	-	Symbol	VDD	Min	Тур	Max	Unit
Output Rise Time				tTLH	5.0		180	360	ns
				80.0	10	TOA	90	180	ag V n V
				20.0	15	-	65	130	Id. W.
Output Fall Time			4.95	tTHL	5.0		100	200	ns
Output rain rime					10	HOV	50	100	100 mV
					15	-	40	80	100 100
Minimum Pulse Width, C1, Q1/0	22, or P	Cin Input		twH	5.0	1 - mv	125	250	ns
		2.25		81	10	1	60	120	Wo 45
				or.	15	-	45	90	00 20
Maximum Clock Rise and Fall T	ime,	8.78		tTLH.	5.0	15	_	or 1.5 Widet	μs
C1, Q1/C2, or PCin Input				tTHL	10	15	Best T	_	
					15	15	-	r.4.5. Vite)	80 DS
HASE COMPARATOR		550	0.5	1	0.0 1 0			(aby 0.8 v	
Input Resistance		8.75	0.11	Rin	5.0 to 15	-	106	r 13.54/del	MΩ
Input Sensitivity, DC Coupled				-	5.0 to 15	NO.	See Inpu	t Voltage	put Drive C
Turn-Off Delay Time,	-	100	0.1	tPHL	5.0	- T	550	1100	ns
PCout and PCPout Outputs				THE	10	_	195	390	BULHON
100				- 1	13.015		120	240	TE - HDV
Turn-On Delay Time,		0.0	0.1	tPHL	5.0		675	1350	ns
PCout and PCPout Outputs				THE	Pa.010 0	101 - 101	300	600	NO: 10 V
- 001				-	80 15	_	190	380	8.0 - JOV
IVIDE-BY-4, 16, 64 OR 10	o cou	NTER (D1	3.8		2.5			TabV	ST - TOA
Maximum Clock Pulse Frequence				fcl		1401	1850/907	DUTCH ICE/C	MHz
Division Ratio = 4, 64 or 100				'CI	5.0	3.0	6.0	Vdc)_s	S. HON
0.12				- 1	10	8.0	16	Vdc)	NON HOY
				- 1	15	10	22	Velet	FB = HOA
Division Ratio = 16					5.0	1.0	2.5	1000	MHz
			0.44		10	3.0	6.3	Vide) S	10A
					15	5.0	9.7	Vdc)	FO - 70A
Propagation Delay Time, Q1/C2	Output		-0-6	tPLH.	95 6		-	- Lob V	ne
Division Ratio = 4, 64 or 10		1000000:		tPHL	5.0		450	900	in ns
35Au 0.11 -				100	10	- 01	190	380	d.Corrent
					15	1 - m3	130	260	и Сариоти
Division Ratio = 16					5.0		720	1440	ns
150 HADC				0.0	10	-001	300	600	seems Curr
				0.1	15	-	200	400	Per Parkage
ROGRAMMABLE DIVIDE	BY-N	4-BIT COU	NTER	(D2)	a				
Maximum Clock Pulse Frequence	v OC	800.0		fcl	5.0	1.2	1.8	0 €0\ <u>U</u> 01 me	MHz
(Figure 3a)	G#		- 1	CI	10	3.0	8.5	30	Per Package
000 -					15	4.0	12		
Turn-On Delay Time, "0" Outp	ut Oliv	TERRITAN S	0) = 31	tour	5.0	-	450	900	o Supply to
(Figure 3a)			0) - 71	tPLH	10		190	380	ns
			0) - 71		15		130	260	Per Package
Turn-Off Delay Time, "0" Outp	uit.			tou	5.0		225	450	900 10
(Figure 3a)				^t PHL	10		85	170	ns
DEAL O.E.			-		15	1771	60	150	e-Store Le
Minimum Preset Enable Pulse W	lidth			*******	5.0		75	250	toineO 18
The set chapte ruise w	1001		-	tWH(PE)	10	371	40	100	ns
									CLICP Det

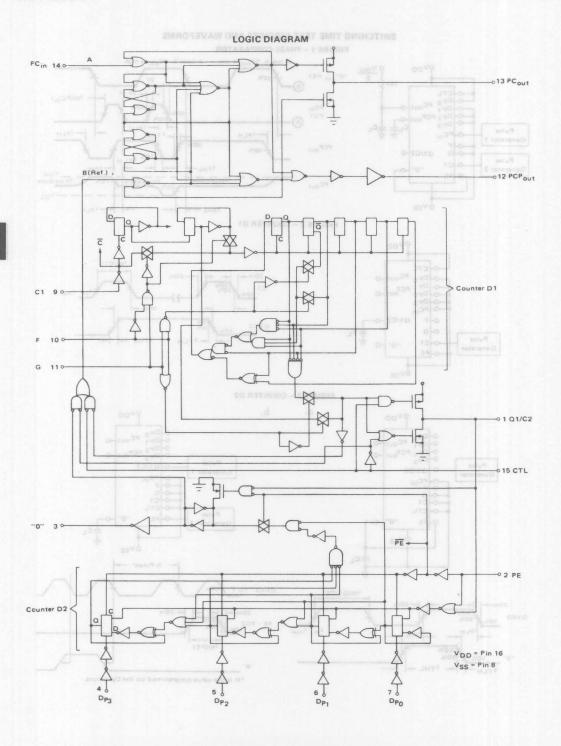
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields: however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that Vin and Vout be constrained to the range $V_{SS} \le (V_{in} \text{ or } V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g. either V_{SS} or V_{DD}).

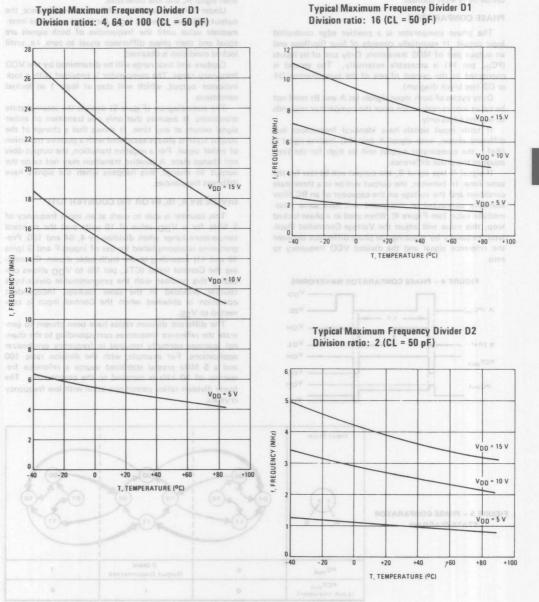
8 T VS8

SWITCHING TIME TEST CIRCUITS AND WAVEFORMS









OPERATING CHARACTERISTICS

The MC14568B contains a phase comparator, a fixed divider (\div 4, \div 16, \div 64, \div 100) and a programmable divide by N 4-bit counter.

PHASE COMPARATOR

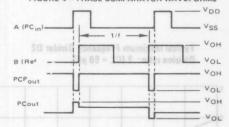
The phase comparator is a positive edge controlled logic circuit. It essentially consists of four flip-flops and an output pair of MOS transistors. Only one of its inputs (PC_{in}, pin 14) is accessible externally. The second is connected to the output of one of the two counters D1 or D2 (see block diagram).

Duty cycles of both input signals (at A and B) need not be taken into consideration since the comparator responds to leading edges only.

If both input signals have identical frequencies but different phases, with signal A (pin 14) leading signal B (Ref.), the comparator output will be high for the time equal to the phase difference.

If signal A lags signal B, the output will be low for the same time. In between, the output will be in a three-state condition and the voltage on the capacitor of an RC filter normally connected at this point will have some intermediate value (see Figure 4). When used in a phase locked loop, this value will adjust the Voltage Controlled Oscillator frequency by reducing the phase difference between the reference signal and the divided VCO frequency to zero.

FIGURE 4 - PHASE COMPARATOR WAVEFORMS



If the input signals have different frequencies, the output signal will be high when signal B has a lower frequency than signal A and low otherwise.

Under the same conditions of frequency difference, the output will vary between VOH (or VOL) and some intermediate value until the frequencies of both signals are equal and their phase difference equal to zero, i.e. until locked condition is obtained.

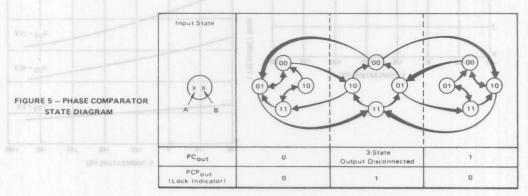
Capture and lock range will be determined by the VCO frequency range. The comparator is provided with a lock indicator output, which will stay at logic 1 in locked conditions.

The state diagram (Figure 5) depicts the internal state transitions. It assumes that only one transition on either signal occurs at any time. It shows that a change of the output state is always associated with a positive transition of either signal. For a negative transition, the output does not change state. A positive transition may not cause the output to change; this happens when the signals have different frequencies

DIVIDE BY 4 16 64 OR 100 COUNTER (D1)

This counter is able to work at an input frequency of 5 MHz for a VDD value of 10 volts over the standard temperature range when dividing by 4, 64 and 100. Programming is accomplished by use of inputs F and G (pins 10 and 11) according to the truth table shown. Connecting the Control input (CTL, pin 15) to VDD allows cascading this counter with the programmable divide-by-N counter provided in the same package. Independent operation is obtained when the Control input is connected to VSS.

The different division ratios have been chosen to generate the reference frequences corresponding to the channel spacings normally required in frequency synthesizer applications. For example, with the division ratio 100 and a 5 MHz crystal stabilized source a reference frequency of 50 kHz is supplied to the comparator. The lower division ratios permit operation with low frequency crystals.



MC14588B

If used in cascade with the programmable divide-by-N counter, practically all usual reference frequencies, or channel spacings of 25, 20, 12.5, 10, 6.25 kHz, etc. are easily achievable.

PROGRAMMABLE DIVIDE-BY-N 4-BIT COUNTER (D2)

This counter is programmable by using inputs Dpo . . .

Dp₃ (pins 7 ... 4). The Preset Enable input enables the parallel preset inputs Dp₀ ... Dp₃. The "0" output must be externally connected to the PE input for single stage applications. Since there is not a cascade feedback input, this counter, when cascaded, must be used as the most significant digit. Because of this, it can be cascaded with binary counters as well as with BCD counters (MC14569B, MC14522B, MC14526B).

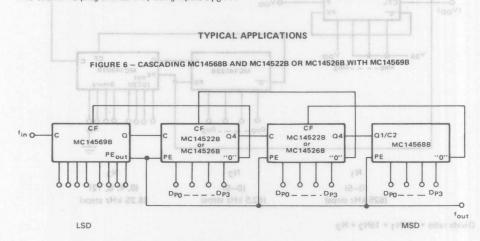
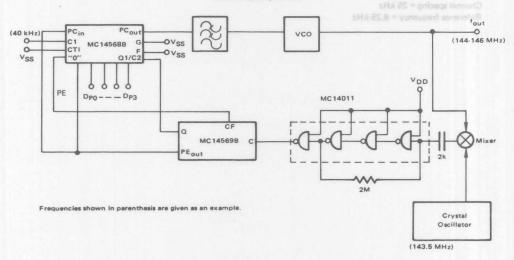
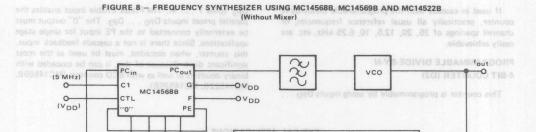


FIGURE 7 — FREQUENCY SYNTHESIZER WITH MC14568B and MC14569B USING A MIXER (Channel Spacing 10 kHz)





MC14522B

DP0 - - - DP3

N₂

(0-9)

(62.5 kHz steps)

"0"

Divide ratio = 160N₁ + 16N₂ + N₃

Example: f_{out} = N₁ (MHz) + N₂ (x100 kHz) + N₃ (x25 kHz)

VDD

DP0----DP3

N₁

(0-5)

(625 kHz steps)

Frequency range = 5 MHz Channel spacing = 25 kHz Figures shown in parenthesis refer to example.

CF

Binary

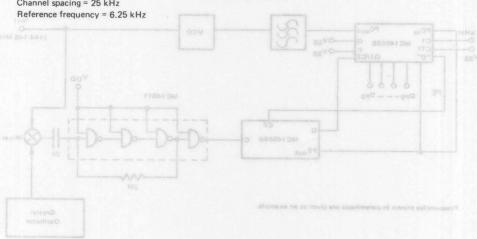
N₃

(0, 4, 8, 12)

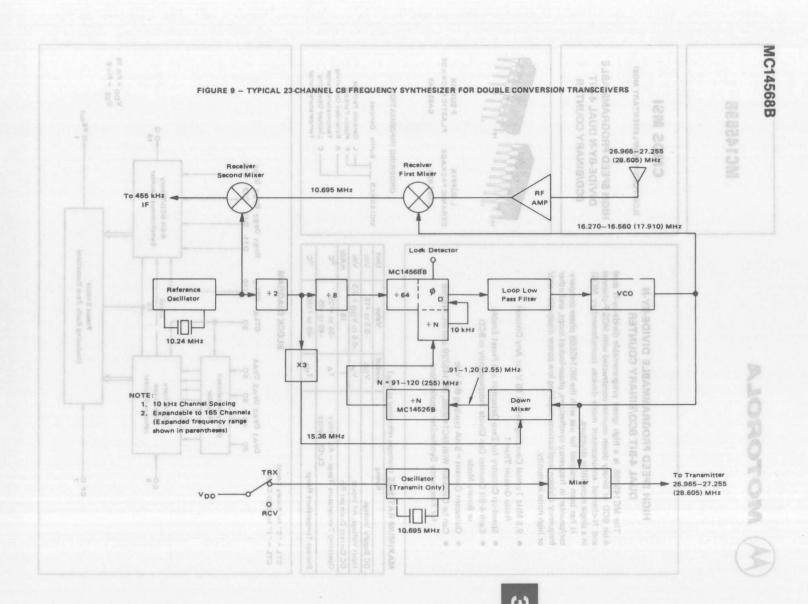
(6.25 kHz steps)

PEout MC14569B

(BCD)







MC14569R

dadcaron

HIGH SPEED PROGRAMMABLE DIVIDE-BY-N

The MC14569B is a high speed programmable divide-by-N dual 4-bit BCD or binary down counter constructed with MOS P-channel and N-channel enhancement mode devices (complementary MOS) in a single monolithic structure.

It has been designed for use with the MC14568B phase comparator/counter in frequency synthesizers, phase-locked loops, and other frequency division applications requiring low power dissipation and/or high noise immunity.

- 9.5 MHz Typical Counting Rate at 10 V for Any Division Ratio Greater Than 1
- Speed-up Circuitry for Zero Detection and Preset Enable
- Each 4-Bit Counter Can Divide Independently in BCD or Binary Mode
- Quiescent Current = 5 nA typ/pkg @ 5 Vdc
- Can be Cascaded With MC14568B, MC14522B and MC14526B for Frequency Synthesizer Applications

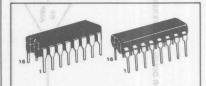
MAXIMUM RATINGS (Voltages referenced to Vss)

Rating		Symbol	Value	Unit
DC Supply Voltage		V _{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs		Vin	-0.5 to V _{DD} + 0.5	Vdc
DC Current Drain per Pin	45	1	10	mAdd
Operating Temperature Range — AL CL/CP	Device Device	TA	-55 to +125 -40 to +85	°C
Storage Temperature Range	9	T _{stg}	-65 to +150	°C

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

HIGH SPEED PROGRAMMABLE DIVIDE-BY-N DUAL 4-BIT BCD/BINARY COUNTER

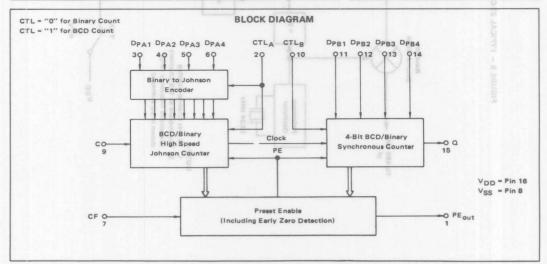


L SUFFIX CERAMIC PACKAGE CASE 620 P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB Suffix Denotes

L Ceramic Package
P Plastic Package
A Extended Operating
Temperature Range
C Limited Operating
Temperature Range



3

FLECTRICAL CHARACTERISTICS

	All Types		VDD	Tie	ow*		25°C		Th	igh *	
Characteristic	2007	Symbol	Vdc	Min	Max	Min	Тур	Max	Min	Max	Unit
Output Voltage	"0" Level	VOL	5.0	-	0.05	-	0	0.05	-	0.05	Vdc
$V_{in} = V_{DD}$ or 0	190	-	10	-	0.05	-	0	0.05	-	0.05	Indane
001	50		15	-	0.05	-	0	0.05	- '	0.05	
. 08	"1" Level	VOH	5.0	4.95		4.95	5.0		4.95		Vdc
$V_{in} = 0$ or V_{DD}	100	On	10	9.95	JHT2	9.95	10	_	9.95	nmil fini	TURTEUR
001	60		15	14.95	-	14.95	15	_	14.95	_	
nput Voltage#	"0" Level	VIL	0								Vdc
(Vo = 4.5 or 0.5 Vdc)		- 11	5.0		1.5	_	2.25	1.5	- 0	1.5	(C-nte)
$(V_0 = 9.0 \text{ or } 1.0 \text{ Vdc})$	420		10 0	3	3.0	-	4.50	3.0	_	3.0	139
$(V_O = 13.5 \text{ or } 1.5 \text{ Vdc})$	179		15		4.0	_	6.75	4.0	_	4.0	197
100 01 1.0 000	"1" Level	VIH	100		4.0		0.70				
$(V_0 = 0.5 \text{ or } 4.5 \text{ Vdc})$		*1H	5.0	3.5	-	3.5	2.75	_	3.5		Vdc
$(V_0 = 1.0 \text{ or } 9.0 \text{ Vdc})$	676		10	7.0		7.0	5.50	_	7.0	5000	1000
(V _O = 1.5 or 13.5 Vdc)	285	-	15	11.0	-	11.0	8.25	_	11.0	_	
	Vi Vi Vi		10	11.0	_	11.0	0.25		11.0		
Output Drive Current (AL		ЮН	F 0	-3.0	UH97	-2.4	-4.2		-1.7	Dellay Fid	mAdd
	Source	-	5.0	-0.64		-0.51	-0.88	_	-0.36	-	PE0
$(V_{OH} = 4.6 \text{ Vdc})$	081		5.0	100000000000000000000000000000000000000	-	-1.3	-2.25		-0.36	-	
$(V_{OH} = 9.5 \text{ Vdc})$	100	-	10	-1.6	-		-0.88	-		-	
(V _{OH} = 13.5 Vdc)	068		15	-4.2	-	-3.4	-	-	-2.4	-	00
$(V_{OL} = 0.4 \text{ Vdc})$	Sink	IOL	5.0	0.64	-	0.51	0.88	-	0.36	-	mAd
$(V_{OL} = 0.5 \text{ Vdc})$	155		10	1.6	-	1.3	2.25	-	0.9	-	
(VOL = 1.5 Vdc)			15	4.2	-	3.4	8.8	-	2.4	-	
Output Drive Current (CL/	CP Device)	10н	100		HAN					THE PARTY NAMED IN	mAd
(VOH = 2.5 Vdc)	Source	, war	5.0	-2.5	-	-2.1	-4.2	-	-1.7	-	
(VOH = 4.6 Vdc)	.08	115	5.0	-0.52	-	-0.44	-0.88	-	-0.36	-	
(VOH = 9.5 Vdc)	3.5	-	10 0	-1.3	101-	-1.1	-2.25		-0.9	to Fengue	Sook Pa
(VOH = 13.5 Vdc)	3.6	-	15 0	-3.6	-	-3.0	-8.8	-	-2.4	-	
(VOI = 0.4 Vdc)	Sink	IOL	5.0	0.52	-	0.44	0.88	_	0.36	-	mAde
$(V_{O1} = 0.5 \text{ Vdc})$		0.	10	1.3	TT HATT	1,1	2.25		0.9	65 SUTF (10)	lock P
(VOL = 1.5 Vdc)	NO LIMIT		15	3.6	THE STREET	3.0	8.8	-	2.4	-	
nput Current (AL Device)		lin	15	-	± 0.1	-	±0.00001	±0.1	-	±1.0	μAdd
nput Current (CL/CP Devi	cel	a elinis o	15	poi - edit	± 0.3	o me old	±0.00001	± 0.3	atel-cos	±1.0	μAdo
nput Capacitance	007			10010, 0119	-	2 2 10 010	5.0	7.5	-	-1.0	pF
(V _{in} = 0)		Cin			_	_	5.0	7.5	-	1	pr
Quiescent Current (AL Dev	rice)	IDD	5.0	PRIZVAI	5.0	1462	0.005	5.0	-	150	μAdo
(Per Package)			10	-	10	-	0.010	10	-	300	
			15	7.380	20	-	0.015	20	-	600	
Quiescent Current (CL/CP	Device)	IDD	5.0	-	50	22 40	0.005	50	0.5	150	μAd
(Per Package)		.00	10	_	100	_	0.010	100	_	300	2.10
	warm? - and	1	15	_	200	- 2	0.015	200	_0	600	1
Total Supply Current**†		IT	5.0			(0.59	μA/kHz)f +	loo	-	1 000	μAd
(Dynamic plus Quiescer	nt.	1	10	100			μΑ/kHz) f +				I AAG
Per Package)			15	1000							
(C ₁ = 50 pF on all outp	uite all	Mat	15			(1.95	μA/kHz)f +	'DD	dy		
buffers switching)	ruts, all										

^{*}Tlow = -55°C for AL Device, -40°C for CL/CP Device.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leqslant (V_{in} \text{ or } V_{out}) \leqslant V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD).

Thigh = +125°C for AL Device, +85°C for CL/CP Device. #Noise immunity specified for worst-case input combination.

Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc

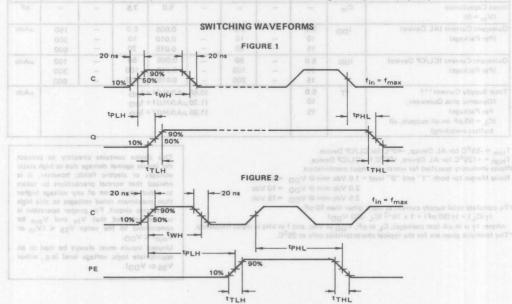
tTo calculate total supply current at loads other than 50 pF:
$$\label{eq:total_loss} \begin{split} &|T(C_L)| = |T(50 \text{ pF}) + 1 \times 10^{-3} \text{ (C}_L - 50) \text{ V}_{DD} \text{f} \\ &\text{where: } |T| \text{ is in } \mu \text{A} \text{ (per package), } C_L \text{ in pF, V}_{DD} \text{ in Vdc, and f in kHz is input frequency.} \end{split}$$
 "The formulas given are for the typical characteristics only at 25°C.

Signature of the second

SWITCHING CHARACTERISTICS (C1 = 50 pF, TA = 25°C)

						wol ^T	V _{DD}	Vie		All Types		
		Charac	cteristic			Symbol	Vdc		Min	Тур	Max	Unit
Output Ri	se Time		00.0	8		tTLH	5.0		304	100	200	ns
						80.0	10		-	50	100	D. H.
						90.0	15		-	40	80	
Output Fa	II Time	9.95		or	3.95	tTHL 8	5.0	1	100	100	200	o o ns V
							10	111	-	50	100	
							15	1	TiV	40	80	earlo V to
Turn-On D	Delay Tim	ne	1.5	25.5	-	tPLH	- 0	8.			(set V 8.0 to	ns
PEout						0.8	5.0	110		420	700	0.8 = oVI
001						0.4	10 3	15	_	175	300	EI - QVI
							15		THY	125	250	
Q Out	out						5.0	1.0	-	675	1200	ns
						- 1	10	10	_	285		0.1 = 0V)
							15	97	1 -	200	400	6 1 = QVI
Turn-Off I	Delay Tir	ne		-4.2	0.5-	tPHL			HOL	1807480	(3A) Menul	ns
PEout							5.0	19	-	380	600	K = HON
							10	18.0	-	150	300	A HOV
							15	3.0	-	100	200	B= HOV
Q Out	put						5.0	-	-	530	1000	ns
mAde							10	1.0	10	225	400	0 = 10 VI
		0.9		2.25	1.3		16	31	-	155	300	0 = 10 A)
Clock Puls	e Width					twH	5.0		300	100	LISI roevos	ns
							10	5.0	150	45	Toby i	IVOH = 2
							15	1.8	115	30	Toby I	Par HOA
Clock Puls	se Freque	ncy #		-2.25	F.T-	fcl	5.0	0.7	-	3.5	2.1	
		-2,4				1 - 1		31	-	9.5	5.7	I = HOV
						- 1	15	1.8	Tol	13.0	7.8	O = LOV
Clock Puls	e Rise an	d Fall Tim	ne	2.26	4.71	tTLH, tTHL	5.0	OI.	1		(strV)	μς
		2.4					10	1.6		NO LIMIT		(VDL = 1
bbAu.						10:1	15	811				mexico Stu

#This implies that zero detection and preset enable are done while the clock is running at the specified frequency.



MC14572UB

OPERATING CHARACTERISTICS

The MC14569B includes a high speed Johnson counter followed by a BCD/binary 4-bit synchronous counter (see block diagram). The use of an encoder allows the Johnson counter to be programmed (i.e. preset) in BCD or binary code through inputs DPA1, DPA2, DPA3, and DPA4.

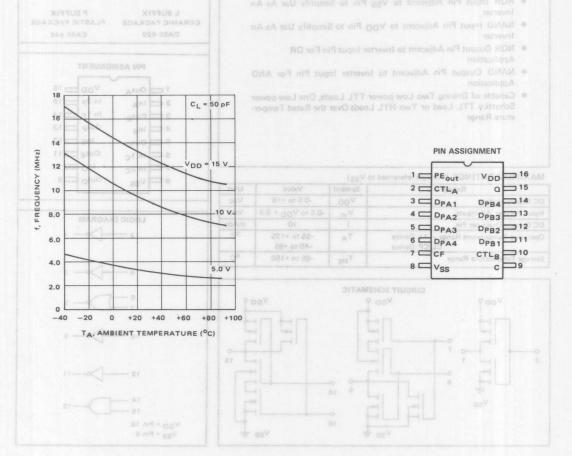
The BCD/binary counter can be programmed through inputs DpB1, DpB2, DpB3, and DpB4. For each counter a divide ratio of 10 (BCD count) or 16 (binary count) can be chosen independently by inputs CTLA and CTLB respectively. When one of those inputs is set high, the divide ratio of the corresponding counter is 10 (BCD); when it is set low, the division ratio is 16 (binary).

A Cascade Feedback input (pin 7), a Q output (pin 15) and a Preset Enable output (pin 1) made it possible to cascade the MC14568B, MC14522B and MC14526B with this device. CF, Q and PEout of MC14569B must be respectively connected to "0", C and PE of the following counter.

When MC14569B is used alone, CF must be connected to VDD. One pulse will appear on output PE_{OUt} every N clock periods (N being the value programmed on the Dp inputs). Both counters included in MC14569B, and eventually all the counters which are cascaded, should normally be preset at the programmed values during the clock period where they all reach the count zero. For best speed performance, preset is started as soon as count 1 is detected. As a consequence, it is not possible to program a frequency division ratio of one. However, it is possible to program a division ratio of 11 (i.e. DPA1, ... DPA4 = 1,0,0,0 and DPB1, ... DPB4 = 1,0,0,0), or a division ratio of 101 if another counter is cascaded with the MC14569B.

This high speed configuration makes it possible to guarantee a maximum clock pulse frequency of 5.7 MHz for a 10 V V_{DD} supply for any division ratio greater than one. Due to the presence of the early zero detection, the circuit must be used in the two least significant digit positions.

Because all the circuitry is static, there is no minimum frequency specification for the Clock input, C (pin 9).





MC14572UB

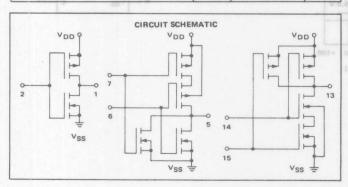
tuelly all the creat HEX GATE should not mally be present the clock

The MC14572UB hex functional gate is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These complementary MOS logic gates find primary use where low power dissipation and/or high noise immunity is desired. The chip contains four inverters, one NOR gate and one NAND gate.

- Quiescent Current = 0.5 nA/package typical @ 5 Vdc
- Noise Immunity = 45% of VDD typical
- Diode Protection on All Inputs are and or sull and
- Single Supply Operation
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Input Impedance = 10¹² ohms typical
- NOR Input Pin Adjacent to VSS Pin to Simplify Use As An Inverter
- NAND Input Pin Adjacent to VDD Pin to Simplify Use As An
- NOR Output Pin Adjacent to Inverter Input Pin For OR Application
- NAND Output Pin Adjacent to Inverter Input Pin For AND
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range

MAXIMUM RATINGS (Voltages referenced to VSS)

Rating	Symbol	Value	Unit
DC Supply Voltage	VDD	-0.5 to +18	Vdc
Input Voltage, All Inputs	Vin	-0.5 to V _{DD} + 0.5	Vdc
DC Current Drain per Pin	1	10	mAdo
Operating Temperature Range - AL Device CL/CP Device	TA	-55 to +125 -40 to +85	°C
Storage Temperature Range	T _{stg}	-65 to +150	°C



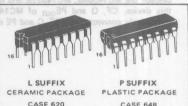
CMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

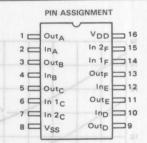
HEX GATE

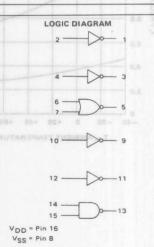
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4 INVERTERS PLUS 2-INPUT NOR GATE PLUS 2-INPUT NAND GATE



CASE 648





ELECTRICAL CHARACTERISTICS

	400平	NSIIN	VDD	TI	ow*		25°C	SITTING	Thi	gh*	
Characteristi	c	Symbol	Vdc	Min	Max	Min	Тур	Max	Min	Max	Unit
Output Voltage	"0" Level	VOL	5.0	6 _	0.05	-	0	0.05	14.15.140	0.05	Vdc
Vin VDD or 0	08	7-	10	-	0.05	-	0	0.05	+ 15 (39	0.05	HATE
130	88	-	15	-	0.05	_	0	0.05	+ 15 140	0.05	HUTT
	"1" Level	VOH	5.0	4.95	THT	4.95	5.0	-	4.95	30/1/10	Vdc
Vin = 0 or VDD		0	10	9.95		9.95	10	_ an 25	9.95	han E_() =	MITT
100		-	15	14.95		14.95	15	12.5 m	14.95	* (0_35 ns	JHET!
Input Voltage#	"0" Level	VIL						11 C/G	"No 1 4014	D1 GG.07 -	Vdc
(V _O = 3.6 or 1.4 Vdc)		12	5.0	_	1.5	-	2.25	1.5	_ami'	1.4	Separation
(V _O = 7.2 or 2.8 Vdc)		-	10	8 _	3.0	-	4.50	3.0	(Figlan C.)	2.9	195.19
(VO = 11.5 or 3.5 Vdc	88	-	15	-	3.75	-	6.75	3.75	1,65 <u>0</u> s/pf	3.6	HJQ!
88	"1" Level	VIH			00		0.70	GF 4 1D	CHANGE AN	HP JH9	3.191
(V _O = 1.4 or 3.6 Vdc)		-111	5.0	3.6	_	3.5	2.75	soired so	3.5	svin-selu	Vdc
(V _O = 2.8 or 7.2 Vdc)			10	7.1		7.0	5.50	-	7.0	_	1
(V _O = 3.5 or 11.5 Vdc)		15	11.4		11.25	8.25	_	11,25	_	
Output Drive Current (AL		ІОН		11.4	-	11.20	0.20		11.20		mAdc
(VOH = 2.5 Vdc)	Source	,OH	5.0	-1.2	_	-1.0	-1.7	_	-0.7		IIIAGC
(V _{OH} = 4.6 Vdc)	Source		5.0	-0.25		-0.2	-0.36	_	-0.14		
(VOH = 9.5 Vdc)			10	-0.62		-0.5	-0.9		-0.35	_	
(V _{OH} = 13.5 Vdc)			15	-1.8	_	-1.5	-3.5	_	-1.1	_	
(V _{OL} = 0.4 Vdc)	Cink	Les	5.0	0.64	-	0.51	-		-		- Ada
(VOL = 0.4 Vdc)	Sink	OL	10	1.6	EST JIMIT	1.3	0.88	FIGUR	0.36	_	mAdc
			15	4.2		3.4	8.8	-	2.4		
(V _{OL} = 1.5 Vdc)			15	4.2		3.4	8.8	_	2.4	_	
Output Drive Current (CL)		ЮН									mAdc
(V _{OH} = 2.5 Vdc)	Source		5.0	-1.0	-	-0.8	-1.7	-	-0.6	-	
(V _{OH} = 4.6 Vdc)			5.0	-0.2	-	-0.16	-0.36	-	-0.12	-	
(V _{OH} = 9.5 Vdc)	adv		10	-0.5	-	-0.4	-0.9	34-	-0.3	-	
(V _{OH} = 13.5 Vdc)	A		15	-1.4	-	-1.2	-3.5	-	-1.0	-	-
$(V_{OL} = 0.4 \text{ Vdc})$	Sink	IOL	5.0	0.52	-	0.44	0.88	-	0.36		mAdc
$(V_{OL} = 0.5 \text{ Vdc})$	0 16		10	1.3	-	1.1	2.25	5 -	0.9	-	
(V _{OL} = 1.5 Vdc)		ugni p	15	3.6	-	3.0	8.8	- 1	2.4	-	
Input Current (AL Device)		1 lin	15		± 0.1	-	±0.00001	± 0.1	-	± 1.0	μAdc
Input Current (CL/CP Dev	ice)	lin	15	-	± 0.3	-	±0.00001	± 0.3	-	±1.0	μAdc
Input Capacitance (Vin = 0)	TI	Cin	-		-	30 2	5.0	7.5	-	-	pF
Quiescent Current (AL De	vice)	IDD	5.0	-	0.25		0.0005	0.25	-	7.5	μAdc
(Per Package)	1	00	10	-	0.50	-	0.0010	0.50	-	15.0	
			15	-	1.00	-	0.0015	1.00	-	30.0	
Quiescent Current (CL/CP	Device)	IDD	5.0	_	1.0	-	0.0005	1.0	_	7.5	μAdc
(Per Package)		.00	10	-	2.0		0.0010	2.0	_	15.0	MAGE
			15	-	4.0	_	0.0015	4.0	_	30.0	
Total Supply Current**†		IT.	5.0			IT = (1	.89 μA/kHz				μAdc
(Dynamic plus Quiescer	nt	1105	10				3.80 μA/kHz				MAGE
Per Package)	C 1000	worth Till	15				.68 µA/kHz				
(C ₁ = 50 pF on all outs	outs all	3005 300K	13	uigni		1 - 10		0			
buffers switching)		2007									1

^{*} T_{low} = -55°C for AL Device, -40°C for CL/CP Device. T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

**Noise immunity specified for worst-case input combination.

17 o calculate total supply current at loads other than 50 pF: $I_T(C_L)$ = $I_T(S_D)$ pF) + 6 × $I_T(S_L)$ = 0.9 V DD where: I_T is in μ A (per package), $I_T(S_L)$ = 0.9 V DD in Vdc, and f in kHz is input frequency.

**The formulas given are for the typical characteristics only at 25°C.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in} \text{ or } V_{out})$ < VDD.

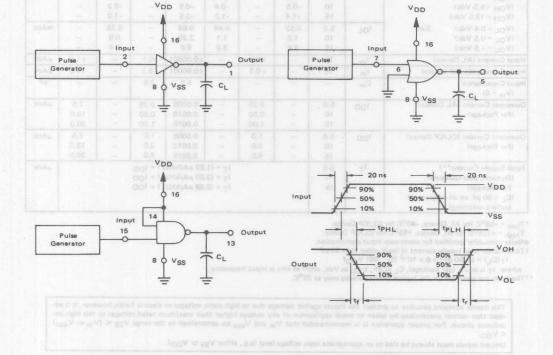
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD).

Characteristic			Symbol	VDD	Min	Тур	Max	Unit
Output Rise Time	gy T	Allo	tTLH	Veter 61a	Symbol		Chargonaristi	ns
tTLH = (3.0 ns/pF) CL + 30 ns			20.0	5.0	Jov	180	360	
tTLH = (1.5 ns/pF) CL + 15 ns			80.0	10	-100	90	180	
tTLH = (1.1 ns/pF) CL + 10 ns			80.0	15	-	65	130	
Output Fall Time	5.0	88.6	tTHL	80 1 08	HOV	lave J "r"		ns
tTHL = (1.5 ns/pF) CL + 25 ns				5.0	NO.	100	200	
tTHL = (0.75 ns/pF) CL + 12.5 ns				10	-	50	100	
t _{THL} = (0.55 ns/pF) C _L + 9.5 ns				15	-,,9	40	80	
Propagation Delay Time	200	15.51	tPLH,	5.0			toby & fixe.	ns ns
tpLH, tpHL = (1.7 ns/pF) CL + 30 ns			tPHL	5.0	-	115	200	
tpLH, tpHL = (0.66 ns/pF) CL + 22 ns			3.75	10		55	110	
tpLH, tpHL = (0.5 ns/pF) CL + 15 ns				15	TurV	40	85	

* The formulae given are for the typical characteristics only.

3





CMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

4 x 4 MULTIPORT REGISTER



4 x 4 MULTIPORT REGISTER

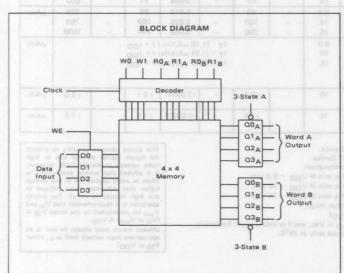
The MC14580B is a 4 by 4 multiport register useful in small scratch pad memories, arithmetic operations when coupled with an adder, and other data storage applications. It allows independent reading of any two words (or the same word at both outputs) while writing into any one of four words.

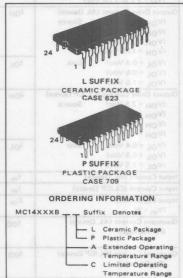
Address changing and data entry occur on the rising edge of the clock. When the write enable input is low, the contents of any word may be accessed but not altered.

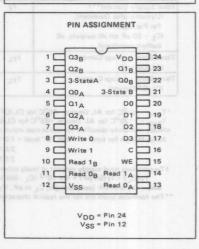
- Logic Swing Independent of Fanout
- No Restrictions on Clock Input Rise or Fall Times
- 3-State Outputs
- Single Phase Clocking
- Quiescent Current = 10 nA/package typical @ 5 Vdc
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range.
- Pin Compatible with CD40108

MAXIMUM RATINGS (Voltages referenced to Vss.)

Rating	Symbol	Value	Unit
DC Supply Voltage	VDD	-0.5 to +18	Vdc
Input Voltage, All Inputs	Vin	-0.5 to V _{DD} + 0.5	Vdc
DC Current Drain per Pin	1	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	TA	-55 to +125 -40 to +85	°C
Storage Temperature Range	T _{stg}	-65 to +150	°C







ELECTRICAL CHARACTERISTICS

		VDD	Tic	w*		25°C		Thi	gh*	
Characteristic	Symbol	Vdc	Min	Max	Min	Тур	Max	Min	Max	Unit
Output Voltage "0" Level	VOL	5.0	-	0.05		0	0.05	-	0.05	Vdc
V _{in} V _{DD} or 0		10	-	0.05	-	0	0.05	-	0.05	
		15	-	0.05	EGIST	1000	0.05	A-3:-A	0.05	
"1" Level	VOH	5.0	4.95	-	4.95	5.0	-	4.95	. 55.5	Vdc
V _{in} 0 or V _{DD}	0	10	9.95	THELD TRIE	9.95	10	a 4 by	9.95	HI DIVI ed	
		15	14.95	HEINGS UR	14.95	15	sordrine,	14.95	ch gad d	38138
nput Voltage# "0" Level	VIL	- 11	нитецьи	ST EWONE	DHS. PC	reamqua s	Selions e	160 TENT	0.008	Vdc
(VO - 4.5 or 0.5 Vdc)		5.0	rive Istue	1.5	your et	2.25	1.5	IN OARS A	1.5	01197
(VO 9.0 or 1.0 Vdc)		10	-	3.0	-	4.50	3.0	a ene yn	3.0	WITH.
(V _O = 13.5 or 1.5 Vdc)		15	T To-out	4.0	it en th	6.75	4.0	prigner	4.0	1
"1" Level	VIH	100	DW YOS	e sineire	w, the ca	ol zi myani	sidene	the write	nedW.s	clock
(V _O = 0.5 or 4.5 Vdc)		5.0	3.5	-	3.5	2.75	ensels to	3.5	races ad	Vdc
(V _O = 1.0 or 9.0 Vdc)		10	7.0	-	7.0	5.50	m teent a	7.0		
(V _O = 1.5 or 13.5 Vdc)		15	11.0	-	11.0	8.25	en Triansi	11.0	LAND THIS	1 73
Output Drive Current (AL Device)	ТОН			2671	1.116.71.31	SALL LAG	MI HOOLD	no engir	o Floritie	mAdd
(V _{OH} = 2.5 Vdc) Source		5.0	-3.0	-	-2.4	-4.2	-	-1.7	State Ou	
(V _{OH} = 4.6 Vdc)		5.0	-0.64	-	-0.51	-0.88	-	-0.36		
(V _{OH} = 9.5 Vdc)		10	-1.6	-	-1.3	-2.25	- 90	-0.9	ngle2Pha	8
(V _{OH} = 13.5 Vdc)		15	-4.2	S Vote:	-3.4	-8.8	AFOI :	-2.4	historia.	1 .
(VOL = 0.4 Vdc) Sink	IOL	5.0	0.64	_	0.51	0.88	_	0.36	_	mAdd
(V _{OL} = 0.5 Vdc)	OL	10	1.6	-	1.3	2.25	DE Page	0.9	oV ylagu	10
(VOL = 1.5 Vdc)		15	4.2	an@ 26	3.4	8.8	J-cwT	2.4	o s k isos	00
Output Drive Current (CL/CP Device)	ІОН		ome T b	maS em	ada Gyes	S.J. J. FRI d	WT to b	10.1.177	volutoris	mAde
(VOH = 2.5 Vdc) Source	·OH	5.0	-2.5	_	-2.1	-4.2	-	-1.7	erus 77 orus	
(V _{OH} = 4.6 Vdc)		5.0	-0.52	-	-0.44	-0.88	ACT (1)	-0.36	in Cōmo	
(V _{OH} = 9.5 Vdc)		10	-1.3		-1.1	-2.25	8-777 LSI	-0.9	dunon u	0.
(V _{OH} = 13.5 Vdc)		15	-3.6	_	-3.0	-8.8	_	-2.4		
(VOI = 0.4 Vdc) Sink	IOL	5.0	0.52	_	0.44	0.88	(910 <u>1</u> 1506)	0.36	HEAR N	mAde
(V _{OL} = 0.5 Vdc)	.OL	10	1.3	SeV _	1.1	2.25	_	0.9	_	I
(VOL = 1.5 Vdc)		15	3.6	134	3.0	8.8		2.4	attenati	
input Current (AL Device)	lin	15	25-10	±0.1	- /	±0.00001	± 0.1	- 1	±1.0	μAdo
Input Current (CL/CP Device)		15	60 40	± 0.3	O V	±0.00001	± 0.3	- 100	±1.0	μAdd
	lin		-						-	-
nput Capacitance	Cin	3-	41.25	01.90	TAT	5.0	7.5	e Range	empirates	pF
(V _{in} = 0)	MICH		284	0100-		93	ACP Design	0		-
Quiescent Current (AL Device)	1DD	5.0	*150T	5.0	072 T	0.010	5.0	Figns P	150	μAdd
(Per Package)		10	-	10	-	0.020	10	-	300	1
The second secon		15	-	20	-	0.030	20	+	600	
Quiescent Current (CL/CP Device)	IDD	5.0	-	50		0.010	50	-	375	μAdd
(Per Package)		10		100		0.020	100	-	750	
Tamper stury Bange		15	-	200	-	0.030	200	-	1500	
Total Supply Current**†	IT	5.0			IT = (1.	18 μA/kHz	f + Ipp			μAdd
(Dynamic plus Quiescent,		10				.91 μA/kHz				
Per Package)		15			IT = (2	.67 μA/kHz	f + IDD			1
(C _L = 50 pF on all outputs, all										
buffers switching)										
Three-State Leakage Current (AL Device)	1 _{TL}	15	-	± 0.1	-	•0.00001	± 0.1	J	±3.0	μAdd
	1	15		±1.0	-	.0.00001	± 1.0		± 7.5	1
(CL/CP Device)	ITL	15	77	A80	7111	0.00001	21.0	7	1 /.5	μAdo

^{*}T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
Thigh = +125°C for AL Device, +85°C for CL/CP Device.

#Noise immunity specified for worst-case input combination.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in} \text{ or } V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD).

Noise Margin for both "1" and "0" level = 1.0 Vdc min @ VDD = 5.0 Vdc

^{2.0} Vdc min @ VDD = 10 Vdc

^{2.5} Vdc min @ VDD = 10 Vdc

2.5 Vdc min @ VDD = 15 Vdc

†To calculate total supply current at loads other than 50 pF:

| T(C_l) = | T|(50 pF) + 4 x 10⁻³ (C_L -50) VDDf

where: I T is in µA (per package), C_L in pF, V_DD in Vdc, and f in kHz is input frequency.

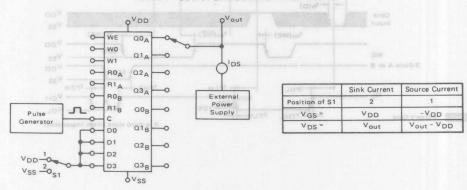
**The formulas given are for the typical characteristics only at 25°C.

SWITCHING	CHARACTERISTICS*	10. = 50 nF	T . = 250(1)

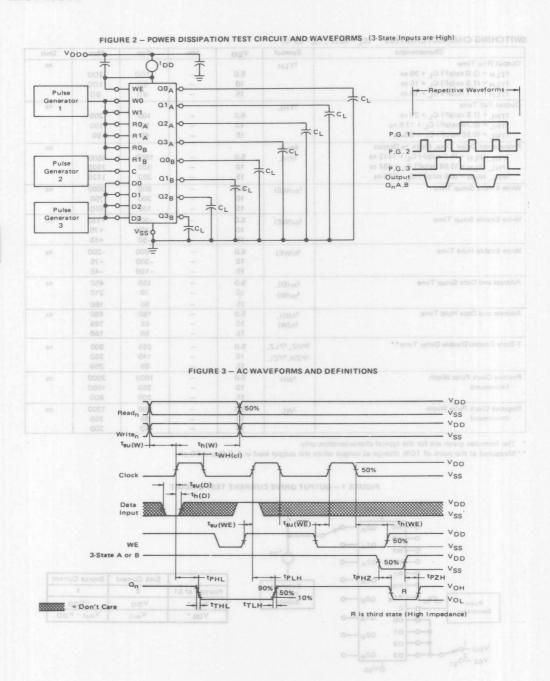
Characteristic	Symbol	VDD	Min	Тур	Max	Unit
Output Rise Time t _{TLH} = (3.0 ns/pF) C _L + 30 ns t _{TLH} = (1.5 ns/pF) C _L + 15 ns	tTLH	5.0 10	Ţ- °	100 50	200	ns Testu4
t _{TLH} = (1.1 ns/pF) C _L + 10 ns		15	_	40	80	- Chermon C
Output Fall Time tTHL = (1.5 ns/pF) CL + 25 ns tTHL = (0.75 ns/pF) CL + 12.5 ns tTHL = (0.55 ns/pF) CL + 9.5 ns	tTHL	5.0 10 15	- 0 4	100 50 40	200 100 80	ns
Propagation Delay Time, Clock to Output tpHL, tpLH = (1.7 ns/pF) CL + 1415 ns tpHL, tpLH = (0.66 ns/pF) CL + 467 ns tpHL, tpLH = (0.5 ns/pF) CL + 325 ns	tPLH, tPHL	5.0 10 15		1500 500 350	4500 1500 1125	ns Pulse reference
Write Enable Setup Time	†su(WE)	5.0 10 15	£ = 0	800 300 180	2000 750 550	ns
Write Enable Setup Time	t _{SU} (WE)	5.0 10 15		-300 -100 -60	+150 +75 +55	ns
Write Enable Hold Time	th(WE)	5.0 10 15		-800 -300 -180	-200 -75 -45	ns
Address and Data Setup Time	t _{su} (D),	5.0 10 15	-	150 70 50	450 210 160	ns
Address and Data Hold Time	^t h(D), ^t h(W)	5.0 10 15	=	160 65 50	480 195 150	ns
3-State Enable/Disable Delay Time**	tPHZ, tPLZ, tPZH, tPZL	5.0 10 15	-	355 140 85	900 350 250	ns
Positive Clock Pulse Width (minimum)	tWН	5.0 10 15		1000 350 200	3000 1050 800	ns
Negative Clock Pulse Width (minimum)	tWL	5.0 10 15		400 85 60	1200 255 200	ns

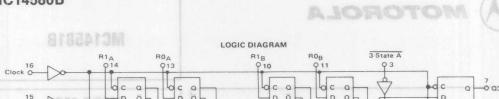
* The formulae given are for the typical characteristics only. **Measured at the point of 10% change at output when the output load in 1,0 Ω and 50 pF.

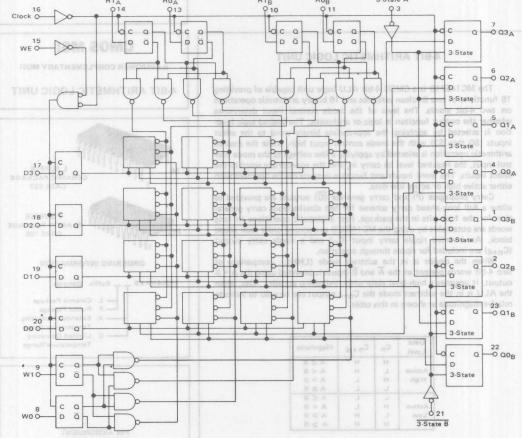
FIGURE 1 - OUTPUT DRIVE CURRENT TEST CIRCUIT











TRUTH TABLE

Clock	WE	Write 1	Write 0	Read 1 _A	Read 0 _A	Read 1 _B	Read 0 _B	3-State A	3-State B	Dn	QnA	Q _n B
	1	0	- 1	0	1	0	1	1	1	. 1	. 1	1.
	1	0	□ a1	0	1	0	1	1	stindu	0	0	0
7	×	×	×	×	X	×	X	lypiqy	5-10 ₁ 0.8	X 8310	No Change	No Change
X	X	X	X	×	X	×	X	0110	1 500 0.6	- X	spiRloV	VIOR .
0	X	×	×	×	X	voq Xvo l	sm(X,ba	JJIT 1	wod-wo.	O.X	No Change	No Change
1	X	X	X	×	X	X	X	INO JUEO	111100	X	No Change	No Change
7	1	0	0	0	1	1	0	1 VasV	y beansel	D _n to word 0	Contents of word 1 displayed	of word 2
7	0	0	0	0	nev 1	BI+ of	0	go V	1	Word 0 not altered	Contents of word 1 displayed	Contents of word 2

R implies high resistance $\sim 10^9$ ohms .

X = Don't care



MC14581B

4-BIT ARITHMETIC LOGIC UNIT

The MC14581B is a CMOS 4-bit ALU logic unit capable of providing 16 functions of two Boolean variables and 16 binary arithmetic operations on two 4-bit words. The level of the mode control input determines whether the output funciton is logic or arithmetic. The desired logic function is selected by applying the appropriate binary word to the select inputs (S0 thru S3) with the mode control input high, while the desired arithmetic operation is selected by applying a low voltage to the mode control input, the required level to carry in, and the appropriate word to the select inputs. The word inputs and function outputs can be operated with either active high or active low data.

Carry propagate $\overline{(P)}$ and carry generate $\overline{(G)}$ outputs are provided to allow a full look-ahead carry scheme for fast simultaneous carry generation for the four bits in the package. Fast arithmetic operations on long words are obtainable by using the MC14582B as a second order look ahead block. An inverted ripple carry input (C_n) and a ripple carry output (C_{n+4}) are included for ripple through operation.

When the device is in the subtract mode (LHHL), comparison of two 4-bit words present at the \overline{A} and \overline{B} inputs is provided using the A = B output. It assumes a high-level state when indicating equality. Also, when the ALU is in the subtract mode the C_{Π^+4} output can be used to indicate relative magnitude as shown in this table:

Data Level	Cn	Cn + 4	Magnitude
	н	н	A≤B
Active	L	н	A < B
High	н	L	A > B
	L	L	A≥B
and the same	L	L	A≤B
Active	н	L	A < B
Low	L	н	A > B
	н	н	A≥B

FEATURES:

- Functional and Pinout Equivalent to 74181.
- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- High Noise Immunity = 45% of VDD typical
- Diode Protection on All Inputs
- Low Input Capacitance 5.0 pF typical
- All Outputs Buffered
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Load, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range

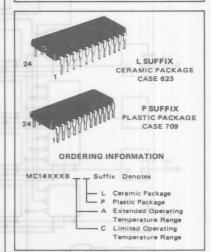
MAXIMUM RATINGS (Voltages referenced to VSS)

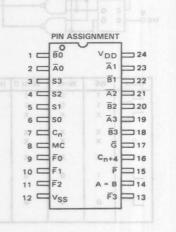
Rating	Symbol	Value	Unit
DC Supply Voltage	V _{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	Vin	-0.5 to V _{DD} + 0.5	Vdc
DC Current Drain per Pin	1	10	mAdd
Operating Temperature Range — AL Device CL/CP Device	TA	-55 to +125 -40 to +85	°C
Storage Temperature Range	T _{stg}	-65 to +150	°C

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

4-BIT ARITHMETIC LOGIC UNIT





ELECTRICAL CHARACTERISTICS

		VDD							igh *	
	Symbol	Vdc	Min	Max	Min	Тур	Max	Min	Max	Unit
"O" Level	VOL	5.0	-	0.05	-	0	0.05	475140	0.05	Vdc
08		10	-	0.05	1	0	0.05		0.05	BUTT
40		15	-	0.05	-	0	0.05	+ 13 (40	0.05	BUT!
"1" Level	VOH	5.0	4.95	JHT	4.95	5.0	-	4.95	6000 T 110	Vdc
001	0	10	9.95	-	9.95	10	<u>In 85</u>	9.95		MIT
- 68		15	14.95	_	14.95	15	12.5 ns	14.95	n d1.0) =	BETT
"0" Level	VII	- 0					STUDIES 1	To (ad/	u ggini A	Vdc
		5.0	-	1.5	-	2.25	1.5	<u>a</u> miT	1.5	
		10		3.0	-	4.50	3.0	_300	3.0	Sumil
302	-	15		4.0	-	6.75	4.0	an T_F} =	4.0	2
"1" Level	VIII	0		4.0	1	28 VIV	_(D-1-4QU	1 (0.95.1)		-
180	TH	50	3.5		2.5	2.75	+ 10 (90	an 3 6 =		
							(ebold s		me2.07 n	mus
208		The case of						1	Named in t	
Devicel	lou	U	11.0		11.0	0.23	JJ 150V	11.0		mAdo
2000	ЮН	5.0	-12		-10	-17	F 13 (3a	-07		
Source										-
320		2.2					0.034	16.030		
		1000	2000	2000	100000			1		
					-			-		-
Sink	OL	400000		-			100	Comment of the Commen	Control of the Contro	-
1000		100		100000000000000000000000000000000000000						
		15	4.2	い対策	3.4		The second	2.4		
and the same of	ЮН	- 0				The second		11-00,U1 T		
Source				-			271.14			
		1000	100000000000000000000000000000000000000	HTA			-			
				-						
48.60%	-		-	-				-		42
Sink	IOL	5.0	0.52	-	0.44	0.88	4 75 140	0.36	and the second second	mAdd
		10	1.3	対力中	1.1		-		huit or ni	CHINA
380		15	3.6	1664	3.0	8.8	+ 75 (34	2.4	JHIP HJ	90
GM	lin	15	-	± 0.1	-	±0.00001	±0.1	0.00	±1.0	μAdd
ce)	lin	15	-	± 0.3	-	±0.00001	± 0.3	20.0094	±1.0	μAdd
200	Cin	- 4	-	2022	-	5.0	7.5		THO OF THE	pF
The state of the s	-111	100		THAI		511.07.7	4 75 1 1 1 1		TH's LEHE	1
	Inn	5.0	-	5.0	-	0.005	5.0		150	μAdo
. 00	.00	10		10	-	100000000000000000000000000000000000000	10	0.01	12.53(20)	
		15	-	20	vino salmit		20	101 416 /		he form
Davical	Inn	5.0		20			20			μAdd
Jevice/	100	the second second second	UP REFI		TOA					MAG
	-	1.77.000		-	-	10.000	10-30-1	-	- Control of the Cont	
	l=	2011/2000	1001 30		555				000	1.04
M BOOM	700		- 55 V (DOTEUTS	1.6 µA/kHz	T + DD	TEST		μAdo
			e'ā enini							
	100	115	20		SAID = C	3. 3 ДА/КН2	לסוי דיי			
uts, all			o'd noint						-	
	"0" Level "0" Level "1" Level "1" Level Source Sink CP Device) Source	"0" Level VOL "1" Level VOH "0" Level VIL "1" Level VIH Device) IOH Source IOH Source IOH Device) IOH Con In	"O" Level VOL 5.0 10 15 "1" Level VOH 5.0 10 15 "0" Level VIL 5.0 10 15 "1" Level VIH 5.0 10 15 Oevice) Source IOH 5.0 10 15 CP Device) IOH 5.0 10 15 Sink IOL 5.0 10 15 CP Device) IOH 5.0 10 15 CP Device IOH 5.0 10 15 15 CP Device IOH 5.0 10 15 15 16 17 18 18 19 19 19 10 10 11 11 11 15 11 11 15 11 11 15 11 11 15 11 11	"O" Level VOL 5.0 — 10 — 110 — 110 — 110 — 111 — 111 — 112 — 113 — 114.95 "O" Level VIL 5.0 — 115 — 116 — 117 — 117 — 118 — 119 — 119 — 110 — 119 — 110 — 119 — 110 — 119 — 110 — 110 — 111 — 1	"O" Level VOL 5.0	To Level Vol. S.0 - 0.05 - 0	"O" Level VOL 5.0 - 0.05 - 0 10 - 0.05 - 0 10 - 0.05 - 0 "1" Level VOH 5.0 4.95 - 9.95 10 15 14.95 - 14.95 15 "0" Level VIL 5.0 - 1.5 - 2.25 10 - 3.0 - 4.50 15 - 4.0 - 6.75 "1" Level VIH 5.0 3.5 - 3.5 2.75 10 7.0 - 7.0 5.50 11.0 - 11.0 8.25 Device) Source 5.0 - 0.64 - 0.51 0.88 10 - 1.6 + -1.3 -2.25 15 - 4.2 - 3.4 8.8 CP Device) Source 5.0 - 0.64 - 0.51 0.88 10 1.6 - 1.3 2.25 15 4.2 - 3.4 8.8 CP Device) Source 5.0 - 0.64 - 0.51 0.88 10 1.6 - 1.3 2.25 15 - 4.2 - 3.4 8.8 CP Device) Source 5.0 - 0.64 - 0.51 0.88 10 1.6 - 1.3 2.25 15 3.6 - 3.6 - 3.0 8.8 10 1.3 - 1.1 2.25 15 3.6 - 3.0 8.8 10 1.3 - 1.1 2.25 15 3.6 - 3.0 8.8 10 1.3 - 1.1 2.25 15 3.6 - 3.0 8.8 10 1.3 - 1.1 2.25 15 3.6 - 5.0 0.88 10 1.3 - 1.1 2.25 15 3.6 - 5.0 - 5.0 - 5.0 10 1.3 - 1.1 2.25 15 3.6 - 3.0 8.8 10 1.3 - 1.1 2.25 15 3.6 - 3.0 - 8.8 10 1.3 - 1.1 2.25 15 3.6 - 3.0 - 3.0 - 8.8 10 1.3 - 1.1 2.25 15 3.6 - 3.0 - 3.0 - 8.8 10 1.3 - 1.1 2.25 15 3.6 - 3.0 8.8 10 1.3 - 1.1 2.25 15 3.6 - 3.0 8.8 10 1.3 - 1.1 2.25 10 - 0.0001 10 - 0.0001 15 - 20 - 0.005 10 - 10 - 0.010 15 - 20 - 0.005 17 4.50 17 5.0 0.015 17 5.0 0.015 17 (5.5 µA/kHz uts, all	"O" Level VOL 5.0 — 0.05 — 0 0.05 "1" Level VOH 5.0 4.95 — 0 0.05 "1" Level VOH 5.0 4.95 — 0 0.05 "1" Level VIL 5.0 — 4.95 5.0 — "0" Level VIL 5.0 — 1.5 — 2.25 1.5 — "1" Level VIL 5.0 — 1.5 — 2.25 1.5 — "1" Level VIH 5.0 — 1.5 — 2.25 1.5 — "1" Level VIH 5.0 3.5 — 3.5 2.75 — — 1.5 — 2.25 1.5 — 3.0 — 4.50 3.0 — 4.50 3.0 — 4.50 3.0 — 4.50 3.0 — 4.50 3.0 — 4.50 3.0 —	"O" Level VOL 5.0 - 0.05 - 0 0	"O" Level VOL 5.0 - 0.05 - 0 0.05 - 0.05 - 0.05 10 - 0.05 - 0 0.05 - 0.05 - 0.05

^{*}T_{IOW} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
=Noise immunity specified for worst-case input combination.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in} \text{ or } V_{out})$ < VDD.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD).

Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc 2.0 Vdc min @ V_{DD} = 10 Vdc 2.5 Vdc min @ V_{DD} = 15 Vdc

[†]To calculate total supply current at loads other than 50 pF: $|\tau(C_L)| = |\tau(50 \text{ pF}) + 8 \times 10^{-3} (C_L - 50) \text{ V}_{DD} \text{f}$ where: $|\tau|$ is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency. *The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS* (CL = 50 pF, TA = 25°C)

Characteristic		Symbol	VDD	Min	Тур	Max	Unit
Output Rise Time	mild	TTLH	Vete hill	Sympol		Districtions	ns
t _{TLH} = (3.0 ns/pF) C _L + 30 ns		0.05	5.0	Jov.	100	200	etho V sugar
tTLH = (1.5 ns/pF) CL + 15 ns		80.0	10	- 20	50	100	ray av
tTLH = (1.1 ns/pF) CL + 10 ns		80.0	15	-	40	80	10.
Output Fall Time	80.0	†THL	08 08	HOV	Seve J. Op.		ns
tTHL = (1.5 ns/pF) CL + 25 ns			5.0	- nu	100	200	100 - aV
t _{THL} = (0.75 ns/pF) C _L + 12.5 ns			10	-	50	100	
t _{THL} = (0.55 ns/pF) C _L + 9.5 ns		-	15	7.0	40	80	anestoV tue
Propagation Delay Time		tPLH.	5.0			raby 8.0 se	a ns
Sum in to Sum Out		tPHL	- 01				0.8 - gV)
tpLH, tpHL = (1.7 ns/pF) CL + 620 ns		0.6	5.0	-	705	1410	IVO - III
tpLH, tpHL = (0.66 ns/pF) CL + 217 ns			10	HIV	250	500	1
tpLH, tpHL = (0.5 ns/pF) CL + 155 ns			15		180	360	(Vo = 0.5)
Sum in to Sum Out (Logic Mode)	7:0	tPLH,	10 2.0			(obV 0.8 vi	0.1 ns//
tPLH, tPHL = (1.7 ns/pF) CL + 520 ns		tPHL	5.0	- 1	605	1210	(Vo - 1.5)
tpLH, tpHL = (0.66 ns/pF) CL + 182 ns			10	Bot	215	430	eviso pour
tPLH, tPHL = (0.5 ns/pF) CL + 155 ns			15		180	360	IVON 2
Sum in to A = B 88.0-	18.0-	tPLH.	0.0 0.6			(utsV)	ns
tpLH, tpHL = (1.7 ns/pF) CL + 870 ns		tPHL	5.0	-	955	1910	1VOH - 9.
tPLH, tPHL = (0.66 ns/pF) CL + 297 ns		- 1	10	- 4	330	660	ET - HOVI
tpLH, tpHL = (0.5 ns/pF) CL + 220 ns			a.0 15 0.8	1 701	245	490	10 = 10VL
Sum In to P or G	1.3	tPLH,	0.1 01			(sbV	ns//
tPLH, tPHL = (1.7 ns/pF) CL + 400 ns	3,6	tPHL	5.0	-	485	970	IVOL * 1.
tpLH, tpHL = (0.66 ns/pF) CL + 147 ns			10	Tigil	180	360	swind mare
tpLH, tpHL = (0.5 ns/pF) CL + 105 ns		- 1	15 0		130	260	Cynst = 2
Sum In to C _{n+4} and a second second	-0.44	tPLH	5.0 -0.5			(abV)	ns
tpLH, tpHL = (1.7 ns/pF) CL + 530 ns		- 11	5.0	-	615	1230	P - HOV
tplH, tpHL = (0.66 ns/pF) CL + 187 ns		- 1.1	E- 10 at	- 1	220	440	ET = HOVE
tpLH, tpHL = (0.5 ns/pF) CL + 135 ns	0.44		15	- Jul	160	360	(Var. = 0.)
Carry In to Sum Out	1.3	tPLH,	0.7 101			Vdc)	ns
tpLH, tpHL = (1.7 ns/pF) CL + 295 ns		tPHL	5.0	-	380	760	Lin Jovi
tpLH, tpHL = (0.66 ns/pF) CL + 112 ns		1.01	10	To I	145	290	Destroy Ditte
tpLH, tpHL = (0.5 ns/pF) CL + 80 ns		504	15	- 6/4	105	210	
Carry in to Cn+4		tPLH,		- GI		-	ns
tpLH, tpHL = (1.7 ns/pF) CL + 220 ns		tPHL	5.0	-0.0	305	610	10 = o(V)
tpLH, tpHL = (0.66 ns/pF) CL + 87 ns		-	10	-	120	240	-
tpLH, tpHL = (0.5 ns/pF) CL + 60 ns		0.8	15	. (GO	85	170	uiescent Cur

^{*} The formulae given are for the typical characteristics only.

AC TEST SETUP REFERENCE TABLE

- 08	AC PA	ATHS	DC DATA	INPUTS		FIG. 3	
TEST	INPUTS	OUTPUTS	TO V _{SS}	TO V _{DD}	MODE	WAVEFORM	Supply Synamic
Sum _{in} to Sum _{out} Delay Time	ÃO	Any F	Remaining A's	All B's	Add	#1	Per Packs Cy = 50 c
Sum _{in} to P Delay Time	ĀO	P	Remaining A's	All B's	Add	#1	we gowifue
Sum _{in} to G Delay Time	BO	G	All Ā's Cn	Remaining B's	Add	10 1/41 0° 85	1 + Frigin
Sum _{in} to C _{n+4} Delay Time	ВO	C _{n+y}	All A's	Remaining B's	Add	#2 1016	prismi issio
C _n to Sum _{out} Delay Time	Cn	Any F	All A's	All B's	Add	#1	
C _n to C _{n+4} Delay Time	c _n	C _{n+4}	All Ā's	All B's	Add	+ (3q #1)+(=(TT(C)
Sum _{in} to A = B Delay Time	ĀO	A = B	All B's Remaining A's	C _n	Sub	#2	umsot en
Sum _{in} to Sum _{out} Delay Time (Logic Mode)	Bo	Any F	All A's	M	Exclusive OR	#2	pedano



FIGURE 2 - TYPICAL SINK CURRENT TEST CIRCUIT

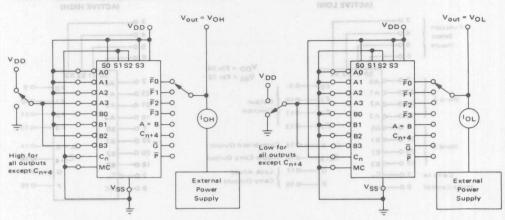
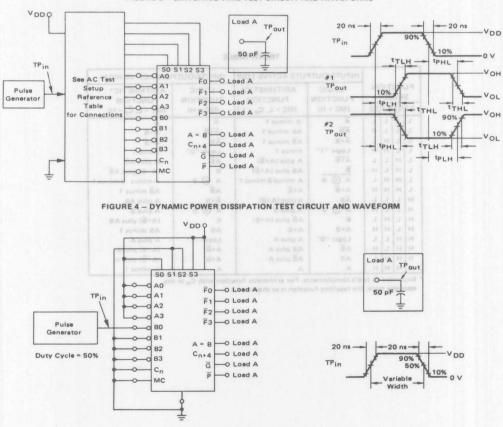
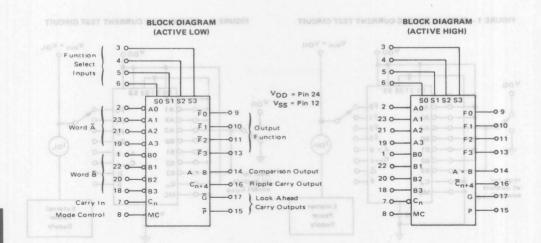


FIGURE 3 - SWITCHING TIME TEST CIRCUIT AND WAVEFORMS







				INPUTS/OUTP	UTS ACTIVE LOW	INPUTS/OUT	TPUTS ACTIVE HIGH		
S	EL	EC	Т	LOGIC FUNCTION	ARITHMETIC* FUNCTION	LOGIC FUNCTION	ARITHMETIC*		
\$3	S2	S1	SO	(MC = H)	$(MC = L, C_n = L)$	(MC = H)	$(MC = L, \overline{C}_n = H)$		
L	L	L	L	Ā	A minus 1	Ā	A		
L	L	L	Н	AB	AB minus 1	A+B	A+B		
L	L	н	L	Ā+B	AB minus 1	ĀB	A+B		
L	L	Н	H	Logic "1"	minus 1	Logic "O"	minus 1		
L	н	L	L	A+B	A plus (A+B)	AB	A plus AB		
L	н	L	н	B	AB plus (A+B)	В	(A+B) plus AB		
L	н	н	L	A ⊕ B	A minus B minus 1	A ① B	A minus B minus 1		
L	н	н	н	A+B	A+B	AB	AB minus 1		
н	L	L	L	ĀB	A plus (A+B)	Ä+B	A plus AB		
н	L	L	н	A ⊕ B	A plus B	A + B	A plus B		
н	L	н	L	В	AB plus (A+B)	В	(A+B) plus AB		
н	L	н	н	A+B	A+B	AB	AB minus 1		
н	н	L	L	Logic "0"	A plus A	Logic "1"	A plus A		
н	н	L	н	AB	AB plus A	A+B	(A+B) plus A		
н	н	н	L	AB	AB plus A	A+B	(A+B) plus A		
н	н	н	н	A	A	A	A minus 1		



LOOK-AHEAD CARRY BLOCK

The MC14582B is a CMOS look-ahead carry generator capable of anticipating a carry across four binary adders or groups of adders. The device is cascadable to perform full look-ahead across n-bit adders. Carry, generate-carry, and propagate-carry functions are provided as enumerated in the pin designation table shown below.

- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- High Speed Operation 140 ns typical @ V_{DD} = 10 Vdc (from Data-in to Carry-out)
- Expandable to any Number of Bits
- Noise Immunity = 45% of VDD typical
- All Buffered Outputs
- Low Power Dissipation
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-Power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range

MAXIMUM RATINGS (Voltages referenced to VSS)

Rating	Symbol	Value	Unit
DC Supply Voltage	VDD	-0.5 to +18	Vdc
Input Voltage, All Inputs	Vin	-0.5 to V _{DD} + 0.5	Vdc
DC Current Drain per Pin	04 1 -	10	mAdc
Operating Temperature Range AL Device CL/CP Device	TA	-55 to +125 -40 to +85	°C
Storage Temperature Range	T _{stg}	-65 to +150	°С

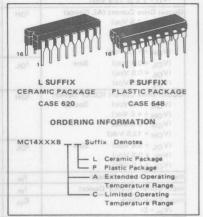
PIN DESIGNATIONS

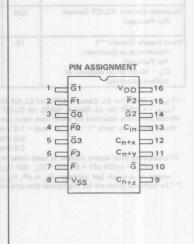
DESIGNATION	PIN NO's	FUNCTION
G0,G1,G2,G3	3,1,14,5	Active-Low Carry-Generate Inputs
P0,P1,P2,P3	4,2,15,6	Active-Low Carry-Propagate Inputs
beas riCn see n	13	Carry Input
C _{n+x} , C _{n+y} C _{n+z}	12,11,9	Carry Outputs
G	10	Active-Low Group Carry-Generate Output
lavel aga Pov orgal a	5 10 0 7 cm	Active-Low Group Carry-Propagate Output

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

LOOK-AHEAD CARRY BLOCK







METARROR ELECTRICAL CHARACTERISTICS

	- 1	VDD	Tio	w*		25°C		Th	igh °	
Characteristic	Symbol	Vdc	Min	Max	Min	Тур	Max	Min	Max	Unit
Output Voltage "0" Level	VOL	5.0	-	0.05	-	0	0.05	-	0.05	Vdc
Vin VDD or 0		10	-	0.05		0	0.05	-	0.05	
12M 20M3	41	15	-	0.05	OJE Y	0 0	0.05	LOOK	0.05	
"1" Level	VOH	5.0	4.95	_	4.95	5.0	_	4.95	_	Vdc
V:a : 0 or Vnn		10	9.95	YOTETSI	9.95	10	IL SOMO	9.95	te Me 14B	T
IN-POWER COMPLEMENTARY MOS	0.0	15	14.95	- 100 TO 100	14.95	15	und-man	14.95	s omissi	nimer.
nput Voltage# "0" Level	VIL		is tid-n	EUUUU II	nne sino	U.S. com	neg of a	dala nan	levice is	Vdc
(V _O = 4.5 or 0.5 Vdc)	- IL	5.0		1.5	BLBS-SIDO	2.25	1.5	OBDEDES:	1.5	-
(V _O = 9.0 or 1.0 Vdc)		10	ong the a	3.0	A.J.100-101	4.50	3.0	penerate	3.0	ders
(V _O = 13.5 or 1.5 Vdc)	. 1	15	.WO	4.0	e nicht n	6.75	4.0	ni betere	4.0	pelaiv
"1" Level	VIH	15	-	4.0		0.75	7.0		4.0	-
(Vo = 0.5 or 4.5 Vdc)	VIH		0.5			0.75		0.5		V-I-
(V _O = 1.0 or 9.0 Vdc)	1	5.0	3.5	56V	3.5	2.75	S,O RAA	3.5	inescent C	Vdc
	-	10	7.0	= 10 Vd	7.0	5.50	091 - n	7.0	gh Speed	H O
(V _O = 1.5 or 13.5 Vdc)		. 15	11.0		11.0	8.25	Service S	11.0	(from Da	
Output Drive Current (AL Device)	ІОН					swift by		VISIO OF	aldshasos	mAde
(V _{OH} = 2.5 Vdc) Source	. 1	5.0	-1.2	-	-1.0	-1.7	V To X	-0.7	oise (mm	1/1 -60
(V _{OH} = 4.6 Vdc)	000	5.0	-0.64	-	-0.51	-0.88	A 10 00 0	-0.36		A 48
(V _{OH} = 9.5 Vdc)	500	10	-1.6	-	-1.3	-2.25	-	-0.9	Bufferer	
(V _{OH} = 13.5 Vdc)	To Lar	15	-4.2	-	-3.4	-8.8	_ no	-2.4	JANKOJ MI	7 6
(VOI = 0.4 Vdc) Sink	IOL	5.0	0.64	-	0.51	0.88	ign <u>i</u> liA	0.36	10017 300	mAde
(V _{OL} = 0.5 Vdc)	0.	10	1.6	-	1.3	2.25	0.8 = 0	0.9	loV_viga	0 30
(VOL = 1.5 Vdc)		15	4.2	One Lo	3.4	8.8	wo Low	2.4	to alded	0 0
Output Drive Current (CL/CP Device)	ТОН		egmat t	ne Hate	1000-20	OJ JIN	092 F 10	160J JT	COLUCY 1	mAd
(VOH = 2.5 Vdc) Source	·OH	5.0	-1.0		-0.8	-1.7		-0.6	ire Eanos	16
(V _{OH} = 4.6 Vdc)		5.0	-0.52	_	-0.44	-0.88	_	-0.36	_	
(V _{OH} = 9.5 Vdc)		10	-1.3	_	-1.1	-2.25	_	-0.9		
(V _{OH} = 13.5 Vdc)		15	-3.6		-3.0	-8.8	nater regi	-2.4	RATIN	MUNICIPAL
(V _{OL} = 0.4 Vdc) Sink	(B7,338)	5.0	0.52	UISV	0.44	0.88		0.36		0 -
	OL	10	1.3	01 0.0-	1.1	2.25		0.36	epsilo	mAd
(V _{OL} = 0.5 Vdc)				-		and the second second	-			-
(V _{OL} = 1.5 Vdc)		15	3.6	an ar sy	3.0	8.8	-	2.4	gal#IA s	scioV
nput Current (AL Device)	lin	15	-	± 0.1	- 1	±0.00001	± 0.1	- 107	± 1.0	μAde
nput Current (CL/CP Device)	lin	15	126 -	± 0.3	-17	±0.00001	±0.3	- sgmaPl	±1.0	μAde
nput Capacitance	Cin	-	- 38	01.95	-	5.0	7.5	JO-	-	pF
$(V_{in} = 0)$			180	ot 88-				9000	B sources	maT =
luiescent Current (AL Device)	IDD	5.0		5.0	018.	0.005	5.0	-	150	μAd
(Per Package)	טטי	10	-	10		0.005	10		300	MAG
		15		20		0.010	20	_	600	
V C (C) (CD D)			-			-				
Quiescent Current (CL/CP Device)	IDD	5.0	-	20	-	0.005	20	-	150	μAd
(Per Package)		10	-	40	-	0.010	40	TALIFIE	300	
		15	-	80	_	0.015	80	10000	600	
otal Supply Current**†	IT	5.0			IT = (1.4 μA/kHz	If + IDD			μAd
(Dynamic plus Quiescent,		10				2.8 μA/kHz				
Per Package)		15				4.3 μA/kHz	If + IDD	G3 + (P3		1
(CL = 50 pF on all outputs, all								P3 e 172 o		
buffers switching)										

^{*}Tlow = -55°C for AL Device, -40°C for CL/CP Device.
Thigh = +125°C for AL Device, +85°C for CL/CP Device.
=Noise immunity specified for worst-case input combination.

This device contains circuitry to protect This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and Vout be constrained to the range VSS < (Vin or Vout) < VDD.

Unused inputs must always be tied to an

appropriate logic voltage level (e.g., either VSS or VDD).

Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc

^{2.0} Vdc min @ VDD = 10 Vdc 2.0 Vdc min @ V_{DD} = 10 Vdc 2.5 Vdc min @ V_{DD} = 15 Vdc

^{2.5} Vdc min @ V_{DD} = 15 Vdc †To calculate total supply current at loads other than 50 pF: $I_T(C_L) = I_T(50 \, \text{pF}) + 5 \times 10^{-3} \, (C_L - 50) \, V_{DD}$ where: I_T is in μ A (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency. **The formulas given are for the typical characteristics only at 25°C.

Characteristic	Symbol	VDD	Min	Тур	Max	Unit
Output Rise Time	tTLH					ns
$t_{T_1 H} = (3.0 \text{ ns/pF}) C_1 + 30 \text{ ns}$		5.0	-	100	200	
tTLH = (1.5 ns/pF) CL + 15 ns		10	-	50	100	
t _{TLH} = (1.1 ns/pF) C _L + 10 ns		15	-	40	80	
Output Fall Time	tTHL					ns
tTHL = (1.5 ns/pF) CL + 25 ns	Tun V	5.0	- 1	100	200	
t _{THL} = (0.75 ns/pF) C _L + 12.5 ns	7	10	W. 5 F-0-	50	100	
t _{THL} = (0.55 ns/pF) C _L + 9.5 ns	-	15	00 0-0-	40	80	
Propagation Delay Time	tPLH.	0-x+n2				ns
tPLH tPHL = (1.7 ns/pF) CL + 260 ns	tPHL	Clock to Q	20.0-0-	345	690	
tPLH, tPHL = (0.66 ns/pF) CL + 107 ns	-	10	10 10-0	140	280	
tPLH, tPHL = (0.5 ns/pF) CL + 85 ns		15	09 0-0-	110	220	

^{*} The formulae given are for the typical characteristics only.

FIGURE 1 – DYNAMIC POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

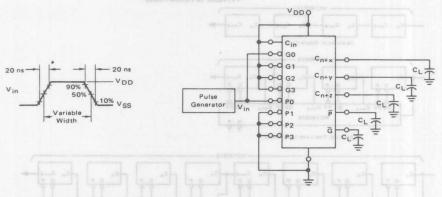
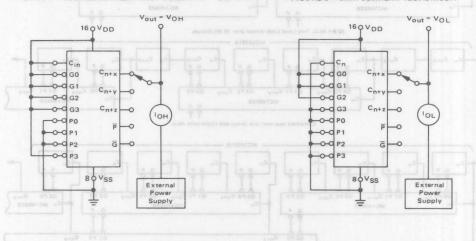
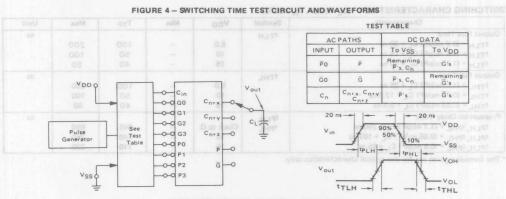
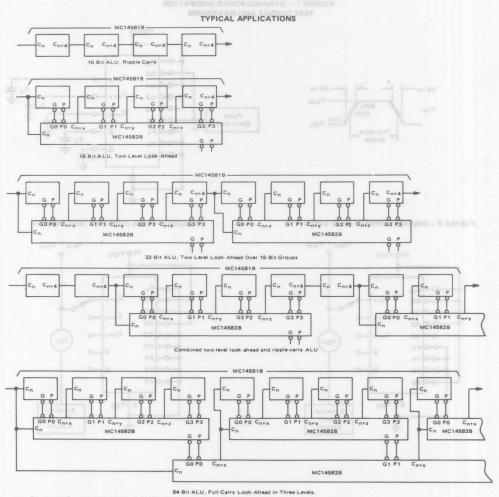


FIGURE 2 - SOURCE CURRENT TEST CIRCUIT

FIGURE 3 - SINK CURRENT TEST CIRCUIT







A and B inputs and F outputs are not shown (MC14581B).



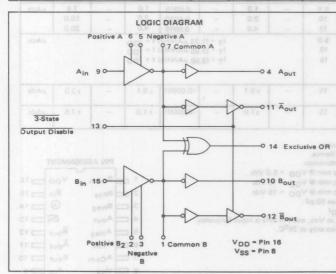
DUAL SCHMITT TRIGGER

The MC14583B is a dual Schmitt trigger constructed with complementary P-channel and N-channel MOS devices on a monolithic silicon substrate. Each Schmitt trigger is functionally independent except for a common 3-state input and an internally-connected Exclusive OR output for use in line receiver applications. Trigger levels are adjustable through the positive, negative, and common terminals with the use of external resistors. Applications include the speed-up of a slow waveform edge in interface receivers, level detectors, etc.

- Quiescent Current = 0.5 nA/package typical @ 5 Vdc
- Schmitt Trigger Input Noise Immunity = 60% of VDD Typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Single Supply Operation
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range
- Resistor Adjustable Trigger Levels

MAXIMUM RATINGS (Voltages referenced to Vss)

Rating	Symbol	Value	Unit
DC Supply Voltage	V _{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	Vin	-0.5 to V _{DD} + 0.5	Vdc
DC Current Drain per Pin	1 -	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	TA	-55 to +125 -40 to +85	°C
Storage Temperature Range	T _{stg}	-65 to +150	°C



MC14583B

CMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

DUAL SCHMITT TRIGGER



L SUFFIX
CERAMIC PACKAGE

P SUFFIX
PLASTIC PACKAGE

NC14583B

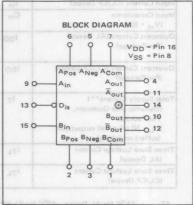
CASE 620

CASE 648

ORDERING INFORMATION

MC14XXXB Suffix Denotes

L Ceramic Package
P Plastic Package
A Extended Operating
Temperature Range
C Limited Operating



du l	NPUT:	S	Deill (20	OUTPUTS						
Α	В	Dis	Aout	Aout	B _{out}	Bout	①			
0	0	0	0	R	0	R	0			
0	0	1	0	1.1.	0	100	0			
0	1	0	0	R	. 1	R	1			
0	1	1	0	1	1	0	1			
1	0	0	of the	R	0	R	1			
1	0	- 1	1	0	0	1	1			
1	1	0	1	R	1	R	0			
1	1	1	1	0	1	0	0			

ELECTRICAL CHARACTERISTICS (R1 = R2 = ∞)

		VDD	Tic	ow*		25°C		Th	igh*	100
Characteristic	Symbol	Vdc	Min	Max	Min	Тур	Max	Min	Max	Unit
Output Voltage "0" Level	VOL	5.0	-	0.05	-	0	0.05	-	0.05	Vdc
V _{in} = V _{DD} or 0		10	-	0.05	-	0	0.05	-	0.05	
		15	-	0.05	-	0	0.05	-	0.05	
"1" Level	VOH	5.0	4.95	- 8	4.95	5.0	452 JA	4.95	_	Vdd
Vin = 0 or VDD	On	10	9.95	-	9.95	10		9.95	_	
W POWER COMPLEMENTARY MOS	DUE	15	14.95	bsackata	14.95	15	a deal S	14.95	tie MC14	10
Input Voltage# A and B "0" Level	VIL	ai	milenen	E 00 20	liveb 20	Vi lennark	and N-	channol	I yestine	Vdd
(V _O = 4.5 or 0.5 Vdc)		5.0	decende	1.5	donet a	2.25	1.5	sta -Ead	1.5	silie
(VO = 9.0 or 1.0 Vdc)		10	R fure suin	3.0	esint or	4.50	3.0	montano:	3.0	oxs
(V _O = 13.5 or 1.5 Vdc)		15	wel Tappol	4.0	mitoTio 3	6.75	4.0	el fluite	4.0	deuta
"1" Level	VIH	10	mierrain e	commos	tone suit	noon sulti	the per	Brownels i	distantib	916
(V _O = 0.5 or 4.5 Vdc)		5.0	3.5	in sōulse	3.5	2.75	sub-Tu bea	3.5	neu-Torit	Vdc
(V _O = 1.0 or 9.0 Vdc)	5500	10	7.0	teb Teve	7.0	5.50	i ni agb	7.0	ew Water	to.
(VO = 1.5 or 13.5 Vdc)	E 200	15	11.0	100 (9/0	11.0	8.25	er ser series	11.0	PAN MORE	10
Output Drive Current (AL Device)	ГОН									mAdo
(VOH = 2.5 Vdc) Source	011	5.0	-1.2	5 Vdc	-1.0	-1.7	An_3.0 :	-0.7	Insperio	0 0
(VOH = 4.6 Vdc)		5.0	-0.25	V S	-0.2	-0.36	aldVi na	-0.14	T affords	
(V _{OH} = 9.5 Vdc)		10	-0.62	an	-0.5	-0.9	DELICATI STR	-0.35	-	
(V _{OH} = 13.5 Vdc)	1000	15	-1.8	-	-1.5	-3.5	and HA n	0 01,108	iode_Pro	0 0
(Va. = 0.4 Vda) Sink	loL	5.0	0.64	-	0.51	0.88	7.E = spr	0.36	oV vl agu	mAdo
(V _{OL} = 0.5 Vdc)	.OL	10	1.6	_	1.3	2.25	A SAN SAN SAN SAN SAN SAN SAN SAN SAN SA	0.9	a a director	
(V _{OL} = 1.5 Vdc)		15	4.2	_	3.4	8.8	ation	2.4	ngle_Sup	8 0
Output Drive Current (CL/CP Device)	ГОН	10.90	W00-W0	900 20	0.1.17	7500000000	Two Le	BOTHER	o aldson	mAd
(VOH = 2.5 Vdc) Source	HO	5.0	-1.0	ts P-orts	-0.8	-1.7	wT-so b	-0.6	volerario	1
(V _{OH} = 4.6 Vdc)		5.0	-0.2	1000	-0.16	-0.36		-0.12		
(V _{OH} = 9.5 Vdc)		10	-0.5		-0.4	-0.9		-0.12	STREET, STATE	
(V _{OH} = 13.5 Vdc)		15	-1.4		-1.2	-3.5	тарділ Т і	-1.0	esistor A	8 9
(VOL = 0.4 Vdc) Sink	IOL	5.0	0.52		0.44	0.88		0.36		mAde
(VOL = 0.5 Vdc)	OL	10	1.3		1.1	2.25	min same	0.9	MITARIN	
(VOL = 1.5 Vdc)		15	3.6	1.0-	3.0	8.8	THE STATE OF	2.4	art esserin	A. O. L.
Input Current (AL Device)	I.	15	5.0	± 0.1	1 1000011	±0.00001	±0.1	4.7	±1.0	μAdo
Input Current (CL/CP Device)	lin	1755-17	911	± 0.1	Jav			-	12/12/2017	1000000
	lin	15	8.57 to	1 V. OD. N. O	V.a.	±0.00001	± 0.3	- 21	±1.0	μAdd
Input Capacitance	Cin	obein.	-	01 =	-	5.0	7.5	- 1019	199 Tland	pF
(V _{in} = 0) AARDARD MOO.M		90	201	nr 22.	1		med Lie	sensit.	autosanni	Lonita
Quiescent Current (AL Device)	IDD	5.0	- 884	0.25	-	0.0005	0.25	10 -	7.5	μAdd
(Per Package)		10	021	0.50	17 - 7	0.0010	0.50	-	15.0	T and
V _{9S} = Pin 6		15	-	1.00	23.	0.0015	1.00	7562.000	30.0	100
Quiescent Current (CL/CP Device)	1DD	5.0	-	1.0		0.0005	1.0	-	7.5	μAde
(Per Package)		10	-	2.0	-	0.0010	2.0	-	15.0	
700° MA	9	15	-	4.0	-	0.0015	4.0	-	30.0	
Total Supply Current**†	IT	5.0			IT = (1	.33 µA/kHz) f + 100	A 690120	4	μAde
(Dynamic plus Quiescent,	(23)	10				2.65 µA/kHz				
Per Package)		15				.98 µA/kHz				
(CL = 50 pF on all outputs, all	16		Agus I		, ,,	2	-00			
buffers switching)			31/0							
Three-State Leakage Current	ITL	15	-	± 0.1	-	+0.00001	± 0.1	_	±3.0	μAd
(AL Device)	1.	-			10 1	4	2.0.1		10.0	,di
Three-State Leakage Current	ITL	15	1007 1	±1.0		+0.00001	± 1.0	_	± 7.5	μAdo
(CL/CP Device)	.IL	10		11.0		0.00001	21.0		27.0	MMO

*Tlow = -55°C for AL Device, -40°C for CL/CP Device.

Thigh = +125°C for AL Device, +85°C for CL/CP Device.

#Noise immunity specified for worst-case input combination.

Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc

2.0 Vdc min @ V_{DD} = 10 Vdc

2.5 Vdc min @ V_{DD} = 15 Vdc

*To calculate total supply current at loads other than 50 pF:

IT(CL) = IT(50 pF) + 5 x 10-3 (CL -50) V_{DD} where: IT is in µA (per package), CL in pF, V_{DD} in Vdc, and f in kHz is input frequency.

*The formulas given are for the typical characteristics only at 25°C.



3

SWITCHING CHARACTERISTICS* (C1 = 50 pF, TA = 25°C)

Characteristic	Symbol	VDD	Min	Тур	Max	Unit
Output Rise Time tTLH = (3.0 ns/pF) CL + 30 ns	^t TLH	5.0		180	360	ns
		10		90	180	do,
t _{TLH} = (1.5 ns/pF) C _L + 15 ns		C)	_			9
tTLH = (1.1 ns/pF) CL + 10 ns		15		65	130	
Output Fall Time	THL			luck.		ns
tTHL = (1.5 ns/pF) CL + 25 ns		5.0	- 0		200	
t _{THL} = (0.75 ns/pF) C _L + 12.5 ns	пиятио	10	-	50	100	
t _{THL} = (0.55 ns/pF) C _L + 9.5 ns		15		40	80	SSA
Propagation Delay Time	tPLH,	70	-0-7	Age		ns
Ain, Bin to Aout, Bout	*****	in the same of	0-0-0	ein b-	and i	
tpLH, tpHL = (1.7 ns/pF) CL + 565 ns		5.0	-	650	1300	
tpLH, tpHL = (0.66 ns/pF) CL + 197 ns		10	0 7	230	460	-
tpLH, tpHL = (0.5 ns/pF) CL + 125 ns		15	0 ,	150	300	
Ain, Bin to Aout, Bout	tPLH,	Y	L		2440 C	ns
tp_H, tpHL = (1.7 ns/pF) CL + 1015 ns	tPHL	5.0		1100	2200	
tp_H, tpHL = (0.66 ns/pF) CL + 347 ns	1110	10		380	760	
tpLH, tpHL = (0.5 ns/pF) CL + 235 ns		15		260	520	
Ain, Bin to Exclusive OR	tPLH,			-		ns
tpLH, tpHL = (1.7 ns/pF) CL + 665 ns	tPHL	5.0		750	1500	1
tp_H, tpHL = (0.66 ns/pF) CL + 257 ns	PHL	10		280	560	
tp_H, tpHL = (0.5 ns/pF) CL + 145 ns	DIN TEST OF	TANS IN	E 2 - POWE	170	340	
3-State Enable, Disable Delay Time (see figure 5)				1.0	0.0	
	ton,	5.0		225	450	ns
t _{on} , t _{off} = (1.7 ns/pF) C _L + 140 ns	toff	700	- 9		180	
t_{on} , $t_{off} = (0.66 \text{ ns/pF}) C_L + 57 \text{ ns}$		10		90	1	
t_{on} , $t_{off} = (0.5 \text{ ns/pF}) C_L + 30 \text{ ns}$		15	4	55	110	
Positive Threshold Voltage	V _{T+}	5.0	OT-	3.30		Vdc
$(R1, R2 = 5.0 k\Omega)$		10	<u>_</u>	5.70	-	
		15	-	8.20	-	
Negative Threshold Voltage	V _T _	5.0	- 1	1.70	1 -	Vdc
$(R1, R2 = 5.0 \text{ k}\Omega)$		10	-	4.30	7 1 10	General
ngA suo		15	-	6.80	-	
Hysteresis Voltage	VH	5.0	0.85	1.70	3.40	Vdd
$(R1, R2 = 5.0 k\Omega)$		10	0.70	1.40	2.80	
		15	0.70	1.40	2.80	120
Threshold Voltage Variation, A to B	ΔVT	5.0	-6-	0.1	9 - 8 -	Vdc
$(R1, R2 = 5.0 k\Omega)$		10		0.15	1	
	大の大	15	0×2×0	0.20	_	

^{*} The formulae given are for the typical characteristics only.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in} \text{ or } V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).



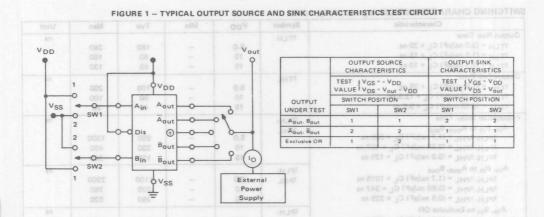


FIGURE 2 - POWER DISSIPATION TEST CIRCUIT AND WAVEFORMS

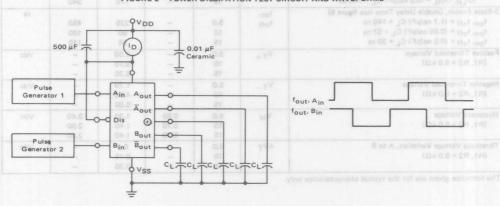
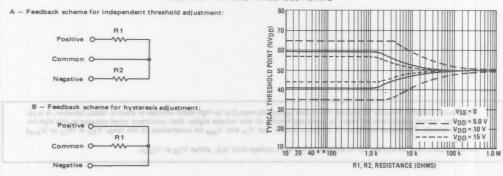
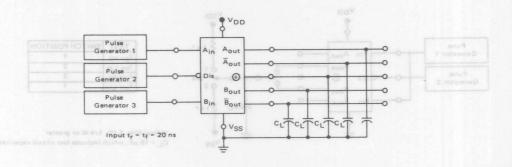
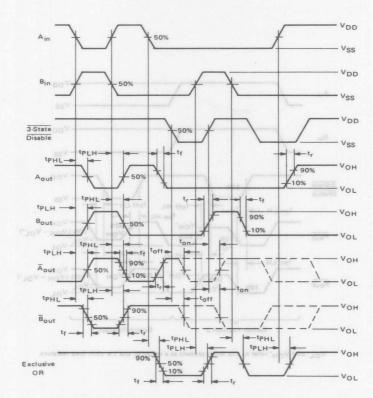


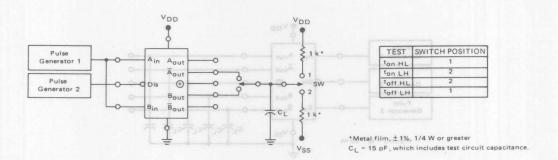
FIGURE 3 - TYPICAL THRESHOLD POINTS



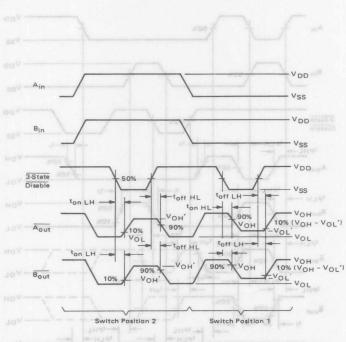




Note: Dashed lines indicate high output resistance.



3





MC14584B

NU14584B

HEX SCHMITT TRIGGER

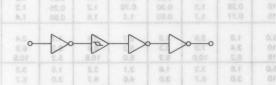
The MC14584B hex Schmitt Trigger is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These devices find primary use where low power dissipation and/or high noise immunity is desired. The MC14584B may be used in place of the MC14069UB hex inverter for enhanced noise immunity or to "square up" slowly changing waveforms.

- Quiescent Current = 0.5 nA typ/pkg @ 5 Vdc
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-Power TTL Loads, One Low-Power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range
- Double Diode Protection on All Inputs
- Can Be Used to Replace MC14069UB
- For Greater Hysterisis, Use MC14106B which is Pin-for-Pin Replacement for CD40106B and MM74C14

MAXIMUM RATINGS (Voltages referenced to VSS)

Rating A.V. G.O.	Symbol	Value	Unit
DC Supply Voltage	VDD	-0.5 to +18	Vdc
Input Voltage, All Inputs	Vin	-0.5 to V _{DD} + 0.5	Vdc
DC Current Drain per Pin	1	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T _A _	-55 to +125 -40 to +85	°C
Storage Temperature Range	T _{stg}	-65 to +150	°C

EQUIVALENT CIRCUIT SCHEMATIC (1/6 OF CIRCUIT SHOWN)



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leqslant (V_{in} \text{ or } V_{out}) \leqslant V_{DD}.$

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD).

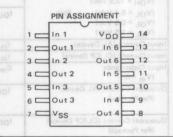
CMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

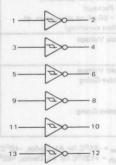
HEX SCHMITT TRIGGER



L SUFFIX CERAMIC PACKAGE CASE 632 P SUFFIX
PLASTIC PACKAGE
CASE 646



LOGIC DIAGRAM



V_{DD} = Pin 14 V_{SS} = Pin 7



ELECTRICAL CHARACTERISTICS

		VDD		w*		25°C			gh *	
Characteristic	Symbol	Vdc	Min	Max	Min	Тур	Max	Min	Max	Unit
utput Voltage "0" Level	VOL	5.0	-	0.05	-	0	0.05	-	0.05	Vdd
Vin VDD or 0	-	10	-	0.05	-	0	0.05	-	0.05	1
		15	-	0.05	-	0	0.05	-	0.05	
"1" Level	VOH	5.0	4.95	_	4.95	5.0	-	4.95	-	Vdc
Vin = 0 or VDD	011	10	9.95	_	9.95	10	_	9.95	_	
		15	14.95	_	14.95	15	1200-000	14.95	_	
put Voltage# "0" Level	VIL			-	74.473.		77.10.0			Vdc
(V _O = 4.5 or 0.5 Vdc)	AIL	5.0	ONLettin	1.5	ence si	2.25	1.5	M BA83	1.5	Vac
(V _O = 9.0 or 1.0 Vdc)		10	innie a r	3.0	nede	4.50	3.0	mH=14.1	3.0	P-ch
(V _O = 13.5 or 1.5 Vdc)		15	Affine by	4.0	outer to	6.75	4.0	200-00-01	4.0	11000
"1" Level	VIH	10	VOI STOR		smrq n	3170	-	78 40 LOU	S CMITTIES	10000
(V _O = 0.5 or 4.5 Vdc)	VIH	5.0	the bes	sap at A	hinumm	2.75	diet hig	IS HOUSE		Vdc
(V _O = 1.0 or 9.0 Vdc)		10	3.5	80890	3.5	5.50	o ni bas	3.5	45848	Vuc
0	-		A SHELLING THE SHELL	up" slos	7.0	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	rummi s	7.0	merine to	391
(V _O = 1.5 or 13.5 Vdc)		15	11.0	_	11.0	8.25	_	11.0	iolar ave	
utput Drive Current (AL Device)	ІОН			1.0						mAdd
(V _{OH} = 2.5 Vdc) Source	Ton.	5.0	-3.0	-obV	-2.4	-4.2	0.4 =	-1.7	mage siu	0
(V _{OH} = 4.6 Vdc)	1000	5.0	-0.64	- of	-0.51	-0.88	= epri	-0.36	V ylogu	0
(V _{OH} = 9.5 Vdc)	100	10	-1.6	-	-1.3	-2.25	-	-0.9	-	
(V _{OH} = 13.5 Vdc)	1 42	15	-4.2	Dade, C	-3.4	-8.8	OWIT (-2.4) SIGRICE	0 0
(VOL = 0.4 Vdc) Sink	IOL	5.0	0.64	is Over 1	0.51	0.88	1901 1	0.36	06 Tamo	mAdd
(V _{OL} = 0.5 Vdc)		10	1.6	-	1.3	2.25	- 9	0.9	Jena me	
(VOL = 1.5 Vdc)		15	4.2	-	3.4	8.8	noison	2.4	Classic and	10
utput Drive Current (CL/CP Device)	ГОН					111111111111111111111111111111111111111	7 1182235		-	mAdd
(VOH = 2.5 Vdc) Source	.On	5.0	-2.5	_	-2.1	-4.2	fi epalqs	-1.7	U e8 ne	0
(V _{OH} = 4.6 Vdc)		5.0	-0.52	g ai-doid	-0.44	-0.88	oll_sipi	-0.36	100-7	0
(V _{OH} = 9.5 Vdc)		10	-1.3	- K	C=1.1	-2.25	04610	-0.9		
(V _{OH} = 13.5 Vdc)	-	15	-3.6		-3.0	-8.8	O LOPIG	-2.4	- Principalities	
011			0.52			0.88	_	0.36		0 -1
(VOL = 0.4 Vdc) Sink	OL	5.0		_	0.44	2.25		1		mAdd
(V _{OL} = 0.5 Vdc)			1.3	-	1.1			0.9	-	
(V _{OL} = 1.5 Vdc)		15	3.6	-	3.0	8.8	-	2.4	-	
put Current (AL Device)	lin	15	-	± 0.1	-	±0.00001	±0.1	-	± 1.0	μAdo
nput Current (CL/CP Device)	1in	15	-	± 0.3	- 12	±0.00001	± 0.3	10VA 20	±1.0	μAdo
put Capacitance	Cin	StreU	-	wov-	latin	5.0	7.5	Filite	-	pF
(Vin = 0) 3 nl			874	er 8.0-	2 ment				ancito's	ulmma
uiescent Current (AL Device)	IDD	5.0	1 - 7	0.25		0.0005	0.25		7.5	μAdo
(Per Package)	.00	10	a.0 + o	0.50	I niv	0.0010	0.50	514	15	SHOVI
		15.	-	1.00		0.0015	1.00	00	30	1015110
uiescent Current (CL/CP Device)	lee	5.0	621	1.0	1 67	0.0005	1.0	- 995671	7.5	μAdo
(Per Package)	IDD	10	85	2.0	-	0.0005	2.0	10	15	μAdd
(rei rackage)	النسسيم	15	081	4.0		0.0015	4.0	sonsi	34	neT ep
		-	-000	4.0	1 100				34	-
otal Supply Current**†	IT	5.0	-			1.8 µA/kHz)				μAdd
(Dynamic plus Quiescent,		10				3.6 µA/kHz)				
Per Package)		15			T = ($5.4 \mu\text{A/kHz}$	f+IDD	EQUIN		1 10 10
(CL = 50 pF on all outputs, all						ROUIT SHO				
buffers switching)			-							
ysteresis Voltage	VH [‡]	5.0	0.27	1.0	0.25	0.55	1.0	0.21	1.0	Vdc
3	1	10	0.36	1.3	0.30	0.70	1.2	0.25	1.2	1
		15	0.77	1.7	0.60	1.1	1.5	0.50	1,4	
hreshold Voltage										
Positive-Going	V _{T+}	5.0	1.9	3.5	1.8	2.7	3.4	1.7	3.4	Vdc
		10	3.4	7.0	3.3	5.3	6.9	3.2	6.9	
8-00		15	5.2	10.6	5.2	8.0	10.5	5.2	10.5	
Negative-Going	V _T -	5.0	1,6	3.3	1.6	2.1	3.2	1.5	3.2	Vdc
	- 1-	10	3.0	6.7	3.0	4.6	6.7	3.0	6.7	V GC
01		15	4.5	9.7	4.6	6.9	9.8			
		10	4.5	9.7	4.6	6.9	9.8	4.7	9.9	

^{*}T_{low} = -55°C for AL Device, -40°C for CL/CP Device.

Thigh = +125°C for AL Device, +85°C for CL/CP Device.

#Noise immunity specified for worst-case input combination. Noise Margin for both "1" and "0" level =

1.0 Vdc min @ V_{DD} = 5.0 Vdc 2.0 Vdc min @ V_{DD} = 10 Vdc 2.5 Vdc min @ V_{DD} = 15 Vdc

†To calculate total supply current at loads other than 50 pF: IT (CL) = IT (50 pF) + 1 \times 10⁻³ (CL -50) VDDf

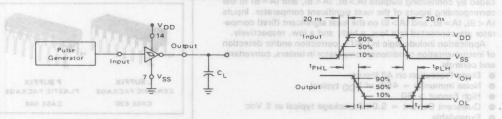
where: I $_{T}$ is in μ A (per package), C $_{L}$ in pF, V $_{DD}$ in Vdc, and f in kHz is input frequency.

**The formulas given are for the typical characteristics only at 25°C. $^{\dagger}V_{H}$ = V_{T+} - V_{T-} (But maximum variation of V_{H} is specified as less than V_{T+} max – V_{T-} min).

SWITCHING CHARACTERISTICS (CL = 50 pF, TA = 25°C)

Characteristic	Symbol	V _{DD} Vdc	Min	Тур	Max	Unit
Output Rise Time	tTLH	5.0 10 15	- - -	100 50 40	200 100 80	ns
Output Fall Time	JHT [‡] constructed ide devices.	5.0 10 15	inude-Comp (OS) enhand	100 50 40	200 100 80	ns M adT noo dily
Propagation Delay Time	tPLH, tPHL	5.0 10 15	i inpl <u>in</u> s (A3, its (A <a, a<br="">A>B), This</a,>	125 50 40	250 100 80	OB O

FIGURE 1 - SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



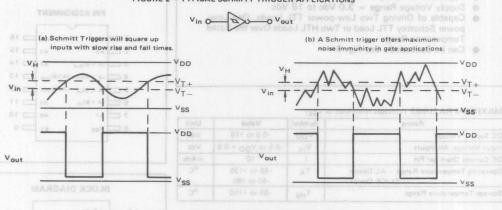
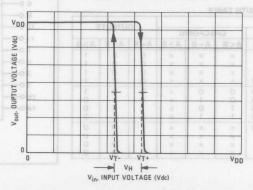


FIGURE 3 - TYPICAL TRANSFER CHARACTERISTICS



4-BIT MAGNITUDE COMPARATOR

The MC14585B 4-Bit Magnitude Comparator is constructed with complementary MOS (CMOS) enhancement mode devices. The circuit has eight comparing inputs (A3, B3, A2, B2, A1, B1, A0, B0), three cascading inputs (A<A, A=B, and A>B), and three outputs (A<B, A=B, and A>B). This device compares two 4-bit words (A and B) and determines whether they are "less than", "equal to", or "greater than" by a high level on the appropriate output. For words greater than 4-bits, units can be cascaded by connecting outputs (A>B), (A<B), and (A=B) to the corresponding inputs of the next significant comparator. Inputs (A<B), (A=B), and (A>B) on the least significant (first) comparator are connected to a low, a high, and a low, respectively.

Application include logic in CPU's, correction and/or detection of instrumentation conditions, comparator in testers, converters, and controls.

- Diode Protection on All Inputs
- Noise Immunity = 45% of V_{DD} typical
- High Fanout > 50
- Quiescent Current = 5.0 nA/package typical at 5 Vdc
- Expandable
- Applicable to Binary or 8421-BCD Code
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Lowpower Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range
- Can be Cascaded See Fig. 3

MAXIMUM RATINGS (Voltages referenced to VSS)

Rating	Symbol	Value	Unit
DC Supply Voltage	VDD	-0.5 to +18	Vdc
Input Voltage, All Inputs	Vin	-0.5 to V _{DD} + 0.5	Vdc
DC Current Drain per Pin	1	100 10	mAdc
Operating Temperature Range — AL Device CL/CP Device	TA	-55 to +125 -40 to +85	°С
Storage Temperature Range	T _{stg}	-65 to +150	°C

TRUTH TABLE

		11	NPUTS				0	LITOLIT	0
	COMP	ARING		CA	SCADIN	NG	10	UTPUT	5
A3, B3	A2, B2	A1, B1	A0, B0	A <b< th=""><th>A=B</th><th>A>B</th><th>A<b< th=""><th>A = B</th><th>A>B</th></b<></th></b<>	A=B	A>B	A <b< th=""><th>A = B</th><th>A>B</th></b<>	A = B	A>B
A3>B3	×	×	×	×	×	×	0	0	1
A3 = B3	A2>B2	×	×	×	×	×	0	0	1
A3 = B3	A2 = B2	A1>B1	×	×	×	×	0	0	1
A3 = B3	A2=B2	A1 = B1	A0>B0	×	×	×	0	0	1
A3 = B3	A2=B2	A1=B1	A0 = B0	0	0	×	0	-0	1
A3 = B3	A2 = B2	A1=B1	A0 = B0	0	1	×	0	1	0
A3 = B3	A2=B2	A1=B1	A0 = B0	1	0	×	1	0	0
A3 = B3	A2=B2	A1 = B1	A0 = B0	1	1	×	1	1	0
A3 = B3	A2=B2	A1 = B1	A0 <b0< td=""><td>×</td><td>×</td><td>×</td><td>1</td><td>0</td><td>0</td></b0<>	×	×	×	1	0	0
A3 = B3	A2=B2	A1 <b1< td=""><td>×</td><td>×</td><td>×</td><td>×</td><td>1</td><td>0</td><td>0</td></b1<>	×	×	×	×	1	0	0
A3 = B3	A2 <b2< td=""><td>×</td><td>×</td><td>×</td><td>×</td><td>×</td><td>1</td><td>0</td><td>0</td></b2<>	×	×	×	×	×	1	0	0
A3 <b3< td=""><td>×</td><td>×</td><td>×</td><td>×</td><td>×</td><td>×</td><td>1</td><td>0</td><td>0</td></b3<>	×	×	×	×	×	×	1	0	0

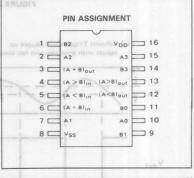
x = Don't Care

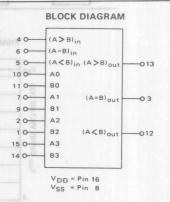
CMOS MSI

(LOW POWER COMPLEMENTARY MOS)

4-BIT MAGNITUDE COMPARATOR







ELECTRICAL CHARACTERISTICS

	RYT	nith	VDD	Tic	w*		25°C	pitairut	perent Thi	gh*	
Characteristic		Symbol	Vdc	Min	Max	Min	Тур	Max	Min	Max	Unit
Output Voltage	"0" Level	VOL	5.0	-	0.05	-	0	0.05	N DO	0.05	Vdc
Vin = VDD or 0	0.8		10	-	0.05	-	0	0.05	1 13 13	0.05	HEIT
0.8	0.5	-	15	-	0.05	-	0	0.05	+ 10 (4)	0.05	HJT
	"1" Level	Vон	5.0	4.95	JHT	4.95	5.0	-	4.95	90/1 /is	Vdc
Vin = 0 or VDD	190	0,,	10	9.95		9.95	10	25 ns	9.95	en 81_11 =	JHT7
100	50	-	15	14.95	-	14.95	15	+ 12,5 ns	14.95	= (Q.75 m	UHTT
Input Voltage#	"0" Level	VIL	1 8					su dig a	To tadis	n #0.01 =	Vdc
(Vo = 4.5 or 0.5 Vdc)			5.0	-	1.5	-	2.25	1.5	97	1.5	10-mu
(VO = 9.0 or 1.0 Vdc)	GEA	-	10	8 -	3.0	-	4.50	3.0	Palan S.	3.0	4391
(V _O = 13.5 or 1.5 Vdc)	180	- 1	15	-	4.0	-	6.75	4.0	10/81 BB.4	4.0	1191
280	"1" Level	VIH	1 3				20%	801 + JO	नव्यक्षा हर	7 " JH9"	HURT
(VO = 0.5 or 4.5 Vdc)			5.0	3.5	-	3.5	2.75	solgyr or	3.5	lavia aslui	Vdc
$(V_0 = 1.0 \text{ or } 9.0 \text{ Vdc})$			10	7.0	_	7.0	5.50	- 44 000	7.0	Our	
(V _O = 1.5 or 13.5 Vdc)			15	11.0	-	11.0	8.25	_	11.0		
Output Drive Current (AL I	Device)	IOH		1	-	11.0	0.00		11.0		mAdc
	Source	·OH	5.0	-3.0	_	-2.4	-4.2		-1.7		1111100
(V _{OH} = 4.6 Vdc)			5.0	-0.64		-0.51	-0.88	_	-0.36		
(V _{OH} = 9.5 Vdc)			10	-1.6	_	-1.3	-2.25	_	-0.9	_	
(V _{OH} = 13.5 Vdc)	1.5		15	-4.2	_	-3.4	-8.8	_	-2.4		1300
	Sink	1	5.0	0.64	_	0.51	0.88	_	0.36	-	mAdc
(V _{OL} = 0.5 Vdc)	SIRK	IOL	10	1.6	-	1.3	2.25	_	0.36		MAGC
$(V_{OL} = 1.5 \text{ Vdc})$			15	4.2		3.4	8.8	_	2.4	_	
			15	4.2	_	3.4	0.0				-
Output Drive Current (CL/C		ЮН		0.5		MOIT	N DISSIP	MIC POWE	AMYO -		mAdc
(V _{OH} = 2.5 Vdc)	source	RE 2 - DY		-2.5	-	-2.1	-4.2	WAVEF	1m1a7a		
(V _{OH} = 4.6 Vdc)			5.0	-0.52	-	-0.44	-0.88	-	-0.36	-	
(V _{OH} = 9.5 Vdc)			. 10	-1.3	-	-1.1	-2.25		-0.9		
(V _{OH} = 13.5 Vdc)			15	-3.6	-	-3.0	-8.8	-	-2.4	Jan 20.0	
OL	Sink	IOL	5.0	0.52		0.44	0.88		0.36	-	mAdc
(V _{OL} = 0.5 Vdc)		ha-al)	10	1.3	-	1.1	2.25	- 4	0.9	-	1.11.5
(V _{OL} = 1.5 Vdc)		-	15	3.6	-	3.0	8.8	-1	2.4	V -	
Input Current (AL Device)	97 U	lin	15	-	± 0.1	-	±0.00001	± 0.1	-	± 1.0	μAdc
Input Current (CL/CP Device	e)	lin	15		± 0.3	1V	±0.00001	± 0.3	7	± 1.0	μAdc
Input Capacitance (Vin = 0)		Cin	- 011		-	- J	5.0	7.5	-		pF
Quiescent Current (AL Devi	ce)	IDD	5.0	-	5.0		0.005	5.0	-	150	μAdc
(Per Package)	aroe %	.00	10	-		V	0.010	10	/	300	
	Name 1		15	_	20	-	0.015	20	- \	600	
Quiescent Current (CL/CP (Device)	Ipp	5.0	-	20	V	0.005	20		150	μAdc
(Per Package)	201	יטטי	10	(A)	40		0.005	40		300	имас
(refrackage)		HJ77	15	_	80	W	0.015	80		600	
Total Supply Current**†		IT	5.0		00	l= = 11	1			800	0.41
(Dynamic plus Quiescen		'T	10				0.6 μΑ/kHz				μAdc
Per Package)	,		15				1.2 µA/kHz			700	
(C ₁ = 50 pF on all outp	ute all	and I have to		111		I (1.8 μA/kHz	I I + IDD			
buffers switching)	115, dil										

 $^{^{\}circ}T_{low}$ = $-55^{\circ}C$ for AL Device, $-40^{\circ}C$ for CL/CP Device. T_{high} = $+125^{\circ}C$ for AL Device, $+85^{\circ}C$ for CL/CP Device. #Noise immunity specified for worst-case input combination.

Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc

2.0 Vdc min @ V_{DD} = 10 Vdc

2.5 Vdc min @ V_{DD} = 15 Vdc

1To calculate total supply current at loads other than 50 pF:

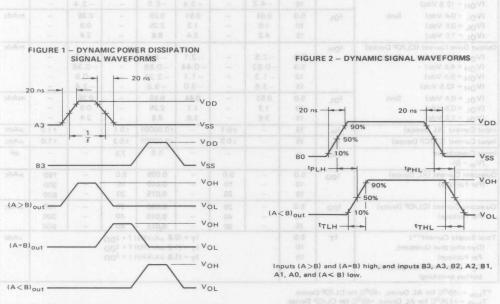
I_T(C_L) = I_T(50 pF) + 1 × 10⁻³ (C_L -50) V_{DD}f

where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.

**The formulas given are for the typical characteristics only at 25°C.

Characteristic	26°C		Symbol	VDD	aV	Min	Тур	Max	Unit
Output Rise Time	RYT .	niM	tTLH	oild si	6V	Symbol		Chargeneralls	ns
tTLH = (3.0 ns/pF) CL + 30 ns				5.0	18	Jov	100	200	
tTLH = (1.5 ns/pF) CL + 15 ns				10	NI I	-	50	100	aV-LV
tTLH = (1.1 ns/pF) CL + 10 ns				15	31	-	40	80	
Output Fall Time	0.8	4.95	tTHL	0 b 1 0	10 1	MOV	hour I may		ns
tTHL = (1.5 ns/pF) CL + 25 ns		8.95		5.0	01	-	100	200	10.0 - m.V
tTHL = (0.75 ns/pF) C1 + 12.5 ns		14.95		10	ar I	_	50	100	
tTHL = (0.55 ns/pF) CL + 9.5 ns				15	-	TuV.	40	80	anerto V. Door
Turn-Off Delay Time	20.0		tPLH,	- 1-0	18			John Cond	ns
tpLH, tpHL = (1.7 ns/pF) CL + 345	ns	1 3 1	tPHL	5.0	110		430	860	0.0 DV)
tPLH, tPHL = (0.66 ns/pF) CL + 147	ns		4.0	10	ar l	_	180	360	ET - DVI
tpLH, tpHL = (0.5 ns/pF) CL + 105	ns	1		15		7,00	130	260	7

^{*} The formulae given are for the typical characteristics only.



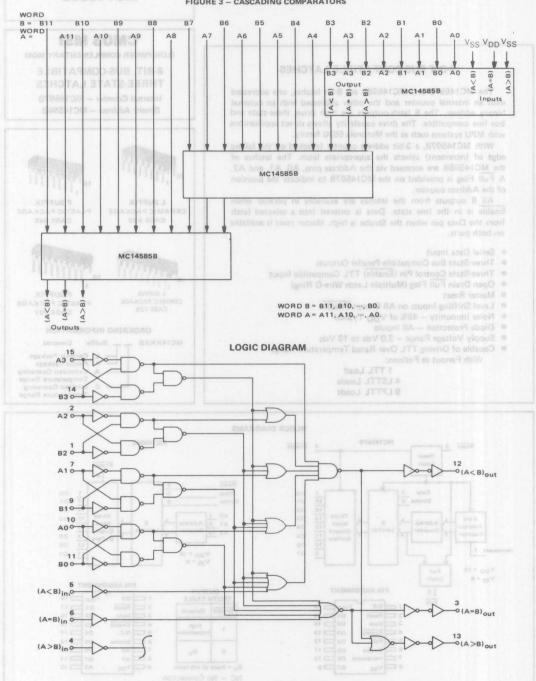
Inputs (A > B) and (A=B) high, and inputs B2, A2, B1, A1, B0, A0 and (A < B) low

f in respect to a system clock.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in} \text{ or } V_{out})$

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD).

FIGURE 3 - CASCADING COMPARATORS



8-BIT BUS-COMPATIBLE LATCHES

The MC14597B and MC14598B are 8-bit latches, one addressed with an internal counter and the other addressed with an external binary address. The 8 latch-outputs are high drive, three-state and bus line compatible. The drive capability allows direct applications with MPU systems such as the Motorola 6800 family.

With MC14597B, a 3-bit address counter (clocked on the falling edge of Increment) selects the appropriate latch. The latches of the MC14598B are accessed via the Address pins, A0, A1, and A2. A $\overline{\text{Full}}$ Flag is provided on the MC14597B to indicate the position of the Address counter.

All 8 outputs from the latches are available in parallel when Enable is in the low state. Data is entered into a selected latch from the Data pin when the Strobe is high. Master reset is available on both parts.

- Serial Data Input
- Three-State Bus Compatible Parallel Outputs
- Three-State Control Pin (Enable) TTL Compatible Input
- Open Drain Full Flag (Multiple Latch Wire-O Ring)
- Master Reset
- Level Shifting Inputs on All Except Enable = 9 0 8 0 W
- Noise Immunity 45% of VDD Typical
- Diode Protection All Inputs
- Supply Voltage Range 3.0 Vdc to 18 Vdc
- Capable of Driving TTL Over Rated Temperature Range
 With Fanout as Follows:

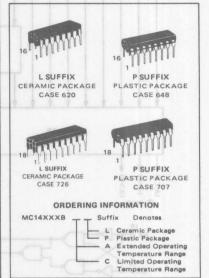
1 TTL Load 4 LSTTL Loads 9 LPTTL Loads

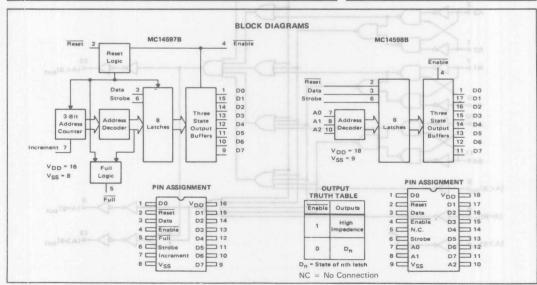
CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

8-BIT, BUS-COMPATIBLE THREE-STATE LATCHES

Internal Counter - MC14597B Binary Address - MC14598B





MAXIMUM RATINGS (Voltage referenced to VSS)

Rating SEGVT NA	Symbol	Value	Unit
DC Supply Voltage	VDD	-0.5 to +18	Vdc
Input Voltage, Enable	Vin	-0.5 to V _{DD} +0.5	Vdc
Input Voltage, All Other Inputs	Vin	-0.5 to V _{DD} +12	Vdc
DC Current Drain per Pin	-1	010	mAdd
Operating Temperature Range — AL Device CL/CP Device	TA	-55 to +125 -40 to +85	°C
Storage Temperature Range	T _{stg}	-65 to +150	°C

protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that Vout be constrained to the range V_{SS} < (V_{out}) < V_{DD}

ELECTRICAL CHARACTERISTICS

		VDD	Tio	w*		25°C		This	gh*	1
Characteristic	Symbol	Vdc	Min	Max	Min	Тур	Max	Min	Max	. Unit
Output Voltage "0" Level	VOL	5.0	1 - 0	0.05	-	0	0.05	MCHBB	0.05	Vdc
Vin = VDD or 0 000	0.	10	- 0	0.05	-	0	0.05	-	0.05	
0 180		15	1 - 8	0.05	-	0	0.05	-	0.05	
085 "1" Level	VOH	5.0	4.95	8 -	4.95	5.0	-	4.95	twores o	Vdc
Vin = 0 or VDD 081	0	10	9.95	- 1	9.95	10	-	9.95	-	
0 140		15	14.95	-	14.95	15	_	14.95	-	
Input Voltage# - Enable "0" Level	VIL								11	Vdc
(V _O = 4.5 or 0.5 Vdc)	12	5.0	- 0	0.8	11427	1.1	0.8	-	0.8	den9
(VO = 9.0 or 1.0 Vdc)		10	- 0	1.6	348	2.2	1.6	-	1.6	
(V _O = 13.5 or 1.5 Vdc)		15	- 8	2.4	_	3.4	2.4	-	2.4	
"1" Level	VIH	200	0	8						Vdc
(V _O = 0.5 or 4.5 Vdc)	·in	5.0	2.0	_	2.0	1.9	_	2.0	_	
(V _O = 1.0 or 9.0 Vdc)		10	6.0		6.0	3.1	_	6.0	_	
(V _O = 1.5 or 13.5 Vdc)		15	10	8 -	10	4.3	- 10	10	DMT me	locen
Input Voltage# - "0" Level	VIL	100	1 5	2						Vdc
Other Inputs	1.	08	8							
(Vo = 4.5 or 0.5 Vdc)		5.0	- 6	1.5	-	2.25	1.5	-	1.5	House
(VO = 9.0 or 1.0 Vdc)	8	10	- 0	3.0		4.50	3.0	-	3.0	
(VO = 13.5 or 1.5 Vdc)		15	- 8	4.0	-	6.75	4.0	-	4.0	
"1" Level	VIH								97	Vdc
(Vo = 0.5 or 4.5 Vdc)	· III	5.0	3.5	a -	3.5	2.75	-	3.5	-	Date
(V _O = 1.0 or 9.0 Vdc)		10	7.0	-	7.0	5.50	-	7.0	-	-
(V _O = 1.5 or 13.5 Vdc)		15	11		11	8.25	-	11	-	
Output Drive Current Source	ГОН	200	0	2				Vine 868	s (MC14)	mAdo
(Full -Sink Only)		100	1 8							
(VOH = 4.6 Vdc)		5.0	-1.0	-	-1.0	-2.0	-	-1.0	-	
(V _{OH} = 9.5 Vdc)		10	1 - 0	2 -	-	-6.0	- (4	4597B on	OMT me	- Innerel
(VOH = 13.5 Vdc)		15	- 7	-	-	-12	- "	-	-	-
(VOI = 0.4 Vdc) Sink	IOL	5.0	1.6	-	1.6	3.2	-	1.6	-	mAdd
(VOL = 0.5 Vdc)	02	10	-	-	-	6.0	_	-	-	miT blo
(VOL = 1.5 Vdc)		15	1 - 0		-	12	-	-	-	-140
Input Current (AL Device)	lin	15	- 1	±0.1	-	±0.00001	±0.1	-	±1.0	μAdo
Input Current (CL/CP Device)	lin	15	-	±0.3	-	±0.00001	±0.3	-	±1.0	μAdo
Three-State Leakage Current	ITL	100	1	3		1		ulan ESG	MC14	μAdo
(AL Device)	ITL	15	1 - 3	±0.1		±0.00001	±0.1	_	±3.0	μησο
(CL/CP Device)		15		±1.0	_	±0.00001	±1.0		±7.5	
Input Capacitance	Cin	-	-	-	-	5.0	7.5	-		pF
(V _{in} = 0)	Cin	S 128			rice poly.	161, 3.0 Ha	ine cyprod	101 516 m	svig astu	norda.
Quiescent Current (AL Device)	IDD	5.0	+-	5.0	-	0.005	5.0	_	150	μAdo
(Per Package)	.00	10	-	10	_	0.010	10	_	300	1
(. c acrago)		15	_	20	_	0.015	20	_	600	
Quiescent Current (CL/CP Device)	IDD	5.0	-	20	-	0.005	20	_	150	μAda
(Per Package)	'DD	10	1	40	-	0.005	40	_	300	μπαι
(re) rackage)		15	1 -	80	_	0.015	80		600	
Tatal Supply Supply Supply at an	1-		-	00		$r = (2.0 \mu \text{A/k})$			000	_
Total Supply Current at an	IT	5.0				$r = (2.0 \mu A/k)$ $r = (4.0 \mu A/k)$				
External Load Capacitance (CL)		10								
of 130 pF		15	1		1-	$T = (6.0 \mu A/k)$	Hzlf + In	D		

^{*}Tlow = -55°C for AL Device, -40°C for CL/CP Device.

Thigh = +125°C for AL Device, +85°C for CL/CP Device.

[#]Noise immunity specified for worst-case input combination. Noise Margin both "1" and "0" level = 1.0 Vdc min @ VDD = 5.0 Vdc

^{2.0} Vdc min @ V_{DD} = 10 Vdc 2.5 Vdc min @ V_{DD} = 15 Vdc

[†]The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS* (TA = 25°C, CL = 130 pF + 1 TTL Load)

	STORY PROTEIN	specifor	singly de	18		H an adv at and my		Rating			
					Symbol		Min	Тур	Max	Unit	
Output Ris	e and Fa	II Time	ad moitu	10	tTLH,	adv ar du	ni ^y 1		Enable	ns	
tTLH,					tTHL	5.0 O-	niV_ 1	100	200 IA		
TLH.					atiAm	10	1-	50	100		
		(0.16 ns/pl				15	-	40	80		
Propagation			Juo V 18	(0)	3	(R+ pt Db-		85/0670 /5 -/	ANALY WALLESAN	ns	
Cashia	n Delay	ut OV > 4		V	tPLH.	5.0		160	320		
Chable	to Outpo	Jt			tPHL	WIND MARKET	978 ^T	100000	DE1253 - 01075 1	igmeT again)	
				-		10		125	250	LAGIOVAN	
	_						-	100	200	L=111111.1.121	
Strobe	to Outpu	Jt .		2500		5.0	-	200	400	ns	
						10	OBY .	100	200		
				gyT	n(N)	15 mil	1987	80	160	EN3	
Strobe	to Full	(MC14597	B only)	0	- 1	5.0	0.0	200	400	perio Vns	
				0	- 1	00.0 10 -	8	100	200 0 10	Vin - Voo	
				0	- 1	80,0 15 -	-	80	160		
Reset to	Output	4.95		9.8	4.95	5.0	p 0-0	175 we 1	350	ns	
		9.95		10	9.95	10		90	180	Vin = 0 or	
				ar I	14.85	15		70	140	and the state of	
ulse Width					1 2000						
Enable	8.0			1.0	twH,	5.0	320	160	'0" Enable "0"	igut Voltage	
Enable					tWL.		7000	120		a.a -nsv)	
				2.2	-WL	10 -	240	80		0.8 = QVI	
				3,4			160		or 1.8 tdc)	(Vo = 13.5	
Strobe						5.0	200	100 svs.	Stor -	ns	
				-B.1	2,0	- 10 03	10000	50		8.0 - 0V)	
				1.5	0.8	- 15	1	40	(5LFV 0.8 no	0.1 - oV1	
Increme	ent (MC1	14597B on	ly)	6.3	10	5.0	200	100	13.5¥de)	a. ns	
						10	100	JIV 50 level	"0" 4	egatio V tuan	
				100	1	15	80	40	- erugi	Other 1	
Reset				2.25	- 1	5.0	300	150	(ab)/ 8.0 v	a. ns	
				4,60	1 - 1	0.8 10 -	160	80	1:0 Vale)	0.8 - OV)	
				6.75		0.A 15 -	100	50	or 1.5-Vdc)	(Vo = 13.6	
Setup Time	е							Level VIM	1 pm		
Data				2.75	t _{su}	5.0	100	50	or 4.5 (446)	2.0 = nsV)	
				6.50	'su	- 10		25		0.1 = 0V)	
				8.25	111	15		20	or 13.6 2 del		
Address	(MC14	598B only)			1	5.0	200	HO 100	_triefruc	ns	
Add: 633	(1110174	JUJU ONIY				10	100	50	Internal		
				-2.0	0.1-	15 01	70	35	± (ab∀)	IVON = 4.5	
Inner	/8404						200	-	_ (sbV	ns	
increme	ent (IVIC)	14597B on	iy/			5.0	400	200		Et = HOVI	
					1.6	10	200	100			
		W-7		0.0	100	15	170	10 85 Anis	- (pbV	(Vol = 0.	
Hold Time									(obV	10 = 30V)	
Data					th	5.0	100	50	_	113	
						10	50	nil 25 (solve	DJA) -	they too turn	
						15	35	20	1 90 (JB)	Bout Current	
Addres	s (MC14	598B only)			5.0	100	50	ekage Surrent	J ere ns	
					- 1	10 -	50	25 (soive	LIAI-		
						15	35	20	1351261		

^{*} The formulae given are for the typical characteristics only.

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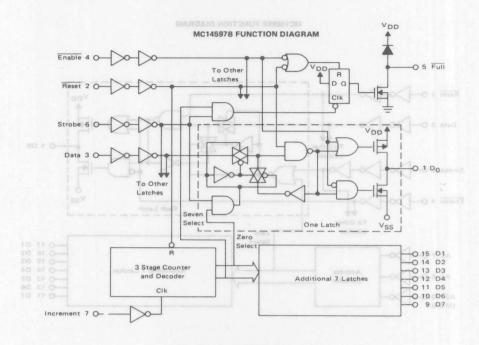
* The formulae given are for the typical characteristics only.

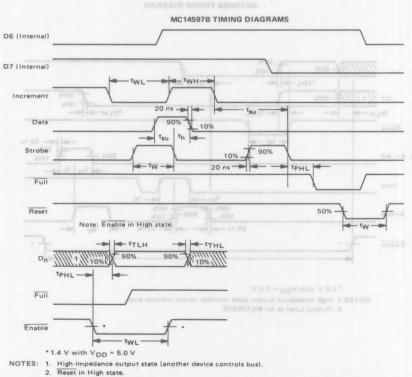
* The formulae given are for the typical characteristics only.

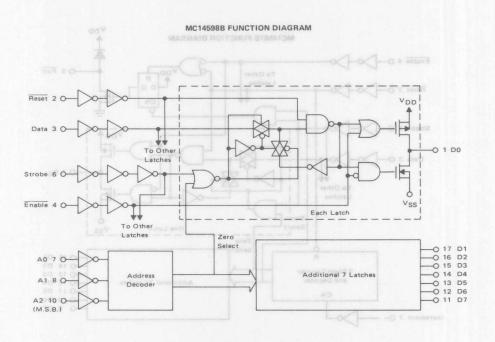
* The formulae given are for the typical characteristics only.

2,5 Vdc min @ Vpp = 15 Vdc

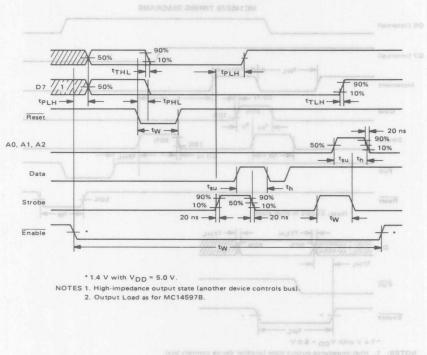
and "0" level = 1.0 Vdc min 9 V00 = 5.0 Vdc











LATCH TRUTH TABLE

Strobe	Reset	Addressed Latch	Other Latches
0	1		
1	1	Data	
X	0	0	0

" = No change in state of latch

X = Don't care

TRUTH TABLE FOR MC14597B

Increment	Enable	Reset	Address Counter	Full
	X	1	Count Up	
	X	1	No Change	
X	SHES	0	Reset to Zero	Set to One
X	0	1	No Change	Set to One
	propriate latch disable is in the		I ADDRESS /	To Zero on Falling Edge of STROBE

Test Load All Outputs RL = 2.5 k 9Y 00V to #CA - valuement sain! . Capable of Driving Two Low Power TTL Load Schottky TTL Load or Two HTL Loads over IV € 11.7 k e. Pin for pin compatible with Fairchild 4724,

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MC14599B

MC14597B=MC14598B

FOR COMPLETE DATA SEE MC14099B

8-BIT ADDRESSABLE LATCHES

The MC14099B and MC14599B are 8-bit addressable latches. Data is entered in serial form when the appropriate latch is addressed (via address pins AO, A1, A2) and write disable is in the low state. Chip enable must be high for writing into MC14599B. For the MC14599B the data pin is a bidirectional data port and for the MC14099B the input is a unidirectional write only port. The Write/Read line controls this port in the MC14599B.

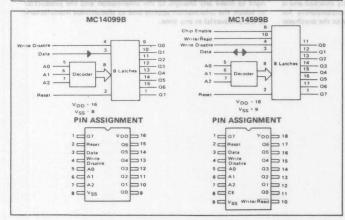
The data is presented in parallel at the output of the eight latches independently of the state of Write Disable, Write/ $\overline{\text{Read}}$ or Chip Enable.

A Master Reset capability is available on both parts.

- Serial Data Input
- Parallel Output
- Low Input Capacitance 5.0 pF typical
- Master Reset
- Noise Immunity 45% of VDD typical
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-Power TTL Loads, One Low-Power Schottky TTL Load or Two HTL Loads over the Rated Temperature Range
- MC14099B pin for pin compatible with CD4099B
- · Pin for pin compatible with Fairchild 4724.

MAXIMUM BATINGS (Voltages referenced to Voc.)

Rating	Symbol	Value	Unit
DC Supply Voltage	V _{DD}	-0 5 to +18	Vdc
Input Voltage, All Inputs	Vin	-0.5 to V _{DD} + 0.5	Vdc
DC Current Drain per Pin	1	10	mAdo
Operating Temperature Range - AL Device CL/CP Device	TA	-55 to +1'25 -40 to +85	°C
Storage Temperature Range	Tstg	-65 to +150	°C

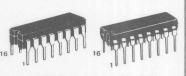


CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

8-BIT ADDRESSABLE LATCH

MC14599B WITH BIDIRECTIONAL PORT



L SUFFIX CERAMIC PACKAGE CASE 620 P SUFFIX
PLASTIC PACKAGE
CASE 648



CERAMIC PACKAGE CASE 726

P SUFFIX PLASTIC PACKAGE CASE 707

ORDERING INFORMATION

MC14XXXB Suffix Denotes

L Ceramic Package
P Plastic Package
A Extended Operating
Temperature Range
C Limited Operating
Temperature Range

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leqslant (V_{in} \text{ or } V_{out}) \leqslant V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD).

Mechanical Data

14-PIN PACKAGES



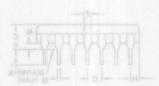




Mechanical Data







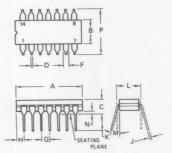


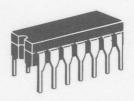
Mechanical Data

The package availability for each device is indicated on the front page of the individual data sheets. Dimensions for the packages are given in this chapter.

14-PIN PACKAGES

L SUFFIX CERAMIC PACKAGE **CASE 632**





NOTES:

- NOTES:

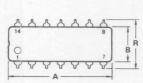
 1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.

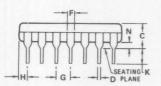
 2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

 3. DIMENSIONS "A" AND "B" DO NOT INCLUDE GLASS RUN-OUT.

	MILLIM	ETERS	INC	HES
DIM	MIN	MAX	MIN	MAX
Α	19.05	19.94	0.750	0.785
В	6.10	7.49	0.240	0.295
C	_	5.08	-	0.200
D	0.38	0.58	0.015	0.023
F	1.40	1.77	0.055	0.070
G	2.54	BSC	0.100	BSC
Н	1.9	2.29	0.075	0.090
J	0.20	0.38	0.008	0.015
K	3.18	5.08	0.125	0.200
L	7.62	BSC	0.300	BSC
M		15°	-	15°
N	0.51	1.02	0.020	0.040

P SUFFIX PLASTIC PACKAGE **CASE 646**

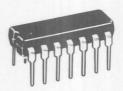








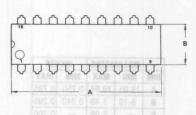
- 1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
- 2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
- 3. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH
- 4. ROUNDED CORNERS OPTIONAL.



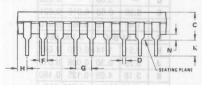
	MILLIN	ETERS	INC	HES
DIM	MIN	MAX	MIN	MAX
A	18.16	19.56	0.715	0.770
В	6.10	6.60	0.240	0.260
C	4.06	5.08	0.160	0.200
D	0.38	0.53	0.015	0.021
F	1.02	1.78	0.040	0.070
G	2.54	BSC	0.100	BSC
Н	1.32	2.41	0.052	0.095
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	7.62	BSC	0.300	BSC
M	0	10°	0°	10"
N	0.51	1.02	0.020	0.040

18-PIN PACKAGES

P SUFFIX PLASTIC PACKAGE CASE 707







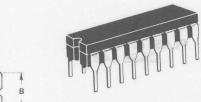


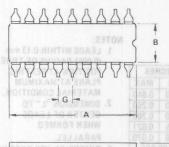
NOTES:

- POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25mm(0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
- 2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
- 3 DIMENSION B DOES NOT INCLUDE MOLD FLASH.

	MILLIN	ETERS	INC	HES	
DIM	MIN	MAX	MIN	MAX	
Α	22.22	23.24	0.875	0.915	
В	6.10	6 60	0.240	0.260	
C	3.56	4.57	0.140	0.180	
D	0.36	0.56	0.014	0.022	
F	1.27	1.78	0.050	0.070	
G	2.54	BSC	0.100 BSC		
H	1.02	1.52	0.040	0.060	
J	0.20	0.30	0.008	0.012	
K	2.92	3.43	0.115	0.135	
L	7.62	BSC	0.300	BSC	
M	00	150	00	150	
N	0.51	1.02	0.020	0.040	

L SUFFIX CERAMIC PACKAGE CASE 726







	DIM	MIN	MAX
	A	22.35	23.11
-	В	6.10	7.49
	C	-	5.08
	D	0.38	0.53
7://	F	1.40	1.78
	G	2.54	BSC
	H	0.51	1.14
1	- 1	0.20	0.30

SOLL	IAL AT LEAL	1001190	0 0 0001	WE:U	7.62
	(at bo)	8.8.1	001	00	
141 8	FIRE OF	ишол а	SEATING	PLANE	
	-	- D			

C

MILLIMETERS INCHES MIN MAX 0.880 0.910 0.240 0.295 0.200 0.015 0.021 0.055 0.070 0.100 BSC 0.020 0.045 0.008 0.012 K 3.18 4.32 0.125 0.170 7.62 BSC 0.300 BSC M 15° 15° N 0.51 1.02 0.020 0.040

NOTES:

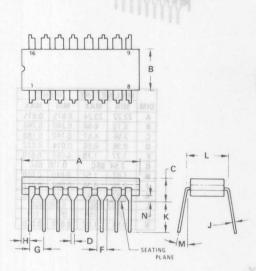
1. LEADS TRUE POSITIONED WITHIN 0.25 mm (0.010) DIA. AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.

2. DIM. "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

3. DIM. "A" & "B" INCLUDES MENISCUS.

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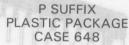


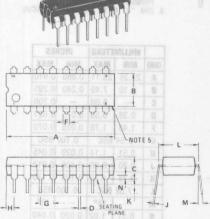


1	MILLIM	ETERS	INC	IES
DIM	MIN	MAX	MIN	MAX
A	19.05	19.94	0.750	0.785
В	6.10	7.49	0.240	0.295
C	-	5.08	-	0.200
D	0.38	0.53	0.015	0.021
F	1.40	1.78	0.055	0.070
G	2.54	BSC	0.100	BSC
H	0.51	1.14	0.020	0.045
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	7.62	BSC	0.300	BSC
M	BURAS	15°	IAMOIT	15°
N	0.51	1.02	0.020	0.040

NOTES:

- LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAX-IMUM MATERIAL CONDITION.
 PACKAGE INDEX: NOTCH IN LEAD NOTCH IN
- CERAMIC OR INK DOT.
- 3. DIM. "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
 4. DIM. "A" AND "B" DO NOT INCLUDE GLASS RUN-OUT.
- DIM "F" MAY NARROW TO 0.76 mm (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY





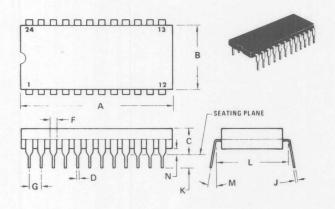
	MILLIN	ETERS	INCHES		
DIM	MIN	MAX	MIN	MAX	
A	18.80	21.34	0.740	0.840	
В	6.10	6.60	0.240	0.260	
C	4.06	5.08	0.160	0.200	
D	0.38	0.53	0.015	0.021	
F	1.02	1.78	0.040	0.070	
G	2.54	BSC	0.100 BSC		
Н	0.38	2.41	0.015	0.095	
J	0.20	0.38	0.008	0.015	
K	2.92	3.43	0.115	0.135	
L	7.62	BSC	0.300	BSC	
M	00	100	00	100	
N	0.51	1.02	0.020	0.040	

NOTES:

- 1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
- 2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED
 - PARALLEL.
- 3. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
- 4. "F" DIMENSION IS FOR FULL LEADS. "HALF" LEADS ARE OPTIONAL AT LEAD POSITIONS 1, 8, 9, and 16).
- 5. ROUNDED CORNERS OPTIONAL

24-PIN PACKAGES

L SUFFIX CERAMIC PACKAGE CASE 623



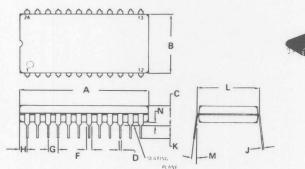
	MILLIMETERS		INCHES		
DIM	MIN	MAX	MIN	MAX	
Α	31.24	32.77	1.230	1.290	
В	12.70	15.49	0.500	0.610	
C	4.06	5.59	0.160	0.220	
D	0.41	0.51	0.016	0.020	
F	1.27	1.52	0.050	0.060	
G	2.54 BSC		0.100 BS0		
J	0.20	0.30	0.008	0.012	
K	3.18	4.06	0.125	0.160	
L	15.24 BSC		0.600 BSC		
M	0°	15°	0°	15°	
N	0.51	1.27	0.020	0.050	

NOTES:

1. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

2. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION. (WHEN FORMED PARALLEL)

P SUFFIX PLASTIC PACKAGE CASE 709



	MILLIMETERS		INCHES		
DIM	MIN	MAX	MIN	MAX	
A	31.37	32.13	1.235	1.265	
В	13.72	14.22	0.540	0 560	
C	3.94	5.08	0.155	0.200	
D	0.36	0.56	0.014	0.022	
F	1.02	1.52	0.040	0.060	
G	2.54	BSC	0.100 BS		
H	1.65	2.03	0.065	0.080	
1	0.20	0.38	0.008	0.015	
K	2.92	3.43	0.115	0.135	
L	15.24 BSC		0.600 BSC		
M	00	150	00	150	
N	0.51	1.02	0.020	0.040	

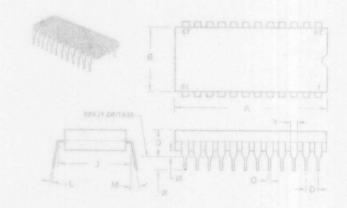


NOTES:

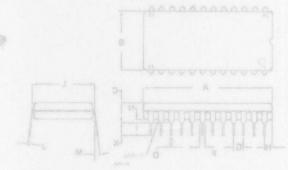
- POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 mm (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
- 2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
- 3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

4

24-PIN PACKAGES



				1	



	MIN			
				L
				N

Handling Procedures for CMOS Devices

Motorola CMOS devices have diode input protection against adverse electrical environments such as electrostatic discharge, in regards to this, the following statement is included on each data sheet:

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leqslant (V_{in} \text{ or } V_{out}) \leqslant V_{DD}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

Unfortunately, severe electrical transient voltages can be generated during handling. For example, static voltages generated by a person walking across a common waxed floor have been measured in the 4 to 15 kV range (depending on humidity, surface conditions, etc.). These static voltages are potentially dangerous when discharged into a CMOS input, considering the energy stored in the capacity (≈ 300 pF) of the human body at these voltage levels.

Present CMOS gate protection structures can generally protect against overvoltages. This is usually sufficient except in the severe cases.

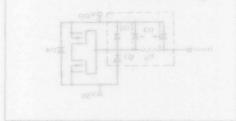
The input protection circuit, while adding some delay time, provides protection by clemping positive and negative potentials to Vpp and Vss respectively. Figure 1 shows the internal circuitry for the diode-resistor protection.

The input protection circuit consists of a series isolation resistor RS, whose typical value is 1.5 k Ω , and diodes D1 and D2, which clamp the input voltages between the power supply pins Vpp and Vss. Diode D3 is a distributed structure resulting from the diffusion fabrication of Rs.

FIGURE 1 - SCHEMATIC DIAGRAM, DIODE-RESISTOR INPUT PROTECTION

S

Handling Precautions



In addition to the internal protection network, the following steps are recommended to further reduce damage to CMOS integrated circuits due to improper handling.

 All CMOS devices should be stored or transported in materials that are antistatic. CMOS devices must not be inserted into conventional plastic "snow", styrofoam or plastic trays; but should be left in their original container until ready for use. Motorola CMOS devices have diode input protection against adverse electrical environments such as electrostatic discharge. In regards to this, the following statement is included on each data sheet:

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leqslant (V_{in} \text{ or } V_{out}) \leqslant V_{DD}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

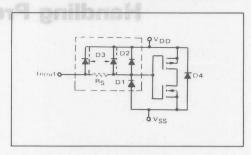
Unfortunately, severe electrical transient voltages can be generated during handling. For example, static voltages generated by a person walking across a common waxed floor have been measured in the 4 to 15 kV range (depending on humidity, surface conditions, etc.). These static voltages are potentially dangerous when discharged into a CMOS input, considering the energy stored in the capacity ($\approx 300~\text{pF}$) of the human body at these voltage levels.

Present CMOS gate protection structures can generally protect against overvoltages. This is usually sufficient except in the severe cases.

The input protection circuit, while adding some delay time, provides protection by clamping positive and negative potentials to VDD and VSS respectively. Figure 1 shows the internal circuitry for the diode-resistor protection.

The input protection circuit consists of a series isolation resistor RS, whose typical value is 1.5 k Ω , and diodes D1 and D2, which clamp the input voltages between the power supply pins VDD and VSS. Diode D3 is a distributed structure resulting from the diffusion fabrication of RS.

FIGURE 1 — SCHEMATIC DIAGRAM, DIODE-RESISTOR INPUT PROTECTION

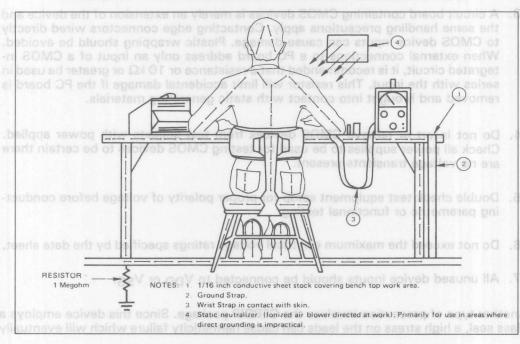


In addition to the internal protection network, the following steps are recommended to further reduce damage to CMOS integrated circuits due to improper handling.

 All CMOS devices should be stored or transported in materials that are antistatic. CMOS devices must not be inserted into conventional plastic "snow", styrofoam or plastic trays, but should be left in their original container until ready for use.

- 2. The shipping rails are antistatically treated inside and outside. They provide adequate protection during storage and test/assembly handling operations, but should not be re-cycled as continuous use will cause deterioration of the antistatic coating.
 - 3. All CMOS devices should be placed on a grounded bench surface and operators should ground themselves prior to handling devices, since a worker can be statically charged with respect to the bench surface. Wrist straps in contact with skin are strongly recommended. See Figure 2.
- Nylon or other static generating materials should not come in contact with CMOS circuits.
- 5. If automatic handling is being used, high levels of static electricity may be generated by the movement of devices or boards. Avoid this by grounding suspect areas and/or by the use of ionized air blowers, and/or air humidifiers.
 - Cold chambers using CO₂ for cooling should be equipped with baffles, and devices must be contained on or in conductive material.
- 7. When lead-straightening or hand-soldering is necessary, provide ground straps for the apparatus used and be sure that soldering ties are grounded.
 - 8. The following steps should be observed during wave solder operations.
 - The solder pot and conductive conveyor system of the wave soldering machine must be grounded to an earth ground.

FIGURE 2 - TYPICAL MANUFACTURING WORK STATION

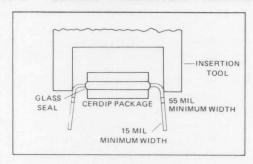


- b. The loading and unloading work benches should have conductive tops which
- c. Operators must comply with precautions previously explained.
 - d. Completed assemblies should be placed in antistatic containers prior to being moved to subsequent stations.
- 9. The following steps should be observed during board cleaning operation.
- a. Vapor degreasers and baskets must be grounded to an earth ground. Operators must likewise be grounded.
 - b. Brush or spray cleaning should not be used.
- c. Assemblies should be placed into the vapor degreaser immediately upon removal from the antistatic container.
- d. Cleaned assemblies should be placed in antistatic container immediately after removal from the cleaning basket.
- e. High velocity air movement or application of solvents and coatings should be employed only when module circuits are grounded and a static eliminator is directed at the module.
- 10. The use of static detection meters for line surveillance is highly recommended.
- 11. All low impedance equipment (pulse generators, etc.) should be connected to CMOS inputs only after the CMOS is powered up. Similarly, this type of equipment should be disconnected before power is turned off.
- 12. Equipment specifications should alert users to the presence of CMOS devices and require familiarization with this specification prior to performing any kind of maintenance or replacement of devices or modules.
- 13. A circuit board containing CMOS devices is merely an extension of the device and the same handling precautions apply. Contacting edge connectors wired directly to CMOS device inputs can cause damage. Plastic wrapping should be avoided. When external connections to a PC board address only an input of a CMOS integrated circuit, it is recommended that a resistance or 10 k Ω or greater be used in series with the input. This resistor will limit accidental damage if the PC board is removed and brought into contact with static generating materials.
- 14. Do not insert or remove CMOS devices from test sockets with power applied. Check all power supplies to be used for testing CMOS devices to be certain there are no voltage transients present.
- 15. Double check test equipment setup for proper polarity of voltage before conducting parametric or functional testing.
- 16. Do not exceed the maximum electrical voltage ratings specified by the data sheet.
- 17. All unused device inputs should be connected to V_{DD} or V_{SS}.

Another type of precaution involves the CERDIP package. Since this device employs a glass seal, a high stress on the leads can cause hermeticity failure which will eventually

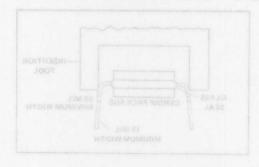
result in aluminum corrosion on the die. To avoid this, the leads should never be flexed above the seating plane. All insertion tools or automated equipment should contact the lead at its narrowest dimension allowing it to bend without affecting the wide portion above the seating plane.

FIGURE 3 — CERDIP INSERTION PRECAUTIONS



result in aluminum corrosion on the die. To avoid this, the leads should never be flexed above the seating plane. All insertion tools or automated equipment should contact the lead at its narrowest dimension allowing it to bend without affecting the wide portion above the seating plane.

FIGURE 3 - CERDIP INSERTION PRECAUTIONS



Reliability and Quality Assurance

Motorola has an active Quality Improvement Program with the objective of Improving failure rates and permitting tighter AQLs. At the time of writing — 83Q2 — the following data was applicable. For current data, please contact your Motorola Sales Office or franchised Motorola distributor.

OUTGOING QUALITY

Functional/Parametric Combined 0.10% AQL Level II

SATIAS SELLIAS

TABLE 1 - PAILURE NATES FOR PLASTIC AND CERAMIC PACKAGES

Failure Rate in %/1000 hours at Ambient Temperature:			
70°C			
0.0027	0.0003	Plastic Ceramic	

The Motorola Philosophy

Our objective is to further improve our position as the quality leader in the supply of semiconductor products.

Our strategies are:

- Actively promote a quality conscious attitude and quality environment in all process, manufacturing and support operations.
 - 2. Actively promote quality improvement plans.
- Quality Assurance
 - 1. Constantly measure and provide product reliability data.
 - 5. Support and develop the Motorola world-wide P.P.M. culture.
 - 3. Provide a fast responsive service for investigating customer related problems.
- Further improve good working relationships with customers' quality/engineering operations.

Reliability and Quality Assurance

Motorola has an active Quality Improvement Program with the objective of improving failure rates and permitting tighter AQLs. At the time of writing -83Q2 — the following data was applicable. For current data, please contact your Motorola Sales Office or franchised Motorola distributor.

OUTGOING QUALITY

Functional/Parametric Combined 0.10% AQL Level II

Visual/Mechanical Combined 0.15% AQL Level II

FAILURE RATES

TABLE 1 — FAILURE RATES FOR PLASTIC AND CERAMIC PACKAGES

Package	Failure Rate in %/1000 hours at Ambient Temperature:				
	50°C	70°C	85°C		
Plastic	0.0003	0.0027	0.0109		
Ceramic	0.0001	0.0006	0.0025		

The Motorola Philosophy

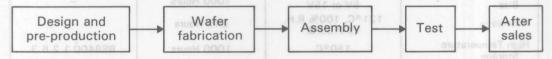
Our objective is to further improve our position as the quality leader in the supply of semiconductor products.

Our strategies are:

- 1. Actively promote a quality conscious attitude and quality environment in all process, manufacturing and support operations.
- 2. Actively promote quality improvement plans.
- 3. Maintain and improve programmes for the
 - 3. Maintain and improve programmes for the continuous improvement of outgoing quality and reliability.
 - 4. Constantly measure and provide product reliability data.
 - 5. Support and develop the Motorola world-wide P.P.M. culture.
 - 6. Provide a fast responsive service for investigating customer related problems.
 - 7. Further improve good working relationships with customers' quality/engineering operations.

Reliability and Quality Assurance Activities

In order to assure conformance to specifications, and to assure high levels of quality and reliability, there are R & QA activities in all parts of the production cycle.



Supporting all these activities is our product analysis group and providing supplementary support is our Hi-Rel operations group.

1. PRE-PRODUCTION

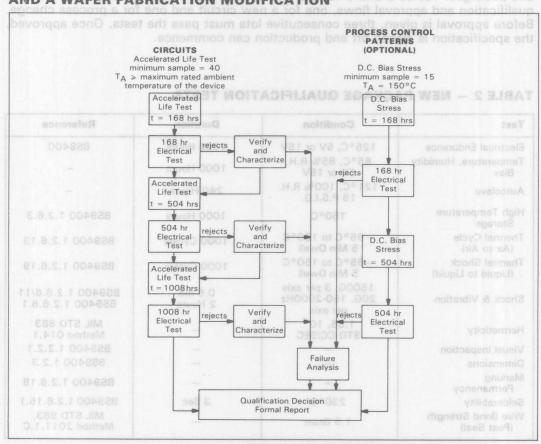
Quality Assurance starts before production commences. Within Motorola, all new production related activities and modifications thereto must be specified, qualified and approved prior to implementation. The form of control is defined by the change, and different controls are used for suppliers, raw materials, processes, equipments, designs and packages. Tables 2 and 3 list the qualification tests. Figure 1 shows two typical qualification and approval flows, one for a new circuit and one for a process change. Before approval is given, three consecutive lots must pass the tests. Once approved, the specification is signed off and production can commence.

TABLE 2 - NEW PACKAGE QUALIFICATION TESTS

Test	Condition	Duration	Reference
Electrical Endurance	125°C, 5V or 15V	1000 Hours	BS9400
Temperature, Humidity Bias	85°C, 85% R.H. 5V or 15V	1000 Hours	
Autoclave	121°C, 100% R.H. 15 P.S.I.G.	240 Hours	
High Temperature Storage	150°C	1000 Hours	BS9400 1.2.6.3
Thermal Cycle (Air to Air)	-65°C to 150°C 5 Min Dwell	1000 Cycles	BS9400 1.2.6.13
Thermal Shock (Liquid to Liquid)	-65°C to 150°C 5 Min Dwell	1000 Cycles	BS9400 1.2.6.19
Shock & Vibration	1500G, 3 per axis 20G, 150-2000Hz per axis	0.5 mS 2 Hours	BS9400 1.2.6.6/11 BS9400 1.2.6.8.1
Hermeticity	1.85, 10 ⁻⁸ STD CC/SEC	Elegerical rejects Test	MIL STD 883 Method 014.1
Visual Inspection			BS9400 1.2.2.1
Dimensions	Faiture, Anglysia	_	BS9400 1.2.3
Marking Permanency	-		BS9400 1.2.6.18
Solderability	230°C 00 000000 00000	3 Sec	BS9400 1.2.6.15.1
Wire Bond Strength (Post Seal)	1.5 Gram		MIL STD 883, Method 2011.1.C

Test	Condition	Duration	Reference
Electrical Endurance	125°C, 5V or 15V	1000 Hours	BS9400
Temperature, Humidity Bias	85°C, 85% R.H. 5V or 15V	1000 Hours	Mark (Autona) Due
Autoclave	121°C, 100% R.H. 15 P.S.I.G.	240 Hours	Design and
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Thermal Shock (Liquid to Liquid)	-65°C to 150°C 5 Min Dwell	1000 Cycles	BS9400 1.2.6.19
Shock & Vibration	1500G, 3 per axis 150-2000Hz, 20G, per axis	0.5 mS 2 Hours	BS9400 1.2.6.6/11 BS9400 1.2.6.8.1
Data Retention Bake (Non Volatile Memories)	200/250°C	1000 Hours	Quality Assurance st
s ans nerricus hame	and an initial near the sine		HOTOR DATE OF COLUMN

FIGURE 1 — QUALIFICATION AND APPROVAL FLOW FOR A NEW CIRCUIT AND A WAFER FABRICATION MODIFICATION



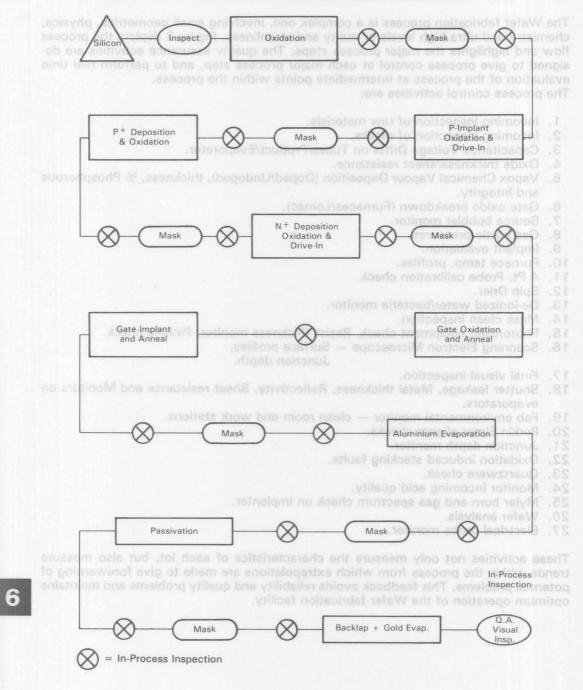
2. WAFER FABRICATION TAGINARY HELAW 20MG - S BRUDIT

The Wafer fabrication process is a complex one, involving small geometries, physics, chemistry and ultra high levels of purity and cleanliness. Figure 2 depicts the process flow and highlights the major process steps. The quality assurance activities are designed to give process control at each major process step, and to perform real time evaluation of the process at intermediate points within the process. The process control activities are:

- 1. Incoming inspection of raw materials.
- 2. Incoming inspection of masks.
- 3. Capacitance Voltage Drifts on Tubes/Product/Evaporator.
- 4. Oxide thickness/sheet resistance.
- Vapox Chemical Vapour Deposition (Doped/Undoped), thickness, % Phosphorous and Integrity.
- 6. Gate oxide breakdown (Furnaces/Lomac).
- 7. Source bubbler monitor.
- 8. Gas bottle pressures.
- 9. Implant evaluation.
- 10. Furnace temp. profiles.
- 11. 4 Pt. Probe calibration check.
- 12. Spin Drier.
- 13. De-ionized water/bacteria monitor.
- 14. Mask clean inspection.
- 15. Photoresist equipment check, Resist thickness monitor, Pinhole check.
- Scanning Electron Microscope Surface profiles, Junction depth.
- 17. Final visual inspection.
- 18. Shutter leakage, Metal thickness, Reflectivity, Sheet resistance and Monitors on evaporators.
- 19. Fab environmental monitor clean room and work stations.
- 20. Perkin Elmer aligner checks.
- 21. Junction depth monitor.
- 22. Oxidation induced stacking faults.
- 23. Quartzware check.
- 24. Monitor incoming acid quality.
- 25. Mylar burn and gas spectrum check on implanter.
- 26. Wafer analysis.
- 27. Electrical probe monitor.

These activities not only measure the characteristics of each lot, but also measure trends within the process from which extrapolations are made to give forewarning of potential problems. This feedback avoids reliability and quality problems and maintains optimum operation of the Wafer fabrication facility.

FIGURE 2 — CMOS WAFER FABRICATION (SIMPLIFIED)

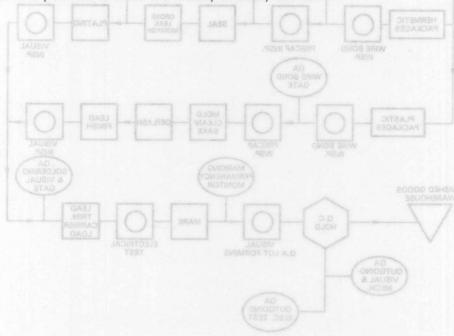


MOURE 3 - TYPICAL INTEGRATED CIRCUITS ASSEMBLY AND STATEMENT STATE

Assembly is highly automated — which benefits reliability and quality. In addition to the 100% screens, there are the following assembly quality activities:

- 1. Incoming inspection of raw materials.
- 2. Scribe audit.
- 3. Die high power visual inspection.
- 4. Die bond inspection.
- 5. Wire bond inspection.
- 6. Pre-cap inspection.
- 7. Hermeticity inspection.
- 8. Plating inspection.
- 9. Solderability.
- 10. Terminal strength.
- 11. Dimensions monitor.
- 12. Visual/mechanical inspection for flaws to body/leads.
- 13. Calibration monitor.
- 14. Moisture monitor.

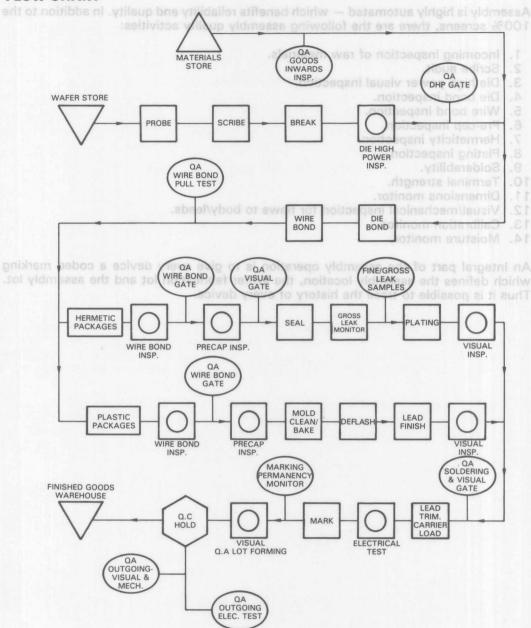
An integral part of the assembly operation is to give every device a coded marking which defines the assembly location, the Wafer fabrication lot and the assembly lot. Thus it is possible to trace the history of every device.



6

FLOW CHART

FIGURE 3 — TYPICAL INTEGRATED CIRCUITS ASSEMBLY & FINAL TEST FLOW CHART



The most significant test is high temperature electrical endurance which is pTeTed.

After 100% electrical test, there is a final inspection before the product is shipped to the warehouse. The inspection is

Functional/parametric combined 0.10% AQL Level II* un eff. assiveb eff to some Visual/mechanical combined to 0.15% AQL Level II* a bas sebapatwob sintements

Electrical parameters include all parameters on the data sheet. Visual/mechanical includes marking legibility, plating, dimensions, etc. We even include the orientation of the devices within the tube!

We believe these are the best AQLs for standard CMOS product in the Semiconductor Industry, and our objective is to maintain this position.

In addition, Motorola has a series of weekly audits as follows:

- 1. Finished goods.
- 2. Marking/marking permanency.
- 3. Hermeticity.
- 4. Dimensions.
- 5. Outgoing shipments.
- 6. Specifications/procedures. Secretary of the specifications of the failure failure for the failure for the failure failure for the failure failure for the failure f
- 7. Static protection. The volume of the state of the stat
- 8. General housekeeping.
- 9. Calibration.

The combination of audits and lot inspection is designed to give maximum protection to our customers. Feedback from our customers shows that they find a reject rate of typically less than 200 PPM, i.e. 1 failure in every 5,000 parts supplied. At this low level, incoming inspection is not cost efficient and it is possible to reduce or eliminate incoming inspection.

Of equal importance to incoming quality is product reliability. Motorola has a comprehensive reliability program which assesses all aspects of product reliability. The program comprises the following periodic tests which are designed to provide mechanical, environmental and electrical stresses which will accelerate the life cycle into a short period:

- Wisual inspection, dw wol ylpnizesigmi ai bins 4 silusif ni berigsig ai (assey 308,8
- Dimensions.
- Marking permanency.
- Resistance to cleaning fluids.
- Solderability and plating.

 Acceleration
- Acceleration.
- Wire bond.
- Hermeticity.
- Thermal shock.
- Temperature cycling.
- Mechanical shock and vibration.
- Flammability.
- High temperature storage. abivoid like topoid oitself etnemnotivne viibimuri to
- High temperature electrical endurance. Ilbnoo gnits eqo lamon erom ni teoo rewol
- Temperature/humidity/bias. med-non yllaplanistni era sepiveb begastag pizzela IIA
- Pressure/temperature/humidity.

^{*} Correct as of 8302, nso dointy was absq bried sylvent mulnimula and to nois

The most significant test is high temperature electrical endurance which is performed at 125°C with the application of a 15V static bias in accordance with the truth table of the individual device. This test accelerates any inherent die related failure mechanisms.

Electrical tests to Motorola Data Sheet specifications are used to measure the performance of the devices. The number of failures at the 1,008 hour readout (including both parametric downgrades and catastrophics) are extrapolated to a lower temperature to provide a failure rate at 85 °C. The mathematical models employed to predict this are detailed in the appendix to this chapter.

TABLE 4 — HIGH TEMPERATURE ELECTRICAL ENDURANCE RESULTS
FOR PLASTIC PACKAGES (1982) Inches a control of the second evening and the second

No. of Batches	No. of Devices	No. of Device Hours at 125°C	Equivalent Device Hours at 85°C	No. of Failures		Failure Rate / 1,000 hou Temperature 70°C	
35	3,302	3.33M (380 years)	86.31M (9,850 years)	8	0.0003	0.0027	0.0109

The failure rate at 85 °C of 0.0109% / 1,000 hours (or a mean time between failures of 1,047 years) is graphed in Figure 4 and compares favourably with our 1981 standard of 0.030% / 1,000 hours.

TABLE 5 — HIGH TEMPERATURE ELECTRICAL ENDURANCE RESULTS FOR CERAMIC PACKAGES (1982)

No. of Batches	No. of Devices	No. of Device Hours at 150°C	Equivalent Device Hours at 85°C	No. of Failures		Failure Rate / 1,000 hou Temperature 70°C	
r. Tiggpro	2,394	2.41M (275 years)	350.15M (39,971 years)	ch e se	0.0001	0.0007	0.003

The failure rate at 85°C of 0.003% / 1,000 hours (or a mean time between failures of 3,805 years) is graphed in Figure 4 and is impressingly low when compared with our 1981 standard of 0.014% / 1,000 hours.

The steady reduction of plastic and ceramic failure rates reflects Motorola's commitment to reliability and quality improvement. The improvements are such that many customers who previously purchased burnt-in components now achieve the same or better reliability using Motorola CMOS without burn-in.

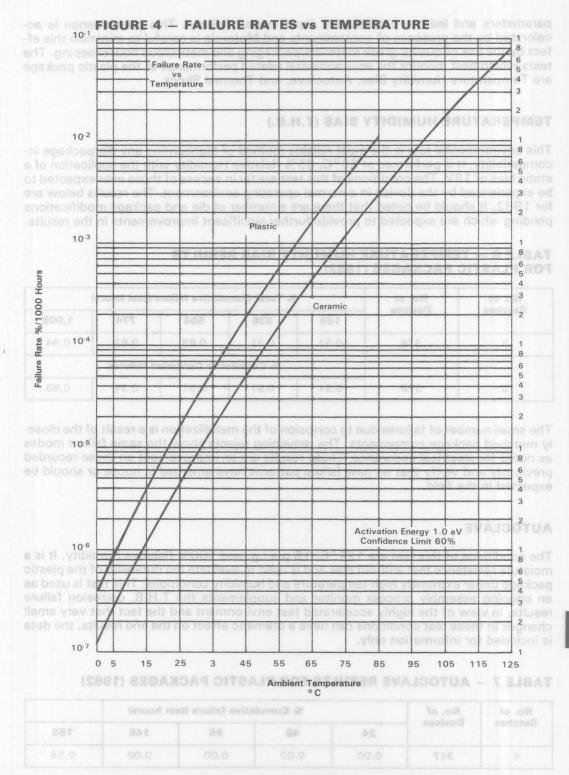
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CERAMIC vs PLASTIC

It is recommended that hermetic ceramic product be used in extreme high temperature or humidity environments. Plastic product will provide similarly excellent reliability for lower cost in more normal operating conditions.

All plastic packaged devices are intrinsically non-hermetic as moisture can penetrate the lead frame/package seal interface or diffuse through the bulk of the plastic. If water reaches the surface of the chip and a bias is applied, an electrolytic cell is set up. Corrosion of the aluminium tracks/bond pads can occur which can downgrade the device





parameters and lead to catastrophic (open metal) failures. This phenomenon is accelerated by the presence of contaminants and Motorola is careful to minimize this effect by the use of quality grade materials/packaging and meticulous housekeeping. The tests which best monitor the environmental related performance of the plastic package are Temperature Humidity Bias, Autoclave, and Thermal Shock.

TEMPERATURE HUMIDITY BIAS (T.H.B.)

This environmental test is the most reliable method of highlighting any die/package incompatibility. It is performed at 85°C, 85% Relative Humidity with the application of a static bias of 15V. The conditions of this test are far in excess of those ever expected to be experienced by the device in a normal operating environment. The results below are for 1982. It should be noted that there are a number of die and package modifications pending which are expected to provide further significant improvements in the results.

TABLE 6 — TEMPERATURE HUMIDITY BIAS RESULTS FOR PLASTIC PACKAGES (1982)

No. of Batches			% Total Cumulative failure (test hours)					
Butunus	168	336	504	774	1,008			
3	378	0.31	0.31	0.63	0.63	0.94		
9			% Cumul	ative Corrosic	on failures			
3	378	0.31	0.31	0.31	0.31	0.63		

The small number of failures due to corrosion of the metallization is a result of the closely matched package components. The remaining rejects show the same failure modes as noted for electrical endurance. These results are an improvement on those recorded previously and verify that no new failure patterns have emerged in house or should be expected in the field.

AUTOCLAVE

The conditions of this test are 121°C, 15 p.s.i.g. and 100% Relative Humidity. It is a moisture resistance test without bias and is used to evaluate the durability of the plastic package under extremely high temperature and humidity conditions. This test is used as an ongoing assembly process monitor and supplements the T.H.B. corrosion failure results. In view of the highly accelerated test environment and the fact that very small changes in these test conditions can have a dramatic effect on the end results, the data is included for information only.

TABLE 7 — AUTOCLAVE RESULTS FOR PLASTIC PACKAGES (1982)

No. of	No. of No. of Batches Devices		% Cumul	ative failure (t	est hours)	
Datches		24	48	96	148	168
4	347	0.00	0.00	0.00	0.00	0.58

The Autoclave results augment those recorded for T.H.B. performance and demonstrate the moisture resistant nature of the Motorola plastic encapsulated devices under extreme conditions.

THERMAL SHOCK

Thermal shock provides a quick and severe method of stress and is a liquid to liquid cycle between -65° C to $+150^{\circ}$ C with a dwell of five minutes at each temperature.

TABLE 8 — THERMAL SHOCK RESULTS FOR PLASTIC PACKAGES (1982)

No. of Batches	No. of Devices	% Cumulative f	ailure (test cycles
Datonos	Dovices	200	1,000
2	250	0.00	0.00

The results verify the plastic mould compound, bond wires and lead frames have closely matched coefficients of expansion. This benefit reduces the potential of moisture ingress (e.g. during the T.H.B. test) within the package ensuring a stable encapsulant for the die.

There is one further important source of quality and reliability data—feedback from our customers!

5. AFTER SALES

CUSTOMER FEEDBACK ENSURES QUALITY IMPROVEMENT

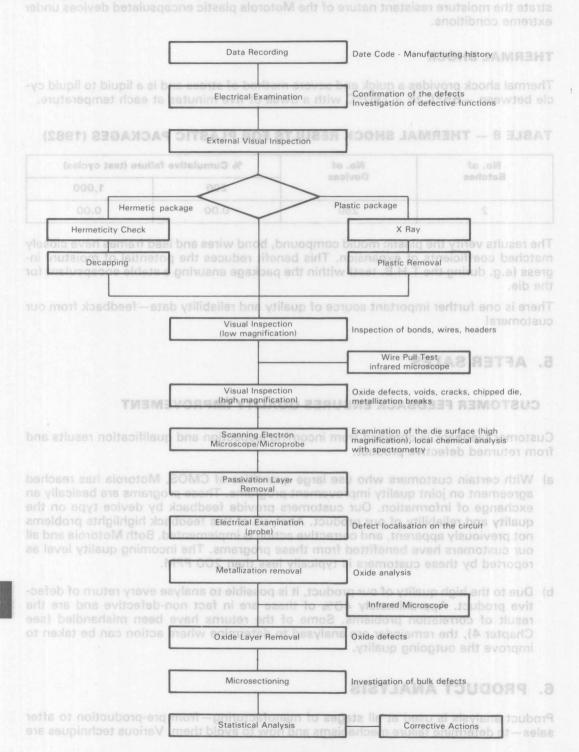
Customer feedback is obtained from incoming inspection and qualification results and from returned defective product.

- a) With certain customers who use large quantities of CMOS, Motorola has reached agreement on joint quality improvement programs. These programs are basically an exchange of information. Our customers provide feedback by device type on the quality and reliability of our product. Analysis of this feedback highlights problems not previously apparent, and corrective action is implemented. Both Motorola and all our customers have benefitted from these programs. The incoming quality level as reported by these customers is typically less than 200 PPM.
- b) Due to the high quality of our product, it is possible to analyse every return of defective product. Approximately 40% of these are in fact non-defective and are the result of correlation problems. Some of the returns have been mishandled (see Chapter 4), the remainder are analysed to determine where action can be taken to improve the outgoing quality.

6. PRODUCT ANALYSIS

Product analysis is used at all stages of manufacturing—from pre-production to after sales—to determine failure mechanisms and how to avoid them. Various techniques are

FIGURE 5 - ANALYSIS FLOW FOR FINISHED PRODUCT atluser evaluation of the state of th



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used and our failure analysis laboratory is well equipped with a variety of equipment including scanning electron microscopes, X-ray analysers and micromanipulative probers. Figure 5 shows the flow used for finished product.

7. HI-REL visit statistical property of beyond the sale statistical of the sale of the sal

Motorola's Hi-Rel programs—for avionic, space and military applications—has indirectly provided a considerable contribution to our commercial products. The Hi-Rel programs set the standards for the control of quality and the assessment of reliability, and at Motorola we use these standards for our commercial product as well as our Hi-Rel product. At the time of writing, Motorola has the following approvals for CMOS product:

DEF STAN 05/31 — MOD Registration 1G9M01
DEF STAN 05/21 — MOD Registration 1G9M01 vilsual anoitaulava validailar soni2
BSI — noitudinaib App. No. 1085 M au bassiuolas ai ara anuliat ent not noitamites

CECC App. No. M0070/CECC/UK 1085 M

CONCLUSION

With design and manufacturing facilities in the U.S.A., Japan and Europe, Motorola's experience in CMOS is unsurpassed. In Europe alone, Motorola has shipped over 500,000,000 CMOS devices. The levels of quality and reliability which we have achieved are extremely high. Through our quality improvement program, we will achieve even higher levels for the benefit of you, our customer.

The second model uses the Arrhenius Equation to relate the failure rate at test temperature to that expected at normal operating conditions.

 $R(T) = Ro EXP (E_0 / kT)$

where R(T) = reaction rate at normal temperatures

(Vef) verene mitevites - 3

L - Rollymann's constant

The use of junction temperatures rather than ambient (lifetest) temperature provides a more accurate failure rate. The junction temperature is computed using the equation

 $(AL\theta \times 9) + (A)T = (L)T$

where T(J) = junction temperature (°C)

T(A) = ambient temperature (°C)

θ_IA = average junction to ambient thermal resistance (°C/W)

6-15

Two mathematical models are employed to predict the failure rate. Firstly it is assumed that the failure rate distribution follows an exponential probability density function.

Motorola's Hi-Rel programs—for
$$(t \lambda - \sqrt{XX}) = (X)$$
 litery applications—has indirect-

where F(X) = probability density function

at Motorola we use these standards for our commercial star arulian vell as α ur Hi-Rel

product. At the time of writing, Motorola has the following approvals for CMOS pro-

Since reliability evaluations usually involve random samples of a population, a point estimation for the failure rate is calculated using the Chi-squared distribution.

$$\lambda = \frac{\chi^2 (\alpha, 2r + 2)}{2nt} \quad \alpha = \frac{(100 - CL)}{100}$$

where χ^2 = tabulated value

CL = confidence limit in percent bearings of the confidence limit in percent

500,000,000 CMOS devices. The levels of que estate and melch ave have

n me number of devices of the number of device

t = duration of the test

A confidence limit of 60% is employed in the formula.

The second model uses the Arrhenius Equation to relate the failure rate at test temperature to that expected at normal operating conditions.

$$R(T) = Ro EXP (E_a / kT)$$

where R(T) = reaction rate at normal temperatures

Ro = a constant

 $E_a = activation energy (1eV)$

k = Boltzmann's constant

T = junction temperature

The use of junction temperatures rather than ambient (lifetest) temperature provides a more accurate failure rate. The junction temperature is computed using the equation below:

$$T(J) = T(A) + (P \times \theta_{JA})$$

where T(J) = junction temperature (°C)

T(A) = ambient temperature (°C)

P = power (Watts)

 θ JA = average junction to ambient thermal resistance (°C/W)

Data Books, Brochures and Selection Guides

Additional information on CMOS products can be found in the following publications available at your nearest Motorola Sales Office or Distributor.

DATA BOOKS

ROO1 A/D and D/A Conversion Manual

ROO28 CMOS Data Manual, Volume 2, Special Functions

8002C CMOS Data Manual, Volume 3, High Speed CMOS

8003A Home Electronics / Integrated Circuits

3011 Memory Data Manual

8025 The European Master Selection

1039 Telecommunications Data Manual

BROCHURES AND SELECTION GUIDES

F045 Telecommunications, A System Approach

FO55 High Speed CMOS Function Selector Guide

-060 Catalog of Technical Literature

EARS CMOS Standard Logic Reliability Report

FD79 Macrocell Arrays and CAD

75 CMOS Function Selector Guide

:077 High Speed CMOS Life Test

APPRICATION MOTES

A complete list of Application Notes can be found in the Catalog of Technical Literature (Reference F060).

ANLESSA Motorola Complementary MOS I/C'S.

This note discusses some of the properties of N-channel and P-channel MOSFET's and describes how they are used to construct complementary MOS integrated circuits. Some basic CMOS logic functions are then discussed.

AN-707 Noise Immunity Comparison of CMOS versus Bipolar Logic Families.

Publications and Applications

Publications

Data Books, Brochures and Selection Guides

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DATA BOOKS

B001 A/D and D/A Conversion Manual
B002B CMOS Data Manual, Volume 2, Special Functions
B002C CMOS Data Manual, Volume 3, High Speed CMOS
B003A Home Electronics / Integrated Circuits
B011 Memory Data Manual
B025 The European Master Selection
B039 Telecommunications Data Manual

BROCHURES AND SELECTION GUIDES

F045 Telecommunications, A System Approach
F055 High Speed CMOS Function Selector Guide
F060 Catalog of Technical Literature
F062 CMOS Standard Logic Reliability Report
F072 Macrocell Arrays and CAD
F075 CMOS Function Selector Guide
F077 High Speed CMOS Life Test

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AN-538A Motorola Complementary MOS I/C's.

This note discusses some of the properties of N-channel and P-channel MOSFET's and describes how they are used to construct complementary MOS integrated circuits. Some basic CMOS logic functions are then discussed.

- AN-707 Noise Immunity Comparison of CMOS versus Bipolar Logic Families.
 - This application note compares the noise immunity of CMOS and bipolar families and includes general notes on common noise sources, precautions against noise, noise specification and standard noise tests.

AN-712A Interface Techniques between Industrial Logic and Power Devices.

This application note presents worst case design approaches to illustrate the methods of interfacing MCMOS and MHTL logic to various power load levels, both a.c. and d.c. Interface devices vary from small-signal transistors to power transistors and thyristors, using direct coupling/level translation and optoelectronic coupling techniques.

AN-715 Introduction to CMOS Integrated Circuits with Three-State Outputs.

This note describes a wide variety of standard CMOS integrated circuits incorporating transmission gates with standard logic. Design rules and applications of these devices include the areas of analog switching and multiplexing, digital multiplexing and data bussing.

AN-768 CMOS Schmitt Triggers.

The Motorola Schmitt triggers—MC14093B, MC14583B and MC14584B—are described. Operating characteristic, theory of operation, and applications of Schmitt triggers are covered.

AN-772 CMOS Monostable Multivibrators.

This note describes the theory and operation of the MC14538B precision monostable multivibrator, which incorporates both digital and linear CMOS technology. Applications are described.

AN-843 A Review of Transients and their means of Suppression.

Transient sources within and outwith electronic equipment are described and characterised, and methods of suppression, and their applications, are covered.

AN-874 Macrocell Arrays: Concept-Features-CAD Interface.

High technology array based products offer the advantages of custom circuits, yet overcome the problems of high costs and long design cycles. Recent developments in array technology make use of Macrocell building blocks rather than primitive gates for easier design and higher performance. Additional developments in computer-aided-design customer interface systems simplify the job of developing array circuit options. This note examines Motorola's Macrocell array concept with special emphasis on the CAD user interface.

Reliability and Quality Assurance

Publications and Applications

4		
1	This application note presents worst Selection Guides trate the methods of interfacing MCMOS and MHTL logic to various power load levels, both a.c. and d.c. Interface devices very from small-signal transistors to power translators and thyristors, using direct coupling/level translation and optoelectronic coupling techniques.	
		AN-715
2	This note describes a wide variety of standard CMO bandered of collecting B-Series Family Data and standard cations of these devices include the second catalogue of these devices include the standard standard of the standard standard of the standard standard of the standard standar	
	CMOS Schmitt Triggers.	
3	The Motorola Schmitt triggers-MC14083B, MC14583B and MC14584B—are described. Operating characteristic, theory of operation, and applications of Schmitt triggers are covered and applications of Schmitt triggers are covered	
	CMOS Monostable Multivibrators.	
	This note describes the theory and operation of the MC14538B precision monostable multivibrator, which incorporates both digital and linear CMOS technology. Applications are described.	
4	Transient sources within and outwire Data Mechanical Data within and methods of a Data within	
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	Reliability and	

Reliability and Quality Assurance

Publications and Applications